Power Systems on Chiplet: Inductor-Linked Multi-Output Switched-Capacitor Multi-Rail Power Delivery on Chiplets

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***Abstract*—The energy demand of future computing introduces new challenges in voltage regulator design. This paper explores an inductor-linked single-input multi-output hybrid switched-capacitor power architecture with modular output cells for 48-V to point-of-load (PoL) chiplet power delivery. The unique inductor-linked configuration of switched-capacitor circuits enables high performance with a high voltage conversion ratio while achieving high efficiency and high power density. The architecture can be used, for example, to support multiple loads in a chiplet with many voltage rails from a high voltage input.**

***Index Terms*—voltage regulation module (VRM), power architecture, magnetics, packaging, switched-capacitor, transformer**

I. Introduction

Voltage regulation modules (VRMs) with high efficiency, high power density, and high control bandwidth are needed to support future microprocessors [1]–[3]. Fig. 1 shows the principles of multi-chip power delivery in a chiplet with many regulated power delivery rails embedded in the interposer. In future multi-chip systems, many high current electronic loads are placed near each other. The size, cost, and performance benefit of heterogeneous integration make it desirable to design modular and miniaturized multi-output dc-dc converters that can be easily scaled in size for a variety of applications. Holistic innovations in architecture and packaging co-design are needed to power future high current chiplets.

One emerging trend in point-of-load power delivery is to feed the low-voltage high-current processors (e.g., <1-V, >500-A) with high voltage (e.g., 48-V) from the computer racks to leverage the existing telecom power ecosystems [4], [5]. Recent developments in high-density on-chip capacitor technologies (e.g., Deep Trench Capacitors (DTC), Metal-Insulator-Metal (MIM) capacitors) make switched capacitor circuits extremely attractive for integrated voltage regulators (IVRs) [6]–[8]. However, a switched capacitor IVR directly interfacing with 48-V is expensive and impractical due to the requirements of high voltage rating switches and capacitors [9]. A popular solution for high voltage conversion ratio and high output current applications is the two-stage intermediate bus architecture (IBA) [2]. In a two-stage IBA design, the front-end stage is usually implemented as an unregulated 48-V to lower voltage (12-V, 6-V, 4-V, 2-V) dc-dc converter [10]. The second stage is usually implemented as a multi-phase buck converter [11]. The switches of the front-end stage and the second stage do not need to handle high voltage and current stresses together. The two stages are usually linked by a large dc decoupling capacitor. Delivering massive current to a tiny space, the power converters need to be co-designed with the packaging with thorough power integrity and signal integrity considerations. Each power conversion stage usually needs one or more magnetic components, limiting the possibilities of system integration. Due to the very high current needed by future microprocessors, it is attractive to

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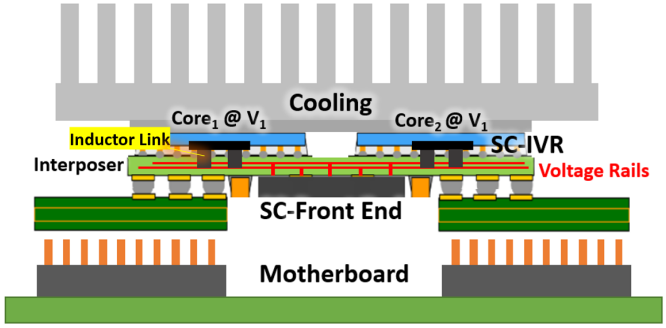

Fig. 1. Packaging principles of the inductor-linked hybrid switched capacitor multi-output architecture for chiplet power delivery. Power is delivered to multiple outputs through many switched voltage rails with multiple interface inductors. Both the front-end and back-end are switched-capacitor circuits.

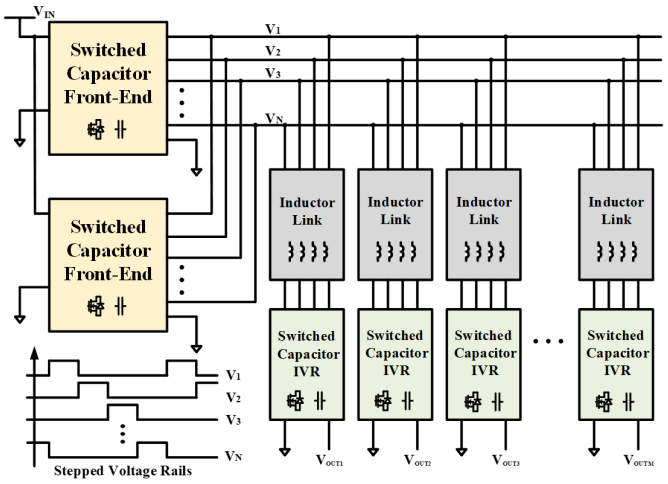

Fig. 2. Block diagram of the inductor-linked architecture with multiple switched capacitor input cells, multiple stepped voltage rails and inductor links, and multiple switched capacitor voltage regulators. The inductor links can be implemented as discrete inductors or coupled inductors

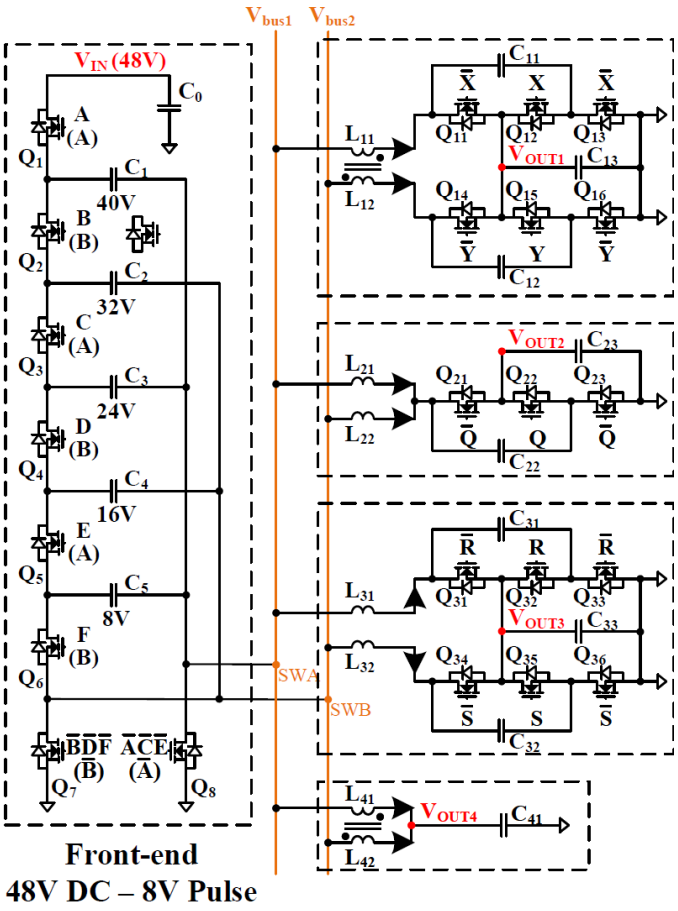

Fig. 3. An example inductor-linked power architecture with a five-capacitor six-level Dickson switched-capacitor converter as the front end to drive two switched voltage rails. Two pairs of coupled inductors are used as the inductor links to connect four switched-capacitor voltage regulators to the two switched voltage rails. The switched voltage rails have stepped voltage between 0-V and 8-V, and the switched-capacitor voltage regulators produce many different regulated output voltages for different loads.

move inductors further away from the chip to enable higher performance in-package or in-PCB magnetics, and rely on lower voltage switched-capacitor circuits to perform the final voltage regulation [12]–[14].

This paper presents a 48-V-to-1-V single-input multi-output VRM architecture which uses magnetic components as the intermediate link. It comprises a front-end switched capacitor stage to convert the 48-V input to multiple stepped voltage rails (e.g., 2-V, 4-V, 6-V, and 8-V) for power distribution and uses much lower voltage switched capacitor IVRs for voltage regulation. The inductor-link absorbs the parasitics in the power distribution network (PDN) and offers soft charging opportunities for most switched capacitors [15]. It is highly modular and well scalable to support many independently regulated output voltage rails.

II. Architecture Overview

Fig. 2 shows the key principles of the inductor-linked multi-output power delivery architecture comprises a switched capacitor (SC) input stage creating multiple stepped voltage rails ($v_{\Phi 1}$, $v_{\Phi 2}$, ..., $v_{\Phi M}$) for power delivery on the chiplet. Each voltage rail steps from 0-V to an intermediate bus voltage (e.g., 8-V) at the switching frequency of the input stage. The voltage rails are distributed across the interposer. Each core is supported by a switched-capacitor IVR. Each switched-capacitor IVR is connected to the stepped voltage rails through an inductor link. The inductor link can be implemented as multiple discrete inductors or a multiphase coupled inductor. Multiple switched capacitor input stages can be connected in parallel to provide an extended power rating. The number of switched capacitor input stages does not need to be equal to the number of SC IVRs, and they do not need to be operate at the same frequency. There is no intermediate bus capacitor between the two switched capacitor stages.

Fig. 3 shows an example implementation of the inductor link architecture, comprising a five-capacitor six-level Dickson switched-capacitor circuit as the input stage to drive two stepped voltage rails with voltages switching between 0-V and 8-V. The voltages of the flying capacitors in the Dickson switched-capacitor circuit are 40-V, 32-V, 24-V, 16-V, and 8-V, respectively. The two switching rails are loaded by four sets of different switched-capacitor voltage regulators with two parallel discrete or coupled inductors as the inductor-links.

Fig. 4 shows the switching sequences of the example implementation in Fig. 3. The six levels of the Dickson switched capacitor circuits (A, B, C, D, E, F) are phase shifted by 60° with the same duty ratio. The switched capacitor rectifiers (X, Y, R, S) do not need to be synchronized with the Dickson switched capacitor circuit and can have different duty ratios for voltage regulation. It is preferable to operate the switched capacitor voltage regulators at a frequency that is higher than that of the Dickson switched capacitor circuit to improve current sharing and voltage balancing of the two stages. Fig. 5 shows an alternative way of driving the example converter in Fig. 3. The six series stacked switches are grouped alternatively into two categories driven by two 180° phase-shifted signals (A, B). The floating switches ($Q_1 \sim Q_6$) switch at the same frequency as the ground-referenced switches ($Q_7 \sim Q_8$). This configuration is not fully soft-switched but can reduce the flying capacitor size as they are effectively operating at a higher frequency.

If the switching frequency of the floating switches ($Q_1 \sim Q_6$) is fixed, the switching frequency of the bottom side switches (Q_7, Q_8) with sequence (A, B, C, D, E, F) is three times higher than with the sequence (A, B, A, B, A, B) at the cost of more extreme duty cycle and higher loss at heavy load, resulting in three times higher pulse frequency of V_{bus1} and V_{bus2}. The control implemented by the switching sequence (A, B, C, D, E, F) is considered as a "soft-charging" mode [15] while the control implemented by the switching sequence (A, B, A, B, A, B) is considered as a "hard-charging" mode. The switching frequencies of the back-end switched-capacitor regulators after the inductor-links are designed to be two times higher than the frequency of the voltage buses, reducing the low-frequency harmonics caused by the voltage bus.

The inductor-linked multi-output architecture can be implemented in many different ways. The Dickson switched capacitor circuit can be replaced by any switched-capacitor cells with multilevel switch nodes having the same average

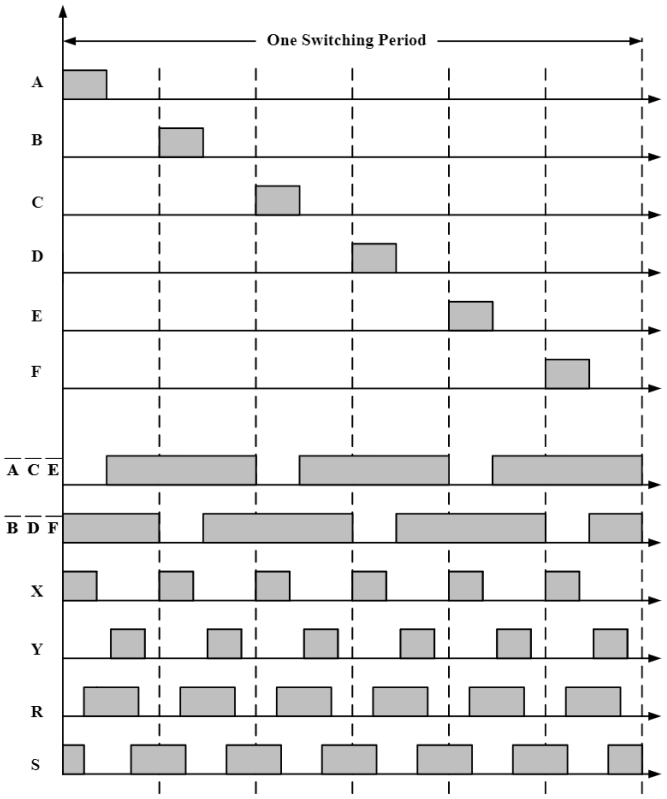

Fig. 4. Switching sequences of the switches labeled in Fig. 3. The six levels of the Dickson switched capacitor circuits (A, B, C, D, E, F) are phase shifted by 60° with the same duty ratio. The switched capacitor rectifiers (X, Y, R, S) do not need to be synchronized with the Dickson switched capacitor circuit and can have different duty ratios for voltage regulation.

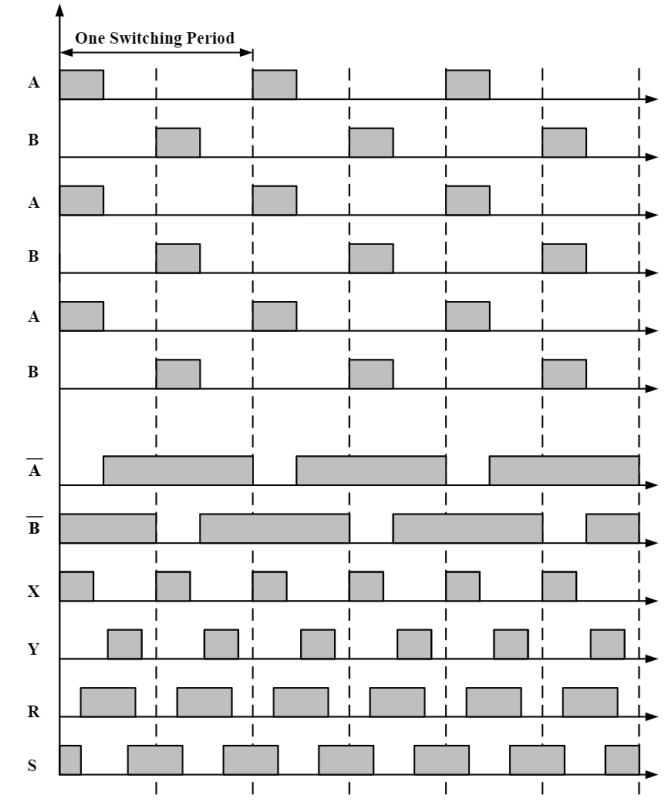

Fig. 5. An alternative switching sequence as labeled in Fig. 3. The six levels of the Dickson switched capacitor circuits are switches as two groups (A, B, A, B, A, B) with the same duty cycle and 180° phase shift.

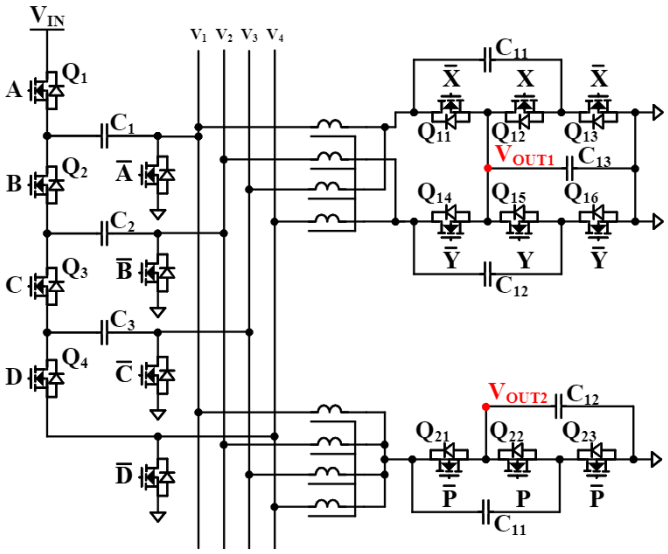

Fig. 6. An alternative way of implementing the inductor-link hybrid-switched-capacitor architecture with multiple intermediate voltage rails. The inductor-links are implemented as multiphase coupled inductors.

voltage, such as buck converters, flying capacitor multilevel converters (FCML) [16], or series-capacitor buck converters [17]. The intermediate voltage rails can be extended to have more phases similar to [18], albeit with stepped voltage but dc current. The switched-capacitor voltage regulators can be extended to have higher voltage conversion ratios. Fig. 6 shows an alternative way of implementing this architecture with four intermediate voltage rails and multiphase coupled inductors. This implementation enables soft-charging of all front-end capacitors and maximizes the benefits of coupled inductors.

III. Prototype Design

Design considerations for the inductor-linked hybrid switched capacitor architecture include: (1) Voltage rail selection for the inductor link: the voltage level and rail numbers of the inductor link should be selected according to the maximum voltage rating and current rating of the various loads in the chiplet. Delivering power at higher voltages reduces the current and reduces losses in the power distribution network but places more stress on the voltage regulator design. Delivering power with multiple voltage rails enables more topology options for the front stage but makes the design of the second stage more challenging because all voltage regulators need to interface with all voltage rails. (2) Topology selection of the switched-capacitor front-end: the switched-capacitor front-end should be selected according to the voltage levels and rail numbers of the inductor link. Multiphase buck converters or series buck converters can be naturally applied to drive multiple voltage rails. (3) Topology selection of the switched capacitor voltage regulator: the switched capacitor voltage regulator should be designed based on the voltage conversion ratios needed and the size and density of capacitors. Switched-capacitor, flying-capacitor, and boost-derived architectures are all applicable. (4) Magnetics implementation of the inductor link: each voltage regulator needs a multiphase magnetic

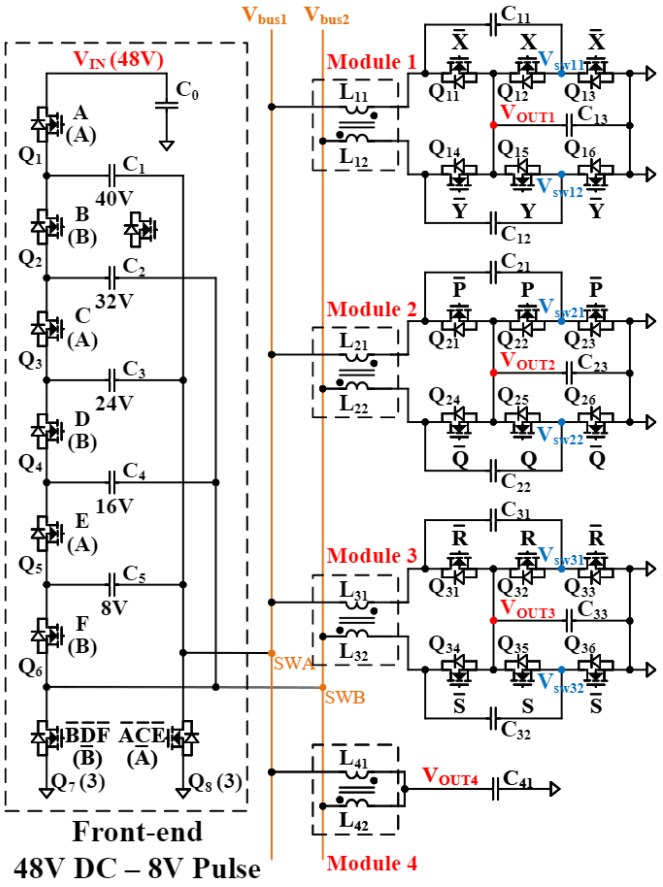

Fig. 7. Prototype schematic of the inductor-link multi-output VRM architecture with a 6-level Dickson switched-capacitor front-end and four back-end modules. Three modules are identical 2:1 switched-capacitor converters while one module is a voltage filter and outputs the average voltage of the bus. All modules are supported by coupled inductors.

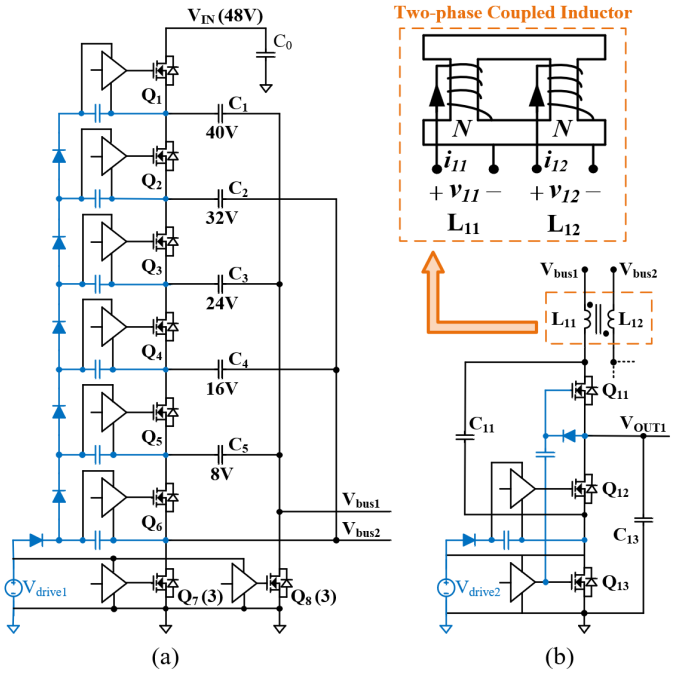

Fig. 8. (a) Gate drive implementation of the front-end switched-capacitor stage. A cascaded diode-chain provides the voltage needed for the gate drives of the floating switches with a very low component count and small board area. (b) Gate drive implementation of a single phase of one module in the second stage. The gate signal of the top switch Q_{11} is bootstrapped from the gate signal of the bottom switch Q_{13}. The power supply of the gate driver for the middle switch Q_{12} is bootstrapped from the voltage supply V_{drive2}. The winding structure of a two-phase coupled inductor is also shown here.

component to interface with the rails. The inductor links can be implemented as discrete or coupled inductors [19], [20].

The voltage conversion ratio of the inductor-linked hybrid converter can be modulated by the duty ratios of the front-end and the back-end. The duty ratio of the top-side switches in the front end (d_F) modulates the widths of the voltage pulses in the intermediate rails, and the duty ratio of the back end (d_B) modulates the output voltage. Fig. 7 shows an example implementation of the inductor-linked hybrid converter with a N-level Dickson ($N = 6$) switched-capacitor front-end. The back-end consists of three identical 2:1 switched-capacitor regulators and one coupled inductor voltage filter.

In the hard-charging operating mode (A, B, A, B, A, B), the front-end creates two voltage rails stepping between 0-V and V_{in}/N-V. With a front-end duty ratio of d_F, the average voltage at the input side of the coupled inductor is $d_F \times V_{in}/N$-V, which is also the average voltage at the input side of the back-end. For an inductor-input switched-capacitor rectifier, assume the duty ratio of the first and third switches of the rectifier (for example Q_{11} and Q_{13} in Fig. 7) is d_B. The volt-second relationship between the input and output is:

$$d_F \times \frac{V_{in}}{N} = d_B \times V_{out} + (1 - d_B) \times 2V_{out}. \quad (1)$$

The overall voltage conversion ratio is:

$$\frac{V_{out}}{V_{in}} = \frac{d_F}{N(2 - d_B)}. \quad (2)$$

With $d_F = 25\%$, $d_B = 50\%$, and $N = 6$, the voltage conversion ratio is $1/36$, leading to a 1.33-V V_{out} if V_{in} is 48-V. V_{out} can be regulated between 1-V and 2-V if d_F is fixed at 25% and d_B is modulated from 0% to 100%.

In the soft-charging opearting mode (A, B, C, D, E, F), the voltage bus has the same frequency as the front-end bottom-side switches, $N/2$ times higher than the front-end top-side switches. The corresponding duty ratio of the pulses on the voltage bus is $N/2$ times higher than the duty ratio of the top-side switches. The voltage relationship between the input and output is:

$$d_F \times \frac{V_{in}}{N} \times \frac{N}{2} = d_B \times V_{out} + (1 - d_B) \times 2V_{out}. \quad (3)$$

The overall voltage conversion ratio is:

$$\frac{V_{out}}{V_{in}} = \frac{d_F}{2(2 - d_B)}. \quad (4)$$

With $d_F = 8.33\%$, $d_B = 50\%$, and $N = 6$, the voltage conversion ratio is $1/36$, leading to a 1.33-V V_{out} if V_{in} is 48-V. The output can be regulated between 1-V and 2-V if d_F is fixed at 8.33% and d_B is modulated from 0% to 100%.

TABLE I
BILL-OF-MATERIAL OF THE 48 V INDUCTOR-LINK POL CONVERTER

Device & Symbol	Description
High-Side Switches, $Q_{1\sim6}$	Infineon BSZ031NE2LS5
Low-Side Switches, $Q_{7\sim8}$	Infineon BSZ011NE2LS5I
Switched Capacitors, $C_{1\sim5}$	Murata GRM32ER71J106
Gate Drivers for $Q_{1\sim6}$	ADI LTC4440
Gate Drivers for $Q_{7\sim8}$	TI LM5114
Switches, $Q_{11\sim36}$	EPC 2067
Switched / Output Capacitors, $C_{11\sim41}$	TDK C2012X5R0G476M
Coupled Inductors, $L_{11\sim42}$	Eaton CL1208
Gate Drivers for $Q_{11\sim36}$	TI LM5113

IV. EXPERIMENTAL RESULTS

A 48-V inductor-linked multi-output prototype with a 6-level switched-capacitor front-end and four independently controlled back-end modules are designed and tested. Table I lists the bill-of-material of the 48-V inductor-linked PoL converter.

Fig. 8a shows an example gate drive implementation of the front-end circuit. A cascaded bootstrapped diode-chain provides the voltage needed for the gate drives of the floating switches. Only level-shifters and ground-referenced gate drives are needed for this implementation. Fig. 8b shows an example gate drive implementation of the back-end circuit. The gate signal of the top switch Q_{11} is bootstrapped from the gate signal of the bottom switch Q_{13}. The power supply of the gate driver for the middle switch Q_{12} is bootstrapped from the voltage supply V_{drive2}.

Fig. 9a shows the annotated top and bottom views of the front-end switched capacitor stage. The six series-stacked switches ($Q_1 \sim Q_6$ in Fig. 8) are lined up on the right-hand side. Each of the ground-reference switches (Q_7 and Q_8 in Fig. 8) is implemented as three parallel MOSFETs to reduce the on-resistance. These six ground-reference MOSFETs are lined up on the left-hand side. The gate drive circuitry and several flying capacitors are on the top side of the layout. The cascaded diode-chain and several flying capacitors are on the bottom side of the layout. Each flying capacitor ($C_1 \sim C_5$) has 100 μF nominal capacitor values before dc-bias derating.

Fig. 9b shows the annotated top and bottom view of the back-end switched capacitor stage. Two groups of series stacked switches ($Q_{11} \sim Q_{16}$) are implemented as GaN switches and are lined up symmetrically. The 500 μF output capacitors (C_{13}) are placed beside the switches. The 100 nH coupled inductors (Eaton CL1208) and the 250 μF switched capacitors (C_{11} and C_{12}) are placed on the other side of the printed circuit board. Fig. 10 shows the top view of the front-end and one back-end module of the prototype.

The switching frequency of the front-end floating switches is set as 252.5 kHz. In the hard-charging mode (A, B, A, B, A, B), the switching frequency of the front-end bottom switches and the back-end switches are set as 252.5 kHz and 505 kHz, respectively. In the soft-charging mode (A, B, C, D, E, F), the switching frequency of the front-end bottom switches and the back-end switches are set as 757.6 kHz and 1.515 MHz, respectively. Fig. 11 shows the waveforms of the bus voltages and the inductor currents in the hard-charging operating mode.

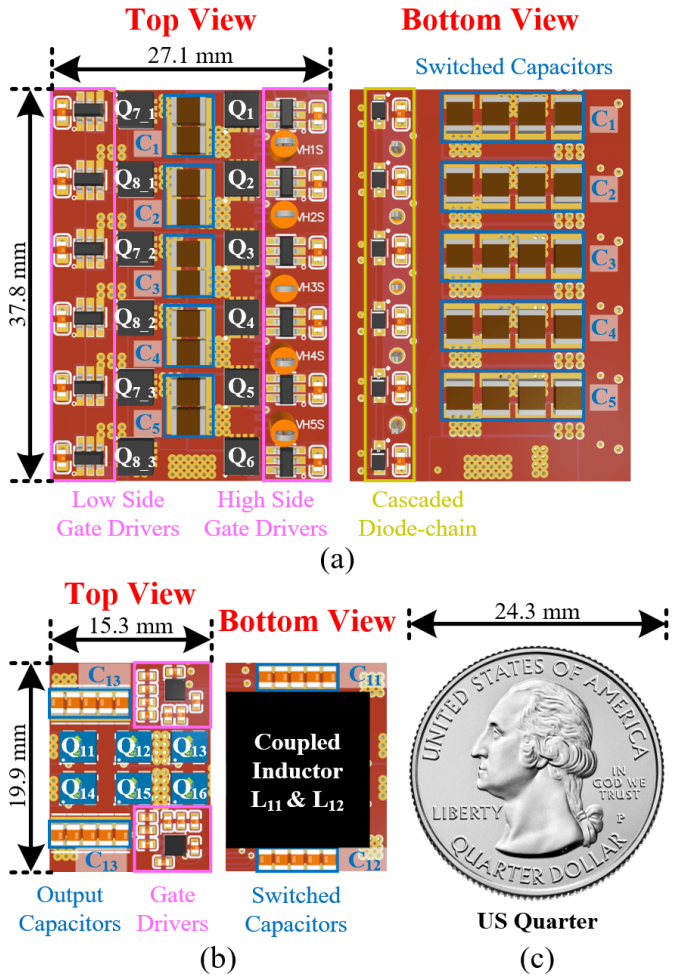

Fig. 9. Top and bottom views of the PCB layout of (a) the front-end of the prototype converter and (b) one back-end module of the prototype converter. (c) The size of a US Quarter. Each back-end regulator is smaller than a US quarter, having the potential to be integrated and stacked with each individual chip in the chiplet applications.

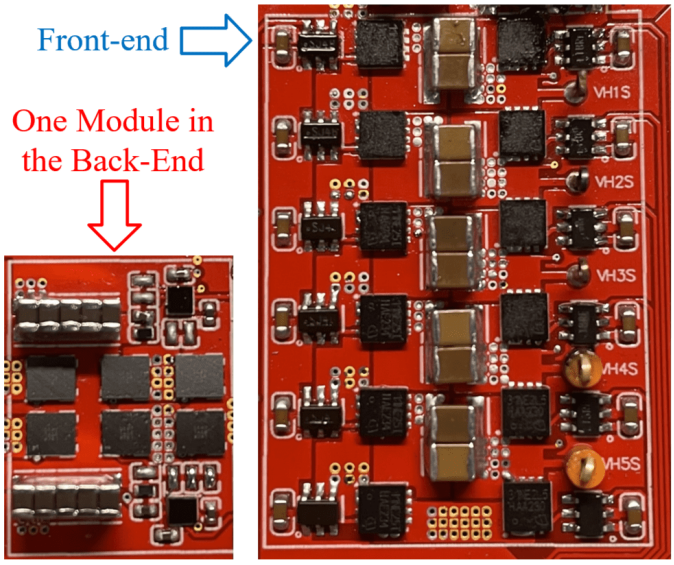

Fig. 10. Top view of the four-layer prototype converter. Both the front-end and one module in the back-end are shown. All gate drive circuits are included.

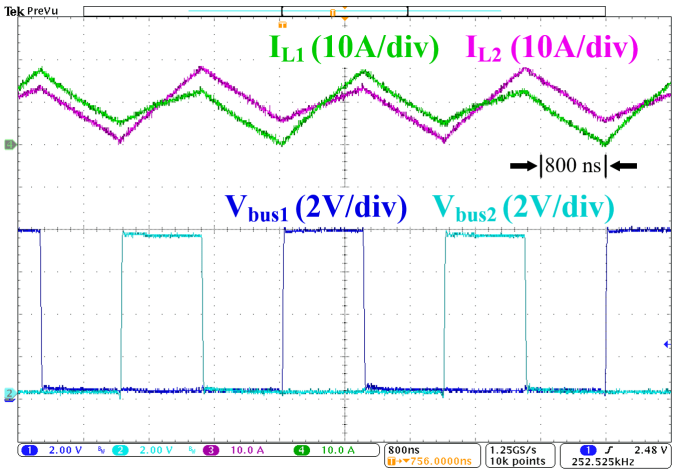

Fig. 11. Measured waveforms of the voltage buses and the inductor currents of Module 1 in the hard-charging operating mode. The frequency of the voltage buses and the currents of coupled inductor is 252.5-kHz and 505-kHz, respectively. The bus voltage is switching between 0-V and 8-V with 25% duty cycle, resulting in 2-V average bus voltage.

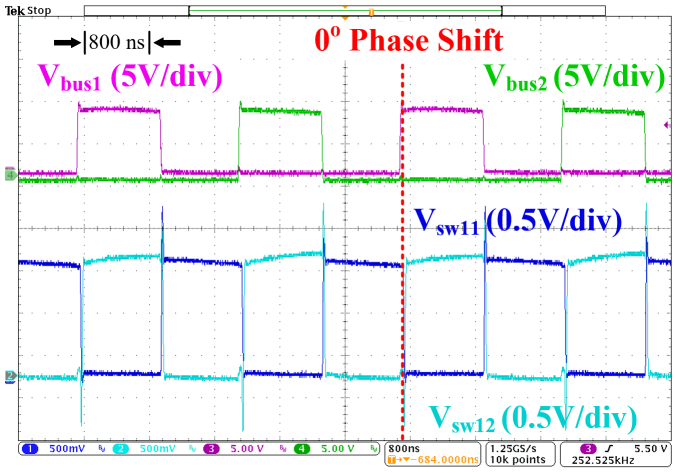

Fig. 12. Measured waveforms of the bus voltages and the switched node voltages in the back-end regulator. The control signal of the back-end is in phase with the control signal of the frond-end.

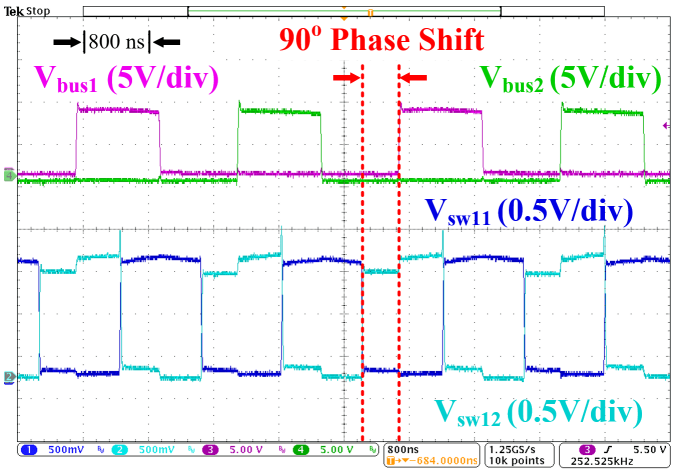

Fig. 13. Measured waveforms of the bus voltages and the switched node voltages in the back-end regulator. The control signal of the back-end has a 90° phase shift with the control signal of the front-end. This phase-shift result in a charge sharing voltage ripple at the switch node.

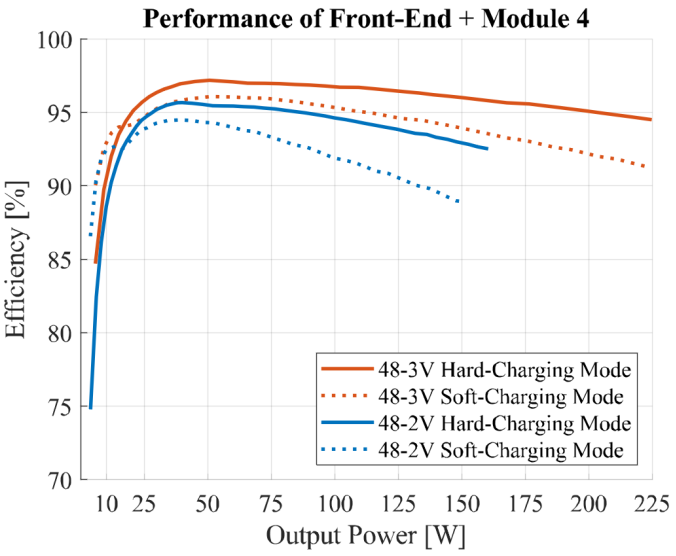

Fig. 14. Measured efficiency when only the input of Module 4 is connected to the stepped voltage rails. The gating losses are not included. With the fixed switching frequency of the front end, the hard-charging operation enables higher efficiency in heavy load, and the soft-charging operation enables higher efficiency in light load. Gating losses are not included.

Two 180° phase-shifted voltage buses are switching between 0-V and 8-V with 252.5 kHz frequency and 25% duty ratio, resulting in 2-V average bus voltage. The coupled inductors double the ripple current frequency of the voltage bus with 20-A peak-to-peak current ripples. Fig. 12 shows the waveforms of the switched node voltage in the back-end when the control signal of the back-end is in-phase with that of the front-end. Fig. 13 shows the waveforms of the switched node voltage in the back-end when the control signal of the back-end is 90° out-of-phase with that of the front-end. The in-phase operation leads to smaller voltage ripples but larger voltage pulses compared to the out-of-phase operation.

Fig. 14 shows the measured efficiency when only one module (Module 4) is connected to the stepped voltage rails. The measured efficiency is effectively the front-end efficiency when the converter operates as a 48-V to 2-V dc-dc converter with the 6-level switched-capacitor front-end and a coupled inductor at the output. The hard-charging mode offers higher efficiency in heavy load while the soft-charging mode performs better at light loads and enables smaller inductors and capacitors in the back-end switched-capacitor rectifiers. When excluding the gating loss, the peak efficiency of the front-end is 97.2% (@51-W) with $V_{out4} = 3$-V and is 95.6% (@40-W) with $V_{out4} = 2$-V in the hard-charging mode.

Fig. 15 shows the measured converter efficiency when the outputs of three identical modules – Module 1, Module 2 and Module 3 – are paralleled to drive the load. Their inputs are connected in parallel to two voltage buses. The duty ratio of the stepped voltage rails is set as 25%, effectively a 2-V average bus voltage (i.e., 0-V to 8-V stepped voltage with 25% duty ratio). The measured efficiencies under different

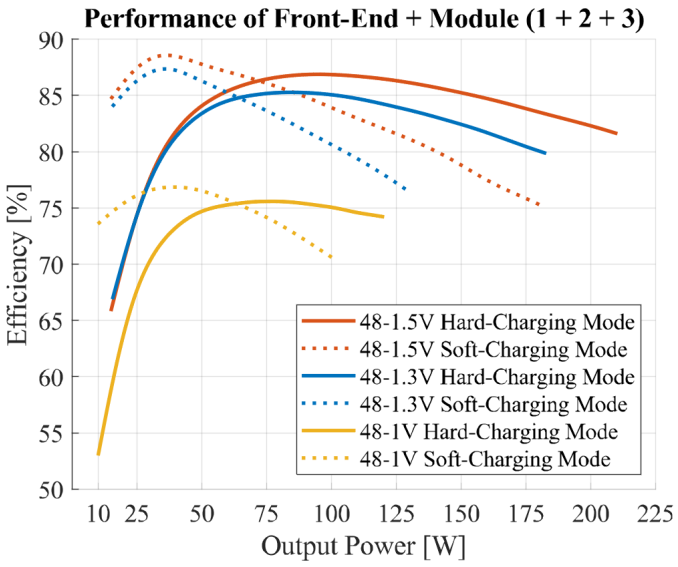

Fig. 15. Measured efficiency when the outputs of Module 1-3 are paralleled and their inputs are connected with the front-end. The average bus voltage is set as 2-V. Gating losses are not included.

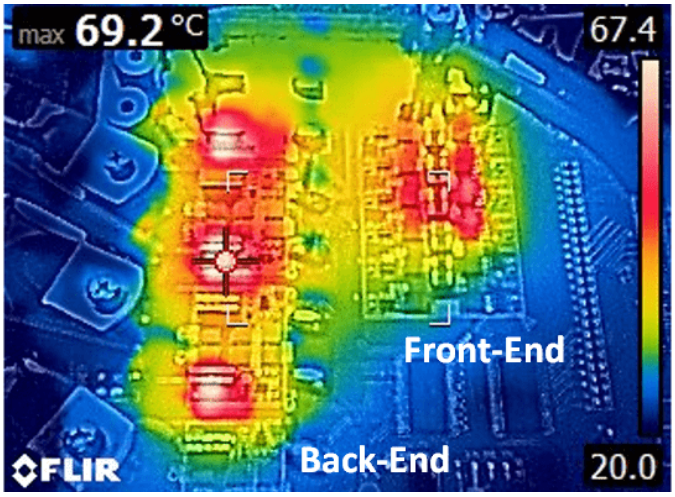

Fig. 16. Thermal image of the prototype converter operating at 48-V to 1.3-V/140A in the hard-charging mode under 72-ft^3/min air cooling from the bottom. Three back-end modules (Module 1+2+3) are connected in parallel.

output voltages (1.5-V, 1.3-V and 1-V) and different control methods (hard-charging and soft-charging modes) are also shown. When excluding the gate losses, the peak efficiency with 1.5-V output is 88.6% (@36-W) in the soft-charging mode. The peak efficiencies with 1.3-V and 1-V output are 87.3% (@36.4-W) and 76.8% (@39-W) in the soft-charging mode, respectively. Fig. 16 shows the thermal image when the prototype is delivering 140-A to a 1.3-V electronic load in the hard-charging operating mode.

V. Conclusions

This paper presents an inductor-linked single-input multi-output hybrid switched-capacitor power architecture with modular output cells for 48-V to PoL chiplet power delivery. The unique inductor-linked configuration of switched-capacitor circuits enables high performance with a high voltage conversion ratio while achieving high efficiency and high power density. The architecture is highly reconfigurable and can be used to support multiple loads in a chiplet with many voltage rails.

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