Vertical Stacked LEGO-PoL CPU Voltage Regulator

Jaeil Baek, *Member, IEEE*, Youssef Elasser, *Student Member, IEEE*, Kaladhar Radhakrishnan, *Senior Member, IEEE*, Houle Gan, *Senior Member, IEEE*, Jonathan Douglas, Harish K. Krishnamurthy, *Senior Member, IEEE*, Xin Li, *Member, IEEE*, Shuai Jiang, *Member, IEEE*, Charles R. Sullivan, *Fellow, IEEE*, and Minjie Chen, *Senior Member, IEEE*

***Abstract*—This paper presents a 48 V–1 V merged-two-stage hybrid-switched-capacitor converter with a *Linear Extendable Group Operated Point-of-Load* (LEGO-PoL) architecture for ultra-high-current microprocessors, featuring 3-D stacked packaging and coupled inductors for miniaturized size, fast speed, and vertical power delivery. The architecture is highly modular and scalable. The switched-capacitor circuits are connected in series on the input side to split the high input voltage into multiple stacked voltage domains. The multiphase buck circuits are connected in parallel to distribute the high output current into multiple parallel current paths. It leverages the advantages of switched-capacitor circuits and multiphase buck circuits to achieve soft charging, current sharing, and voltage balancing. The inductors of the multiphase buck converters are used as current sources to soft-charge and soft-switch the switched-capacitor circuits, and the switched-capacitor circuits are utilized to ensure current sharing among the multiphase buck circuits. A 780 A vertical stacked CPU voltage regulator with a peak efficiency of 91.1% and a full load efficiency of 79.2% at an output voltage of 1 V with liquid cooling is built and tested. The switched capacitor circuits operate at 286 kHz and the buck circuits operate at 1 MHz. It regulates output voltage between 0.8 V and 1.5 V through the entire 780 A current range. This is the first demonstration of a 48 V–1 V CPU voltage regulator to achieve over 1 A/mm^2 current density and the first to achieve 1,000 W/in^3 power density.**

***Index Terms*—Dc-dc power conversion, hybrid switched-capacitor circuit, voltage regulator, series-input-parallel-output architecture, vertical power delivery, coupled inductor**

I. Introduction

This paper is a combination and extension of five previously published conference papers, "LEGO-PoL: A 93.1% 54V-1.5V 300A Merged-Two-Stage Hybrid Converter with a Linear Extendable Group Operated Point-of-Load (LEGO-PoL) Architecture" in IEEE COMPEL 2019 [1], "LEGO-PoL: A 48V-1.5V 300A Merged-Two-Stage Hybrid Converter for Ultra-High-Current Microprocessor" in IEEE APEC 2020 [2], "A Merged-Two-Stage LEGO-PoL Converter with Coupled Inductors for Vertical Power Delivery" in IEEE ECCE 2020 [3], "3D LEGO-PoL: A 93.3% Efficient 48V-1.5V 450A Merged-Two-Stage Hybrid Switched-Capacitor Converter with 3D Vertical Coupled Inductors" in IEEE APEC 2021 [4], and "Vertical Stacked 48V-1V LEGO-PoL CPU Voltage Regulator with 1A/mm^2 Current Density" in IEEE APEC 2022 [5]. This work was jointly supported by Google LLC and Intel Corporation. *(Corresponding Author: Minjie Chen.)*

J. Baek, Y. Elasser, M. Chen are with the Department of Electrical and Computer Engineering and the Andlinger Center for Energy and the Environment at Princeton University, Princeton, NJ, 08540, USA (e-mail: jaeilb, yelasser, minjie@princeton.edu).

K. Radhakrishnan, J. Douglas are with Intel, Chandler, AZ, 85226, USA (e-mail: kaladhar.radhakrishnan, jonathan.p.douglas@intel.com).

H. K. Krishnamurthy is with Intel, Hillsboro, OR, 97124, USA (e-mail: harish.k.krishnamurthy@intel.com).

H. Gan, X. Li, and S. Jiang are with Google, Mountain View, CA, 94043, USA (e-mail: houlegan, xinxli@google.com).

C. R. Sullivan is with Dartmouth College, Hanover, NH, 03755, USA (e-mail: charles.r.sullivan@dartmouth.edu).

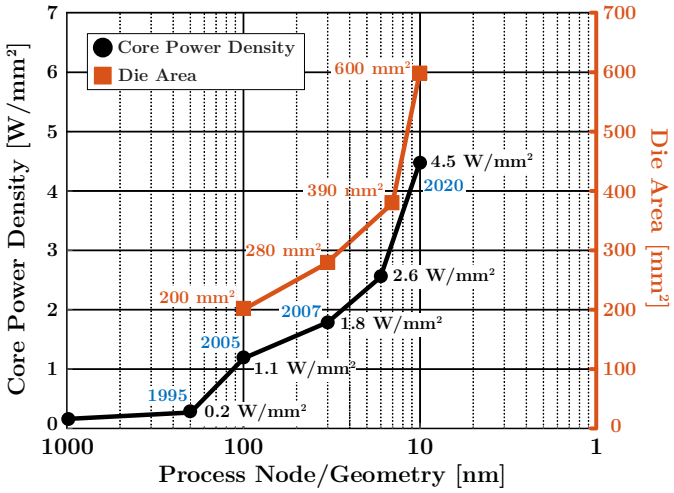


Fig. 1. The breakdown of Dennard scaling [6], [7]. Microprocessors consume higher power per square millimeter in an increasingly larger die area [8], [9], requiring very efficient and miniaturized power delivery from high voltage.

As the data center industry continues to trend towards consuming more power, efficient power delivery architecture is increasing in significance. Future high performance computing systems (CPUs, GPUs, and TPUs) comprise billions of transistors switching at very fast speeds, and consume hundreds of amperes of current at very low voltage (e.g. $\geq$250 A, $\leq$1.5 V) in a small footprint area [10], [11]. High-efficiency, high-power-density, high-bandwidth power electronics are needed to support high performance computing systems. Figure 1 shows the rapid growth of power consumption (= power area density $\times$ die area) of microprocessors against the development of the process nodes. The power area density of microprocessors has exceeded 4.5 W/mm^2, resulting in stringent requirements to improve the power density, and in particular, the current area density, of power electronics. Making the footprint area of voltage regulators smaller than the microprocessor can enable many system level opportunities.

Another emerging trend for efficient power delivery in data centers is powering servers from a high voltage (e.g. 48 V). Delivering power at 48 V reduces power distribution loss and improves UPS deployment flexibility [12]. Various topologies for 48 V-PoL applications have been proposed, including single-stage architectures [13]–[17] and two-stage architectures [18]–[25]. Single-stage architectures are attractive for their low component count, but they often have difficulty achieving high control bandwidth and high output current

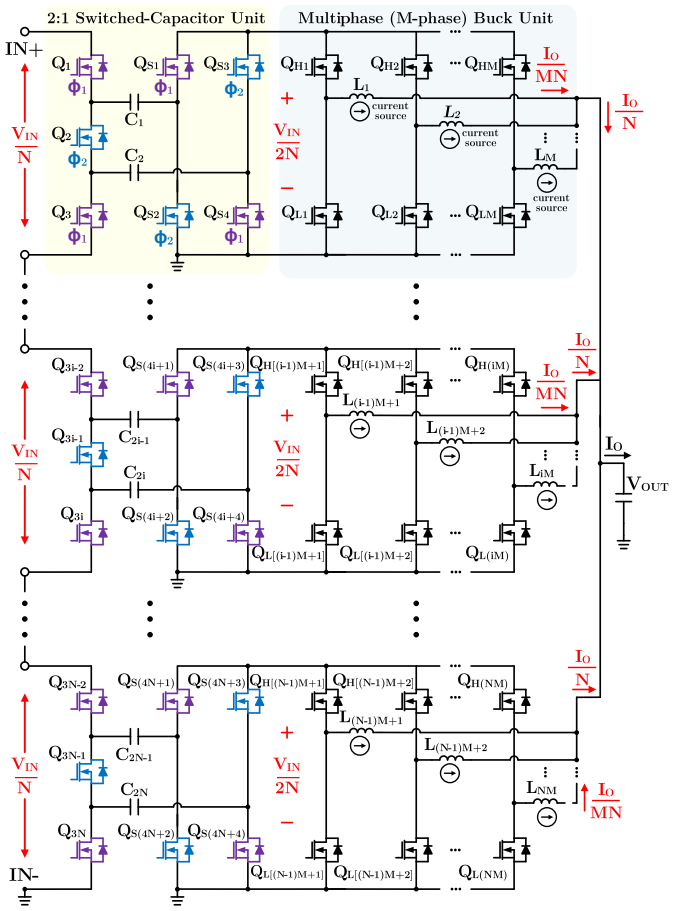


Fig. 2. N-submodules of the merged-two-stage LEGO-PoL architecture. One LEGO-PoL submodule comprises one 2:1 switched-capacitor unit and one M-phase buck unit. N submodules are connected with input in series and output in parallel. The LEGO-PoL architecture can be linearly extended for different input voltage and output current ranges.

capability. Two-stage architectures are more suitable for high output current and high control bandwidth applications. They typically consist of an unregulated stage and a regulation stage. The unregulated stage converts a high input voltage (e.g. 48 V) to a lower bus voltage (e.g., $\leq$ 12 V) with high efficiency. The regulation stage regulates the output voltage with a high control bandwidth. The unregulated stage can be a transformer based topology [18]–[20] or a switched-capacitor based topology [21]–[26]. Transformer based topologies can achieve high heavy-load efficiency but may have inferior light-load efficiency and power density due to transformers. Switched-capacitor based topologies are becoming increasingly popular due to their transformerless design. They offer advantages in reduced device voltage stress and current stress, and can provide soft charging and soft switching, but usually require resonant inductors to achieve high performance.

This paper develops a modular and scalable 48 V–1 V CPU voltage regulator solution – the *Linear Extendable Group Operated Point-of-Load* (LEGO-PoL) architecture – which can achieve extreme current area density and perform vertical power delivery. This architecture decouples the high voltage stress and high current stress with automatically balanced building blocks for modularity and scalability. It has a single magnetic component (the output inductor). The size of the dc decoupling capacitors between two stages is very small. The inductive energy storage per watt of the system is low. The switched-capacitor stage can operate at a low switching frequency (e.g. $\leq$ 300 kHz) to achieve high efficiency. The buck stage can operate at a much higher switching frequency (e.g. $\geq$ 1 MHz) to achieve a high control bandwidth. The coupled inductors further reduce the output inductor size with improved system performance in transient [27]–[34].

A 3D stacked 48 V–1 V CPU voltage regulator with vertical coupled inductors was fabricated and tested to deliver 780 A of output current with a 0.8 V–1.5 V regulated output voltage range. Vertically delivering the power enables the prototype to achieve a high current area density. The prototype achieved a peak efficiency of 91.1% and a full load efficiency of 79.2%, a current area density of 1.017 A/mm^2, and a power density of 1000 W/in^3 at 1 V, 780 A, and 1 MHz buck switching frequency. The system is liquid cooled when operating above 450 A. The semiconductor junction temperature is maintained below 95°C in all operating conditions.

The remainder of this paper is organized as follows: Section II introduces the principles of the LEGO-PoL architecture and its operation mechanisms, including soft charging, automatic current sharing, and automatic voltage balancing. Section III presents the design considerations of the 3D stacked 48 V–1 V point-of-load converter. The experimental setup and measurement results of the prototype are presented in Section IV. Section V includes discussion and details further improvements to achieve improved performance. Finally, Section VI concludes this paper. An extended discussion of the automatic current balancing mechanism is provided in the Appendix.

II. LEGO-PoL Architecture

A. Principles of the LEGO-PoL Architecture

Figure 2 shows the key principles of the merged-two-stage LEGO-PoL architecture with N submodules. One LEGO-PoL submodule comprises two building blocks: a 2:1 switched-capacitor unit and an M-phase buck unit. The 2:1 switched-capacitor unit operates with fixed complementary 50% duty cycles (ϕ_1 and ϕ_2). It is operated at a low frequency to reduce switching losses and achieve high efficiency. The buck unit makes use of interleaving operation at a higher switching frequency for high control bandwidth. There is no resonant inductor in the switched-capacitor unit and no large dc decoupling capacitor between the two stages. The two stages are functionally merged: the buck units act as current sources to soft-charge the switched capacitors.

The LEGO-PoL architecture is highly modular and scalable. The number of submodules can be extended to cover a wider operation range in both the voltage and current domains. With buck units as the output stage, the LEGO-PoL architecture can leverage state-of-the-art voltage-mode or current-mode control techniques that have been developed for voltage regulation modules (VRMs). The N series-connected 2:1 switched-capacitor units split the input voltage into N voltage domains. The N parallel-connected buck units divide the output current

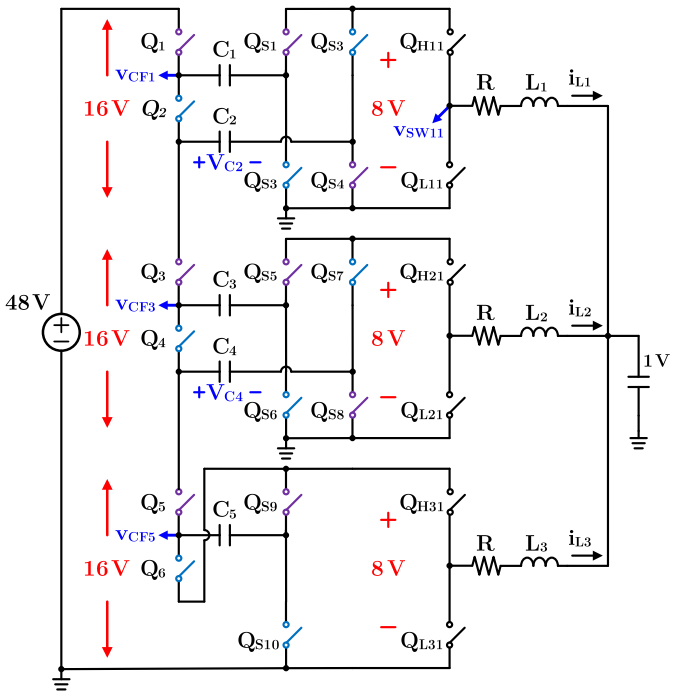


Fig. 3. Topology of a three submodule merged-two-stage LEGO-PoL converter with 48 V input voltage and 1 V output voltage for investigating the operation mechanisms. Single phase buck converters are used to simplify the analysis. The switches with purple color are controlled by a PWM signal ϕ_1, while the switches with blue color are controlled by a PWM signal ϕ_2.

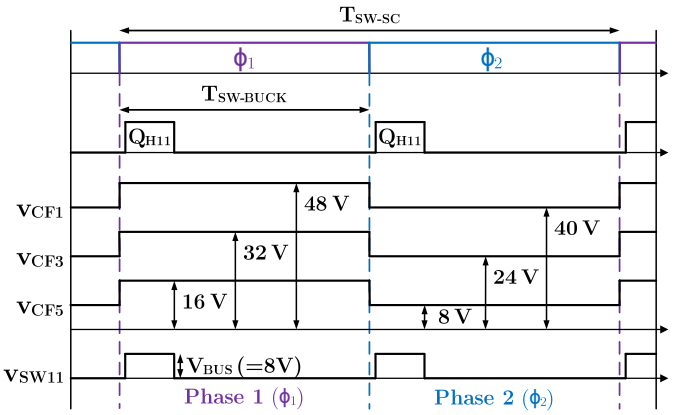


Fig. 4. Operational waveforms of the LEGO-PoL converter shown in Fig. 3.

into N current paths, and each individual phase of the buck units only delivers $\frac{1}{M\times N}$ of the output current. The virtual intermediate bus voltage is $\frac{1}{2N}$ of the input voltage $\left(\frac{V_{IN}}{2N}\right)$. By equally distributing high input voltage stress and high output current stress into each module, the architecture can utilize lower rated semiconductor devices with uniformly distributed heat dissipation across the submodules.

B. Operation Mechanisms of the LEGO-PoL Architecture

The LEGO-PoL architecture decouples the voltage stress, current stress, and dynamic requirements and addresses these design challenges. In this section, we present the soft switching, soft charging, current sharing, and voltage balancing mechanisms in detail. Figures 3 and 4 show a topology and operational waveforms of a LEGO-PoL converter comprising three (N = 3) 2:1 switched-capacitor units and three single-phase ($M = 1$) buck units to illustrate the operation mechanisms. The switched-capacitor units in Fig. 3 are simplified from Fig. 2. The series-connected switches in Fig. 2, such as Q_3 and Q_{3i-2}, can be merged as one switch, Q_3 in Fig. 3. One switch (Q_{3N}), one capacitor (C_{2N}), and two synchronous rectifier switches $\left(Q_{S(4N+3)}\right.$ and $\left.Q_{S(4N+4)}\right)$ in the third 2:1 switched-capacitor unit can be removed because the voltage across C_{2N} is zero. Switch Q_6 is connected to the output of the third 2:1 switched-capacitor unit.

1) Soft Switching and Soft Charging: The LEGO-PoL architecture leverages the merged-two-stage concept presented in [35]–[37]. There are two options for implementing merged-two-stage operations. The first is when the LEGO-PoL converter is designed with a very low parasitic inductance (e.g., $\ll$1 nH) along the current path between the switched-capacitor stage and the buck stage. In this option, the capacitors of the switched-capacitor stage are used as the input capacitors of the buck stage, and the decoupling capacitor between the two stages is eliminated. Buck inductor currents can only conduct through each switched-capacitor unit when the high-side buck switches (Q_{Hx}) are turned on. Zero-current-switching is achieved in the switched-capacitor units by coordinating the switching sequences of the switched-capacitor units and buck units. The key principle is to change the state of the switched-capacitor units during the free-wheeling state of the buck units (Fig. 4). The capacitors of the switched-capacitor units are always charged and discharged by the buck stage which acts as a current source.

The second possible design option is when the LEGO-PoL converter does not have a low enough parasitic inductance (e.g., >1 nH). In this option, a capacitor between two stages is used. This capacitor is large enough to filter the high frequency pulsating current from the buck stage, and is small enough to maintain low charge sharing loss. The current flowing in the switched-capacitor units is the input current of the buck units, filtered by the parasitic inductance and filter capacitance. This design option is implemented in the developed prototype, using the switching control demonstrated in Fig. 4. The design of this filter capacitor is discussed in Section III-B.

In contrast to the resonant hybrid-switched-capacitor converter, which achieves soft charging operation by placing an inductor between two capacitors, the LEGO-PoL architecture utilizes the inductors in the buck stage to achieve soft charging. The selection of the switching frequencies of the switched-capacitor units and buck units are not limited by resonant operation. In both LEGO-PoL design options, the two stages are merged. The large decoupling capacitor present in a traditional two stage architecture is either completely eliminated (option 1) or replaced with a small filter capacitance (option 2). The charge sharing loss can be maintained low in both options.

2) Automatic Current Sharing and Voltage Balancing: The automatic current sharing and voltage balancing mechanism of the LEGO-PoL architecture can be explained by analyzing the current flow in the two switching phases in Fig. 3. In each switching cycle, capacitors C_2 and C_4 are charged by

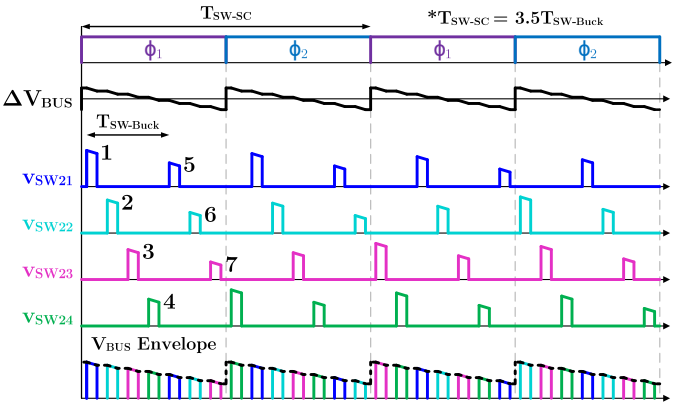


Fig. 5. An example of passive phase current balancing of the LEGO-PoL converter. Phase rotation enables each buck switch node to have the same average input voltage.

one current source in ϕ_1, and discharged by another current source in ϕ_2. Due to the charge balancing requirements of the switched capacitors, the two current sources have to be equal, leading to current sharing between two adjacent modules, and sequentially current sharing to all modules. For example, C_2 is discharged by i_{L_2} in ϕ_1, and charged by i_{L_1} in ϕ_2. C_3 is charged by i_{L_2} in ϕ_1, and discharged by i_{L_2} in ϕ_2. As described in Appendix I, the charge balance requirement of C_2 and C_3 in one switching period forces i_{L_1} to be equal to i_{L_2} in steady state operation. Benefiting from a similar switched-capacitor mechanism, the automatic current sharing leads to automatic voltage balancing between the series stacked switched capacitors. With these features, the LEGO-PoL architecture can handle a very high output current.

3) Passive Phase Current Balancing: The LEGO-PoL architecture automatically balances the current between each submodule. The phase currents of each module can be balanced by coordinating the selection of the switching frequencies of the switched-capacitor stage and buck stage. Since the LEGO-PoL architecture removes large dc decoupling capacitor between the two stages, the virtual intermediate bus voltages (V_{BUS}) contain a higher ripple, which may cause phase current mismatch in a buck unit. There are a few methods to balance the phase currents in the presence of this ripple, including current mode control. The duty ratios of the buck unit switches can be actively modulated to compensate for the input voltage ripple and balance phase currents. Another way is to use a passive phase rotating scheme to balance the current as depicted in Fig. 5. When the buck switching frequency is chosen as

$$f_{\text{Buck}} = \frac{2k+1}{2} f_{\text{SC}}, \quad k = 1, 2, 3, \cdots \tag{1}$$

where f_{Buck} and f_{SC} are the switching frequencies of the buck stage and switched-capacitor stage, respectively, an odd number (seven, in the example of Fig. 5) of buck switching occurrences happen during a half switching cycle of the switched-capacitor stage. This results in rotating through the different buck switches, each taking a turn as the one turned on at the highest V_{BUS} ripple, and resulting in identical average input voltage across all buck switch nodes.

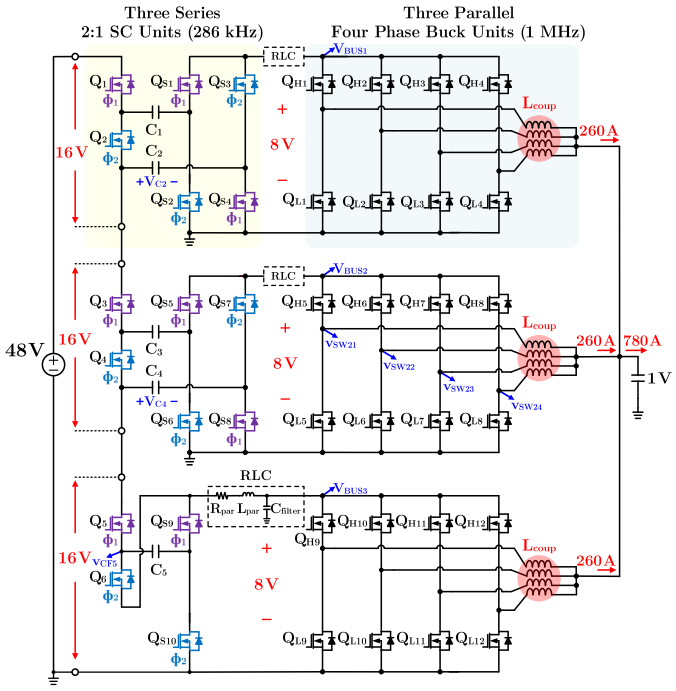


Fig. 6. A 48 V to 1 V, 780 A LEGO-PoL design with three ($N = 3$) stacked sub-modules. The switched-capacitor (SC) units switch at 286 kHz, and the four-phase ($M = 4$) buck units switch at 1 MHz. Each phase delivers 65 A of peak current at an effective current ripple frequency of 4 MHz due to interleaving and magnetic coupling. R_{par} and L_{par} are the lumped parasitic resistance and inductance of the current paths in the switched-capacitor stage. C_{filter} is a small high frequency filter capacitor of the buck stage.

III. Vertical Stacked LEGO-PoL Converter Design

Vertical power delivery for microprocessors can increase current area density (A/mm^2), create space for communication interconnects, reduce I^2R losses in the power delivery network, and improve transient response by reducing parasitic impedances [38]–[41]. This section details how to design a vertical stacked LEGO-PoL converter exceeding 1 A/mm^2, approaching the area power density of the silicon core (Fig. 1).

Figure 6 shows the schematic of a 48 V–1 V 780 A LEGO-PoL converter with three series-stacked 2:1 switched-capacitor units and three parallel-connected four-phase buck units with coupled inductors. This design steps down 48 V to 8 V through the three 2:1 switched-capacitor units, and then 8 V to 1 V through the four-phase buck units. The 8 V interconnect is a virtual intermediate bus with a significant voltage ripple. The twelve phases each deliver a peak current of 65 A with regulated output voltage. To enable vertical power delivery, the inductors are used as a link between the motherboard and the remainder of the converter. Parasitic resistance (R_{par}) and inductance (L_{par}) are considered to design a high frequency input filter capacitor (C_{filter}) for the buck stage. Detailed design considerations of this vertical stack converter for a high current density of 1 A/mm^2 are provided in the following subsections. Figure 7 and Figure 8 show the PCB layout and mechanical demonstration of the 48 V-1 V 780 A vertical stacked LEGO-PoL converter with lateral or vertical power delivery from the motherboard to the CPU.

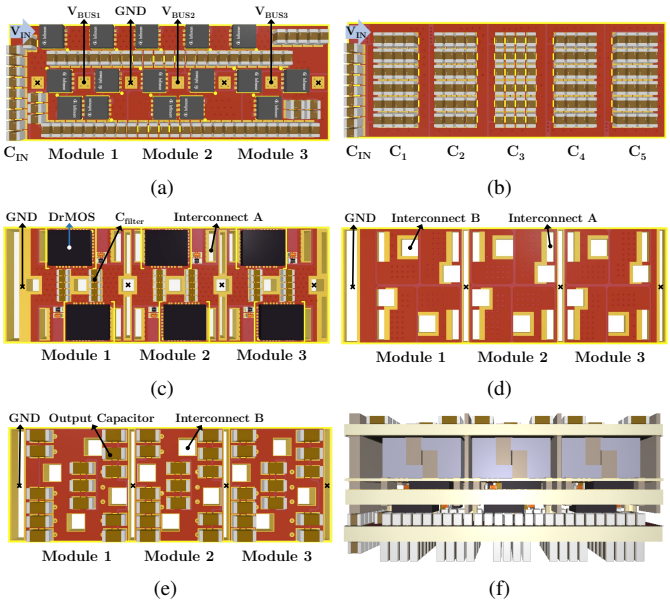


Fig. 7. PCB layout of the vertical stacked LEGO-PoL converter. PCB layout has a 780 mm^2 of area constraint to achieve 1 A/mm^2. (a) Switched-capacitor board, top view (12 layers, 2 oz, 2.2 mm). (b) Switched-capacitor board, bottom view. (c) Buck board (12 layers, 2 oz, 2.2 mm). The top and bottom views are identical. (d) Interposer board (4 layers, 2 oz, 0.8 mm). (e) Output motherboard (4 layers, 3 oz, 1.6 mm). (f) Full system assembly. Power is delivered from the bottom (48 V, 16.25 A side) to the top (1 V, 780 A side).

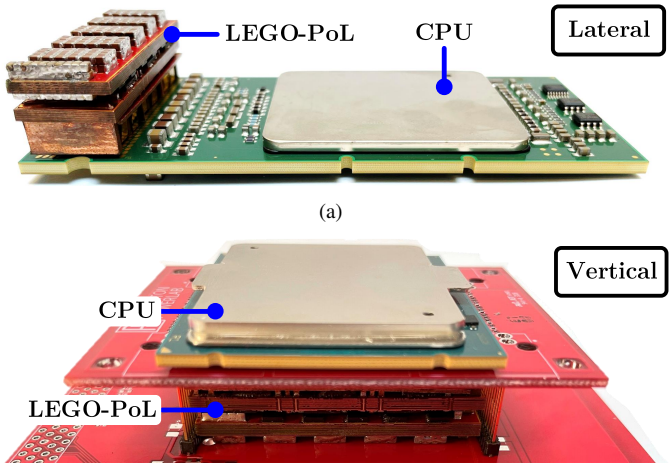


Fig. 8. Mechanical demonstration of the 48 V-1 V 780 A vertical stacked LEGO-PoL converter: (a) Lateral to an Intel Itanium 9150 CPU (TDP 104 W) and (b) Vertical to an Intel Xeon E7-2870 CPU (TDP 130 W).

A. Series-Stacked Switched-Capacitor Stage

Three series stacked 2:1 switched-capacitor units split 48 V high input voltage into smaller 16 V voltage domains to enable the utilization of low-voltage-rating devices with low on-resistance. The voltage stresses on the active switches are either V_{BUS} or $2V_{BUS}$, as the voltage blocked by the switches is always clamped by the capacitors. Due to low voltage stress and low switching frequency, switches in the switched-capacitor stage are implemented as standard MOSFETs.

In many resonant switched-capacitor designs, the capacitors need to be carefully selected because the capacitance value

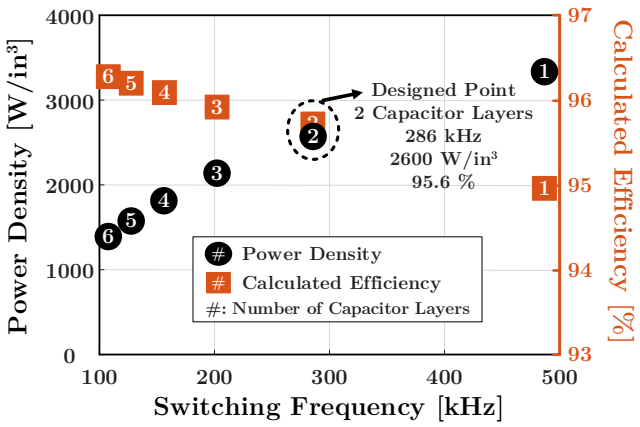


Fig. 9. Power density and calculated efficiency of the switched-capacitor stage according to the layers of bottom capacitors. The efficiency is obtained based on a developed loss model. The switching frequency is chosen to fix the maximum intermediate bus voltage ripple at 3 V when $V_{\text{out}} = 1$ V and $I_{\text{out}} = 780$ A in this graph.

determines the soft charging, soft switching, or resonant operation. Capacitance drifting and degradation may have a significant impact on the system performance. In the LEGO-PoL converter (Fig. 6), C_1–C_5 are flying capacitors and the capacitance values do not need to be precisely controlled. The system can tolerate capacitance variations that result from dc bias, temperature variation, and/or capacitance degradation.

Figures 7a and 7b show the component placement of the switched-capacitor stage within a printed circuit board (PCB) area of 780 mm^2. On the top layer, MOSFETs and capacitors are placed as close as possible to reduce parasitics. Then, the empty space is filled with copper traces and capacitors. On the bottom layer, the capacitors are fully modularized to optimize the current path and reduce the PCB conduction loss. The capacitance of the flying capacitors is selected to optimize the power density, efficiency, and intermediate bus voltage ripple. The bus voltage ripple can be designed considering the voltage rating of the semiconductor devices. Selecting a fixed 3 V intermediate bus voltage ripple for this application, more vertically stacked layers of capacitors enable lower switching frequency operation and higher efficiency but deteriorate the power density as depicted in Fig. 9. In the prototype, two layers of 0805 capacitors are stacked considering a switching frequency of 286 kHz, resulting in a switched-capacitor stage with 2600 W/in^3 power density and 95.6% full load efficiency. Figure 10 shows the gate drive structure for three series stacked 2:1 switched-capacitor units. A pair of 50% complementary gate driver signals (ϕ_1 and ϕ_2) is used. This is a simple and scalable charge pump circuit for generating the bias voltage for the floating MOSFETs and can be fully integrated.

B. Virtual Intermediate Bus Parasitics

Due to the high frequency operation of the buck stage, a small parasitic inductance between the two stages can cause current ringing and increase the stress on the devices in the switched-capacitor stage. Figure 11 shows an equivalent RLC circuit of one submodule of the LEGO-PoL converter. The

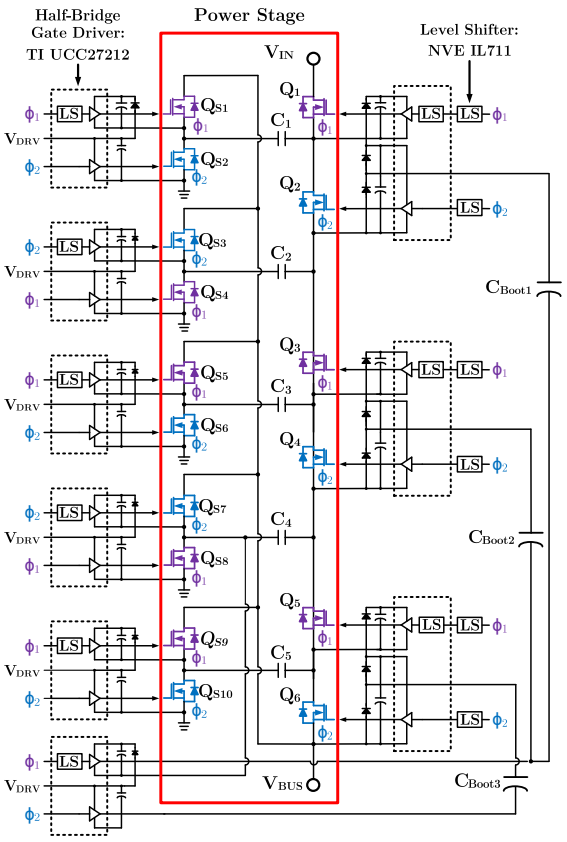


Fig. 10. A modular gate drive circuit for the switched-capacitor stage, which is placed on the switched-capacitor board, outside the power stage.

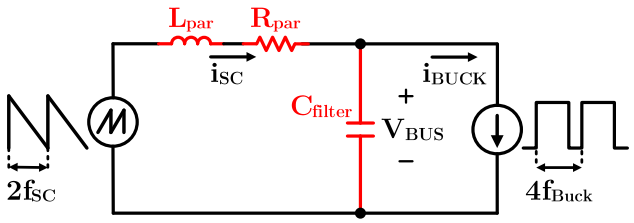


Fig. 11. Equivalent circuit of one submodule of the merged-two-stage LEGO-PoL converter. The 2:1 switched-capacitor unit is represented as a sawtooth voltage source with a frequency of 2 × f_{SC} and an amplitude equal to the ripple voltage of the switched-capacitor. The four-phase buck unit can be represented as a pulse wave current source with a frequency of 4 × f_{Buck}.

switched-capacitor stage is modeled as a sawtooth voltage source whose frequency is twice of that of the switched-capacitor stage ($2f_{SC}$). The buck unit is modeled as a pulse wave current source with 4 times the switching frequency of the buck stage ($4f_{Buck}$). L_{par} and R_{par} are the lumped parasitic inductance and resistance along the current paths in the switched-capacitor stage. C_{filter} is a small input capacitor of the buck stage to smooth the high frequency current. The input current of four-phase buck units (i_{Buck}) is clamped by the inductor current, while the current going through switched-capacitor units (i_{SC}) is determined by the RLC filter and has ringing. This issue commonly exists in merged-two-stage designs [35], [36].

L_{par} contributes to filtering and larger values are beneficial, but layouts that deliberately increase L_{par} often increase resistance and require extra space. Here L_{par} is determined by the practical value achieved in our assembly. R_{par} is minimized to improve efficiency, and thus C_{filter} is the only design parameter for the filter. The cutoff frequency of the RLC filter is

$$f_o = \frac{1}{2\pi\sqrt{L_{par}C_{filter}}}. \quad (2)$$

The switches of the switched-capacitor stage, interconnects between the switched-capacitor stage, and PCB trace are all sources of parasitic inductance and resistance. For the vertical stacked design introduced in Section III, the calculated parasitic inductance is 2.7 nH and parasitic resistance is 6.1 mΩ. The buck switching frequency f_{Buck} is 1 MHz.

Figure 12 shows a Bode plot of the magnitude response of the RLC filter, considering the buck switched current as the input and the current i_{SC} as the output. The response is plotted for various values of C_{filter}. A small filter capacitance of 0.5 μF amplifies the high frequency current, which can cause increased losses. As the filter capacitance increases, the

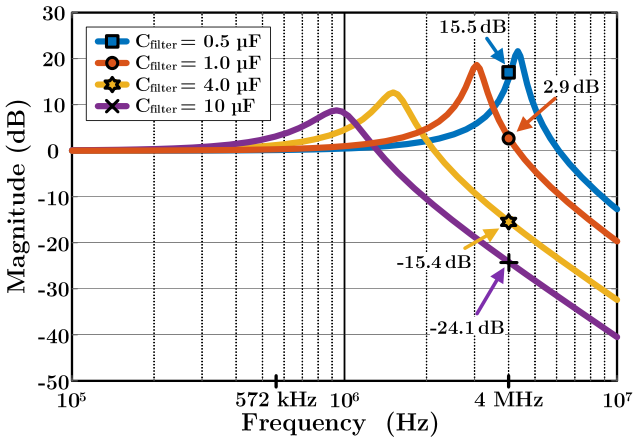


Fig. 12. Bode plot of the parasitic RLC filter magnitude response for various values of C_{filter}. For a buck switching frequency of 1 MHz, low values of C_{filter} result in an attenuation of the high frequency current ripple. A sufficiently high value of C_{filter} should be used to effectively filter the high frequency current.

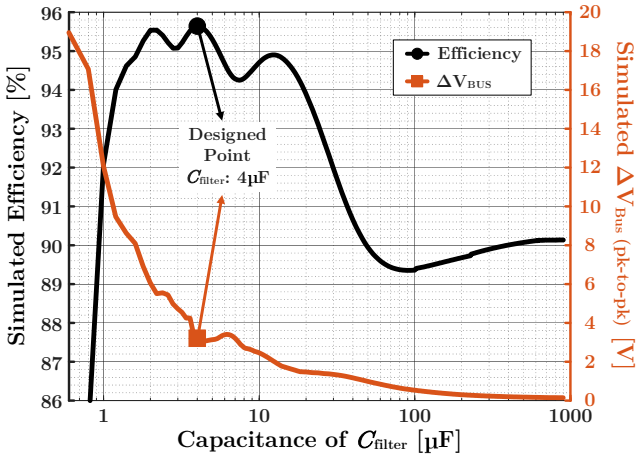


Fig. 13. Simulated efficiency of the switched-capacitor stage and intermediate bus ripple at 1 V and full load (780 A) as a function of the size of C_{filter}. The highest simulated efficiency is 95.6% with a filter capacitor of 4 μF and a voltage ripple of 3 V at f_{SC} = 286 kHz and f_{Buck} = 1 MHz.

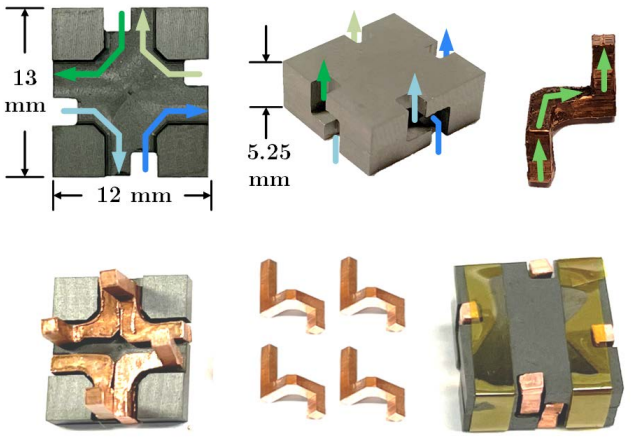


Fig. 14. Picture of the vertical four-phase coupled inductor magnetic core. Four machined copper windings make a 90° rotation within the core and deliver current from bottom to top. Cutouts in the core shorten the conduction path and facilitate the winding placement within the core.

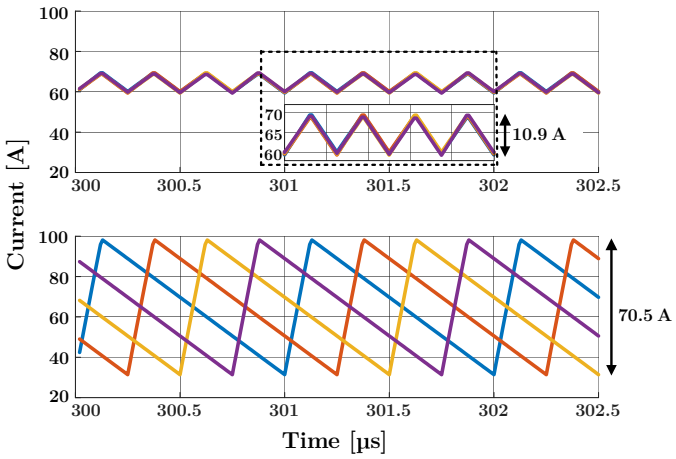


Fig. 15. Simulated waveforms of the multiphase buck converter with a coupled inductor (top) and four uncoupled inductors (bottom). The coupled inductor reduces the peak-to-peak phase current ripple from 70.5 A to 10.9 A while maintaining the same transient performance.

filter is able to adequately damp the current ringing. Figure 13 shows the simulated efficiency and intermediate bus voltage ripple of the LEGO-PoL design in Powersim. The simulated efficiency of the switched-capacitor stage at full load has multiple resonant peaks. When C_{filter} is large (in the range of hundreds of μF), the two stages are decoupled as in traditional two stage solutions, and the intermediate bus voltage ripple is low. However, a large value C_{filter} results in lower efficiency due to the large charge sharing loss, and results in lower power density due to the increased size of C_{filter}. In this design, C_{filter} is selected as 4.0 μF to achieve a high efficiency (95.6%) by taking advantage of low charge sharing loss.

C. Parallel Interleaved Buck Stage

Three parallel-connected four-phase buck units equally share 780 A of output current. Each individual phase delivers 65 A. The peak virtual intermediate bus voltage is 9.5 V (nominally 8 V, with a peak-to-peak voltage ripple of 3 V). The reduced stress enables the use of low voltage high

TABLE I
COMPARISON BETWEEN DISCRETE AND COUPLED INDUCTORS

Symbol	Parameter	Discrete	Coupled
V_{IN}	Buck Stage Input Voltage	8 V	
V_{OUT}	Output Voltage	1 V	
f_{Buck}	Switching Frequency	1 MHz	
L_ℓ	Phase Leakage Inductance	85 nH	12.4 nH
L_{tr}	System Transient Inductance	7.08 nH	1.03 nH
R_{dc}	Phase dc Resistance	0.39 mΩ	0.09 mΩ
P_c	System Core Loss	1.6 W	0.45 W
I_{sat}	Saturation Current	86 A	N/A
Δi_p	Phase Current Ripple	10.3 A	10.9 A
V	Total Volume	4.24 cm^3	2.45 cm^3

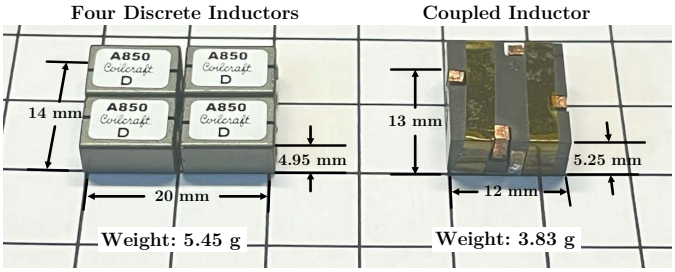


Fig. 16. Comparison of the coupled inductors with four discrete Coilcraft SLR1050A 85 nH discrete inductors. A comparison of the two solutions is presented in Table I. The coupled inductor enables a smaller leakage inductance and overall system transient inductance, lower dc resistance per phase, and lower core loss. The two options have similar phase current ripples. The volume of the three coupled inductors is only 57.7% of that of the twelve discrete inductors, with only 25% of the dc resistance.

current semiconductor devices and small magnetics. State-of-the-art control strategies for multiphase buck converters can be adopted. In a traditional 12-phase buck converter design, the controller needs to balance the current of all phases. Due to automatic current sharing, the controller only needs to balance the current of the four phases within each submodule. This unique feature allows the LEGO-PoL architecture to be scaled to a very high current without adding significant control complexity. This is a key advantage of LEGO-PoL compared to traditional two-stage intermediate bus architectures with numerous parallel units, which require active control for current balancing.

Figure 7c shows the component placement of the buck stage. Two 5 mm × 6 mm DrMOS devices are placed on the top and two are placed on the bottom. Each phase is designed to have the same PCB pattern from the input node to each of the coupled inductor interconnect nodes to minimize the current mismatch. Capacitors, as designed in Section III-B, are placed in the center of the board to filter the high frequency current.

Figure 7d shows the PCB layout of the interposer board. The interposer board decouples the design constraints of the buck board and the coupled inductor. Interconnect A is for the buck PCB connection, while interconnect B is for the coupled inductor. The interposer board is a 4 layer PCB; each layer is 2oz copper, and the overall board thickness is 0.8 mm.

D. Vertical Four-Phase Coupled Inductor

A coupled inductor can reduce the steady-state current ripple in each phase of the buck stage, and achieve fast dynamic performance with small leakage inductance [28]. In the 3D packaged prototype, three four-phase coupled inductors link the buck stage and output board with vertical windings. Figure 14 shows the coupled inductor, which is fabricated with Ferroxcube 3F4 MnZn ferrite. The footprint of the core is 13 mm $\times$ 12 mm, and its height is 5.25 mm. This design is optimized to minimize the core and winding losses at an operating point of 20 A per phase. The designed core has higher density and lower dc resistance than the design presented in [3]. To enable vertical power delivery, the machined copper windings enter from the bottom of the core, make a 90° rotation within the core, and exit from the top of the core to the output motherboard. The empty area within the core between windings can be adjusted to control the leakage flux path, which determines the transient and ripple performance [33]. An extended discussion about the coupled inductor design and optimization parameters is provided in [34].

Table I lists the key parameters of the four-phase buck units with the coupled inductors. The leakage inductance per phase is 12.4 nH, to achieve a targeted maximum output current slew rate of 5 A/ns. The overall system transient inductance is 1.03 nH, as there are 12 total phases amongst the three buck units. The peak-to-peak phase current ripple of the buck units is 10.9 A with the coupled inductor. To achieve the transient current speed using uncoupled discrete inductors, four 12.4 nH discrete inductors must be used. This would yield a 70.5 A peak-to-peak phase current ripple, as simulated in Fig. 15. This coupled inductor is designed to be able to handle a phase current mismatch of 10% of the full load current (65 A per phase) without saturation. If the phase currents are well balanced, the coupled inductor will not saturate.

Figure 16 compares the size of the coupled inductor against four Coilcraft SLR1050A 85 nH discrete inductors, which achieve a similar peak-to-peak phase current ripple as the coupled inductor. A more detailed comparison of the two solutions is presented in Table I. The coupled inductor achieves a much lower leakage inductance while maintaining a similar peak-to-peak phase current ripple as the discrete inductor solution. It also has a lower dc resistance and lower core loss. The volume of the coupled inductor is only 57.7% of that of the four discrete inductors.

E. Output Board and Output Capacitor Design

Figure 7e shows the PCB layout of the output board. The output board combines the current and hosts the output capacitors. Outside of the power stage area, terminal connections are placed to connect the converter to electronic loads. Each module has four terminals, labeled "interconnect B" for the four-phase coupled inductor. The remainder of the space is used for 14 $\times$ 1206 capacitors per module. In the prototype, 220 μF capacitors are used to satisfy a $\pm$2% output voltage ripple requirement. The effective total converter output capacitance is 5.75 mF at an output voltage of 1 V.

TABLE II
KEY COMPONENTS OF THE VERTICAL LEGO-POL PROTOTYPE

Symbol	Component
Q_1 & Q_6	Infineon BSZ010NE2LS5 (25 V, 212 A)
Q_2 – Q_5	Infineon BSZ0501NSI (30 V, 123 A)
Q_{S1} – Q_{S10}	Infineon BSZ010NE2LS5 (25 V, 212 A)
Q_H & Q_L	Infineon TDA21472 DrMOS (16 V, 70 A)
C_1 - C_5	TDK 4.7 μF, 0805 X7R (50 V)
C_{filter}	Kemet 0.22 μF, 0603 X7R (25 V)
Controller	Texas Instruments TMS320F28388D

Symbol	Bias Voltage	Number	Effective Size
C_1	40 V	59	47.2 μF
C_2	32 V	57	62.7 μF
C_3	24 V	58	82.0 μF
C_4	16 V	59	140 μF
C_5	8 V	68	257 μF
C_{filter}	8 V	24	4.0 μF

TABLE III
ESTIMATED PASSIVE COMPONENT SIZES OF A 6:1 RESONANT SWITCHED-CAPACITOR STAGE (BASED ON [22])

Passive Component	Value	Part Number
Resonant Inductors L_{R1}-L_{R3}	50 nH	Pulse PGL6189.500HLT
Resonant Capacitors C_{R1}-C_{R3}	5.6 μF	Kemet 0.47 μF, 1812, U2J (50 V)
Flying Capacitors C_{F1}-C_{F2}	120 μF	TDK 4.7 μF, 0805, X7R (50 V)
Bus Capacitors C_{BUS}	27 μF	Kemet 0.22 μF, 0603, X7R (25 V)

TABLE IV
PASSIVE COMPONENT VOLUME IN THE SWITCHED CAPACITOR STAGE OF A TWO-STAGE DESIGN AND A MERGED-TWO-STAGE DESIGN

Passive Components in the 6:1 Stage		Volume	Total
Two-Stage (Table III)	L_{R1}-L_{R3} & C_{R1}-C_{R3}	2.95 cm^3	3.62 cm^3
	C_{F1}-C_{F2}	0.50 cm^3	
	C_{BUS}	0.17 cm^3	
Merged-Two-Stage	C_1-C_5	0.94 cm^3	1.01 cm^3
	C_{filter}	0.07 cm^3	

Figure 7f shows the full 3D assembly drawing of the prototype. The switched-capacitor stage and the buck stage each occupy about one-half of the system volume. Power is vertically delivered from 48 V on the bottom to 1 V on the top. The overall height of the prototype is 16.65 mm.

IV. EXPERIMENTAL VERIFICATION

A 48 V to 1 V, 780 A vertical stacked LEGO-PoL converter was fabricated and tested. Figure 17 shows the 3D structure and assembly procedure of the prototype. The input voltage range is from 36 V to 54 V, and the output voltage range is from 0.8 V to 1.5 V. Three submodules were used, as per the schematic in Fig. 6. Table II lists the key power stage components of this design. The switches in the switched-capacitor units are implemented as MOSFETs. The switches in the multiphase buck units are implemented as low voltage DrMOS devices. The same type of capacitors was used for $C_1 - C_5$.

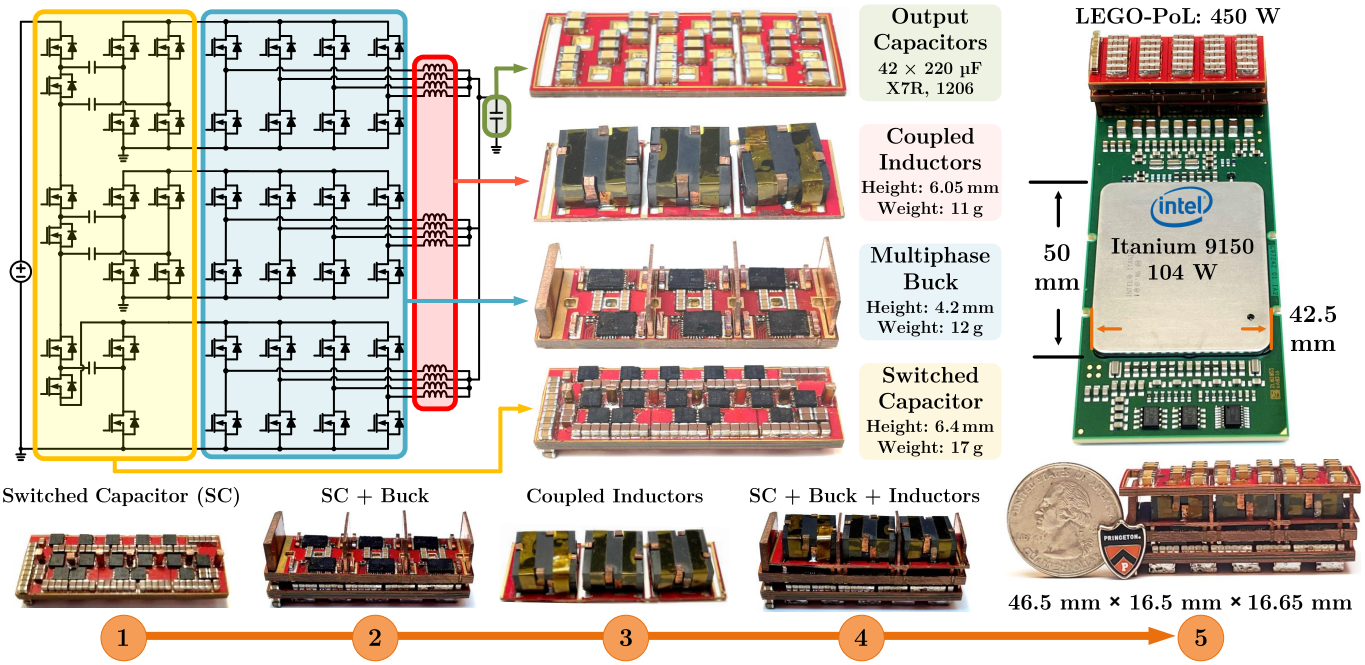


Fig. 17. Simplified schematic of the vertical stacked LEGO-PoL converter highlighting the switched-capacitor stage, buck stage, inductors, and output capacitors (left); assembly procedure of the vertical stacked LEGO-PoL converter (bottom); fully assembled converter next to a US Quarter and an Intel Itanium 9150 CPU. The power stage area of the prototype is 46.5 mm × 16.5 mm = 767.25 mm^2. The height of the prototype is 16.65 mm. The current density is 1.017 A/mm^2 at 780 A and the power density is 1000 W/in^3 at 1 V and 780 A with a maximum junction temperature of 94°C under liquid cooling.

Due to different bias voltages, the derated capacitance of each flying capacitor varies. For the filter capacitance, 24 × 0.22 μF 0603 size capacitors per module are used and the effective C_{filter} is 4.0 μF at 8 V bias voltage and 4 MHz frequency. Table III and Table IV show the estimated passive components of a 6:1 resonant-switched-capacitor stage (based on [22]) as well as a size comparison between the resonant-switched-capacitor design and the merged-two-stage switched-capacitor design. The merged two-stage LEGO-PoL design significantly reduces the passive component size and eliminates the need for resonant inductors in the switched-capacitor stage.

A. Experimental Setup

Figure 18 shows the experimental setup to characterize the performance of the vertical stacked LEGO-PoL converter. All of the necessary equipment is placed in a standard 1U server rack setup. Five Agilent 34401A digital multimeters are used to take automated measurements of the input voltage, input current, output voltage, output current, and DrMOS junction temperature. Rideon RSN-50 and Rideon RSC-1000 current shunts are used for input and output current measurement. A BK Precision 9117 dc power source and two electronic loads, a Chroma 63103A 240 A load and a Chroma 63203 600 A load, are used. The vertical stacked LEGO-PoL prototype was tested under two different cooling conditions: air cooling (Fig. 18b) and liquid cooling (Fig. 18c). Two 36 CFM fans are used for the air cooling. Mineral oil is used for the liquid cooling, and two 36 CFM fans and a pump are used to circulate the liquid at a speed of 9 L/min.

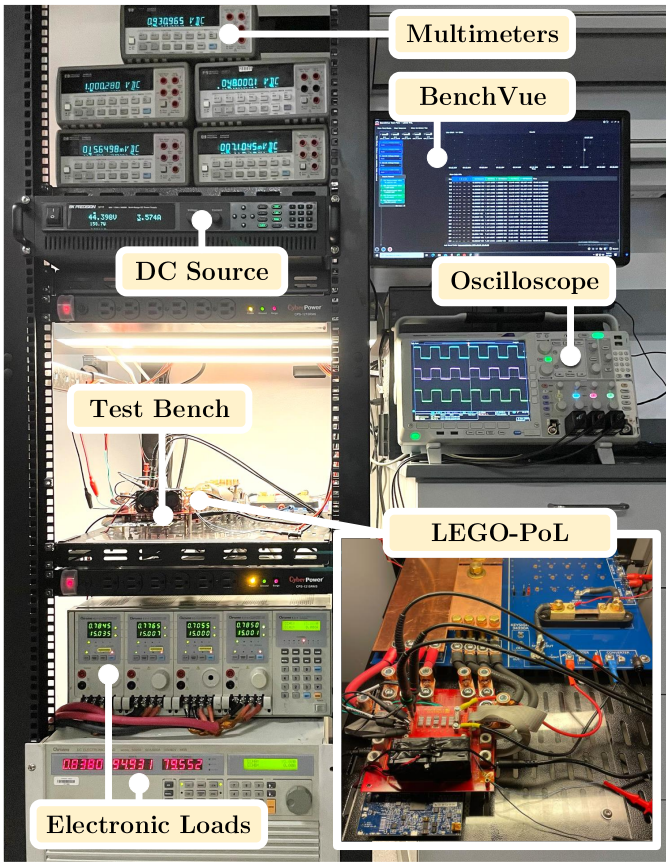
B. Operation and Performance

Figure 19 shows the measured waveforms of the switched-capacitor stage at a 48 V input voltage, 1 V output voltage, and an output current of 780 A. The input voltage is shown on top, and the differential voltage across C_2 and C_4, as well as the leftmost node voltage of C_5 (denoted $V_{C_{F5}}$ on the schematic of Fig. 6), are shown below the input voltage.

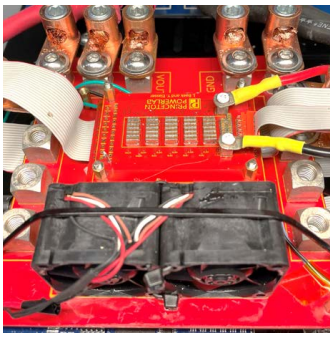
Figure 20 shows the waveforms of the intermediate bus voltages of each module at the same operating condition as above. The dc value of each of the three bus voltages is very close, further verifying the voltage balancing of the LEGO-PoL converter. Due to the different dc bias voltage of the flying capacitors (listed in Table II), each module has a different intermediate bus voltage ripple. Module #1 has the highest voltage ripple due to the higher bias voltage, and module #3 has the lowest voltage ripple.

Figure 21 shows the switch node voltages of each of the four phases of the second buck module. The envelope of the switch nodes is equal to V_{BUS2}, which is the input voltage of the buck unit. The four phases are interleaved, with a duty cycle of 15.7%. The switching frequency is 1 MHz.

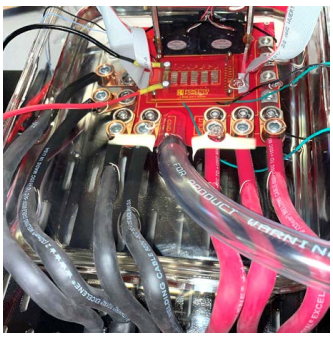
Figure 22 shows the output voltage and virtual intermediate bus voltage waveforms in response to a buck switch duty ratio change from 15% to 20% at an output load current of 150 A. The output voltage settles to within 2% of its expected value in 16.3 μs. The virtual intermediate bus voltages remain stable, with increased ripple during the transition as the output capacitors are being charged to the new output voltage level. The switched-capacitor stage of the LEGO-PoL converter operates as a dc transformer like a traditional hybrid-switched-capacitor stage. Figure 23 shows the input and output voltage ripple



(a)



(b)



(c)

Fig. 18. (a) Picture of the experimental setup. Digital multimeters are used to take automated measurements via the BenchVue software. An interface PCB is used to connect the device under test to the DC power source and the electronic loads, as well as house the measurement shunts; (b) Zoomed in view of the test bench for air cooling operation; (c) Zoomed in view of the test bench for liquid cooling operation. The converter is placed in a container filled with mineral oil. A pump and two fans are used to circulate the oil.

waveforms at 48 V input and 1 V/780 A output. The steady state output voltage ripple is 18 mV with 5.75 mF output capacitance. The input capacitor voltage ripple is 400 mV.

Figure 24 shows a closed-loop transient test for a 50% load step. A classic voltage mode feedback PI controller is used for this experiment. The three virtual intermediate bus voltages and output voltage in response to an output current load step between 50 A and 450 A are measured. The merged-two-stage operation maintains stable intermediate bus voltage without a large decoupling capacitor, with expected ripple due

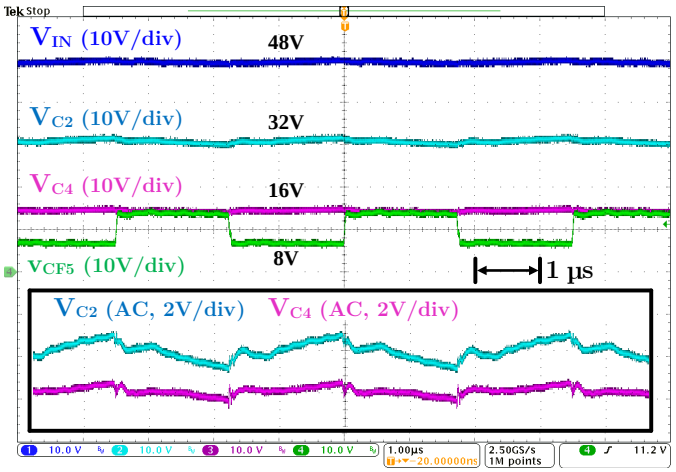


Fig. 19. Measured waveforms of the switched-capacitor stage at 48 V input, 1 V/780 A output. The series-stacked switched-capacitor modules evenly split 48 V input voltage into three 16 V voltage domains. C_2 has a higher voltage ripple than C_4 due to higher dc bias voltage.

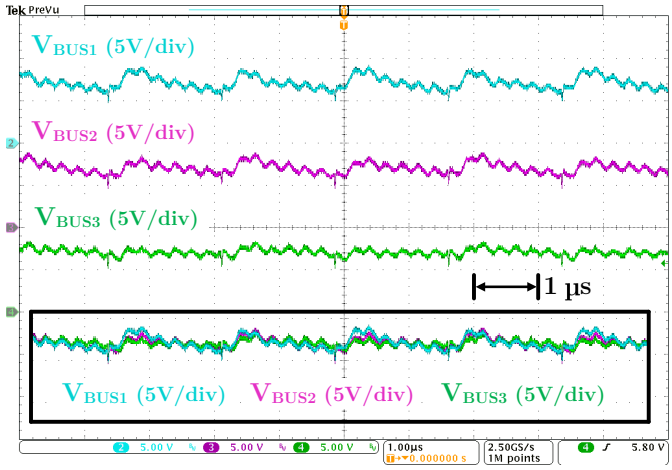


Fig. 20. Measured waveforms of three bus voltages at 48 V input, 1 V/780 A output. The three virtual intermediate bus voltages are automatically balanced.

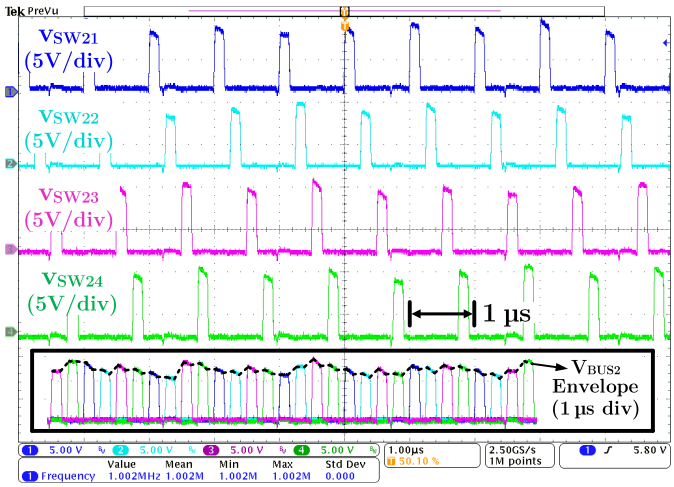


Fig. 21. Measured waveforms of switch nodes of a four-phase buck module at 48 V input, 1 V/780 A output. The four phases are interleaved. The envelope of the switch nodes is equal to the virtual intermediate bus voltage.

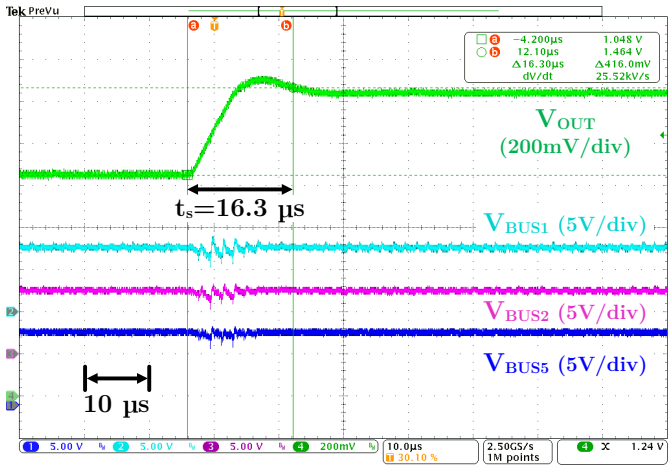


Fig. 22. Measured transient waveforms with an open-loop buck duty ratio step from 15% to 20% at 150 A. The output voltage steps from 1.048 V to 1.464 V within 16.3 μs.

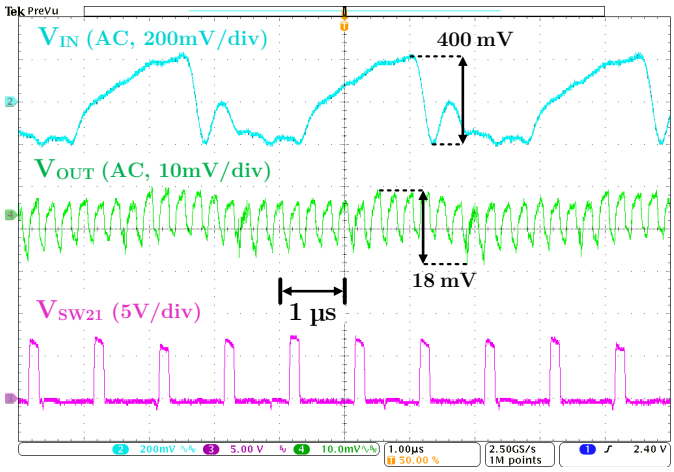
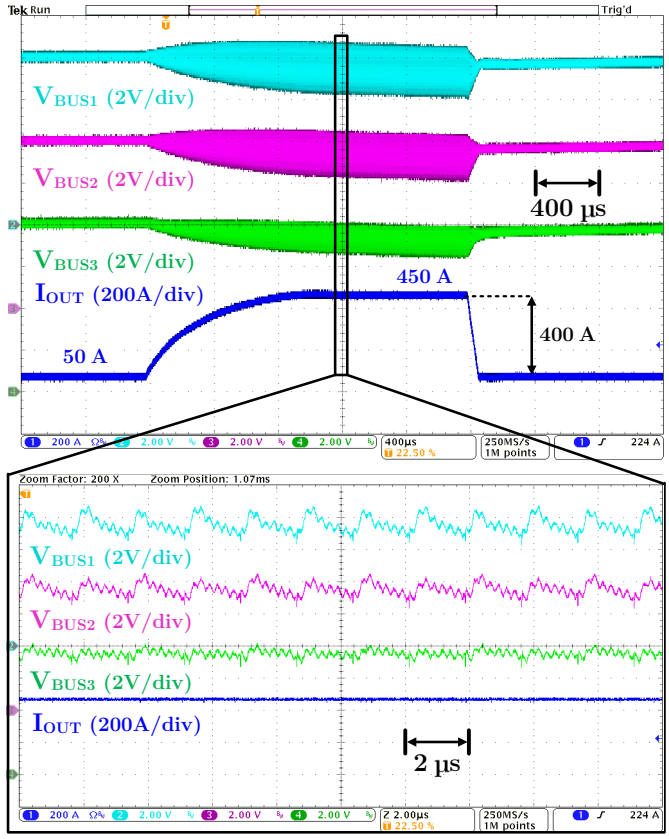


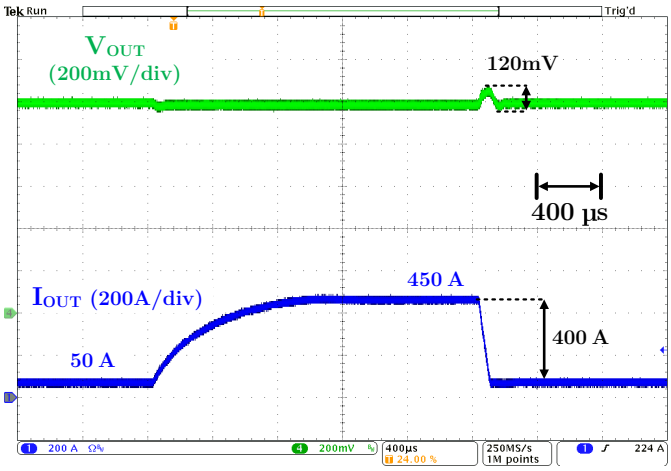
Fig. 23. Measured voltage ripples at 48 V input, 1 V/780 A output.

to the increase in output load current. Due to the limited controller bandwidth, a 120 mV peak-to-peak voltage excursion is observed during the transient. Advanced control methods, such as current mode control, can significantly improve the transient performance. Demonstrating the extreme transient performance of the converter is beyond the scope of this paper.

Figure 25 and 26 summarize the system efficiency of the LEGO-PoL converter with air cooling and liquid cooling. Measurements were taken at four different output voltage conditions: 0.8 V, 1.0 V, 1.2 V, and 1.5 V. The input and output voltages were measured right at the input and output capacitors. Due to the voltage drop between the output of the converter and the electronic loads, the measurement data for the 0.8 V output voltage condition stops at 660 A. The data for the other three conditions are provided across the full operating range in 10 A intervals. The switched-capacitor switching frequency is 286 kHz and the buck switching frequency is 1 MHz. The converter can achieve a 93.2% peak efficiency at $V_{\text{out}} = 1.5$ V and $I_{\text{out}} = 130$ A, and a 91.1% peak efficiency at $V_{\text{out}} = 1.0$ V and $I_{\text{out}} = 160$ A. At 780 A, the efficiency of the converter at $V_{\text{out}} = 1.5$ V is 79.6% and 79.2% at $V_{\text{out}} = 1.0$ V.



(a)



(b)

Fig. 24. Measured transient waveforms with a load current step between 50 A and 450 A (50% load step). (a) Three intermediate bus voltages. (b) Output voltage. A classic voltage-mode digital PI feedback loop was implemented in a microcontroller (TMS320F28388D) for this test. The total output capacitance is 5.75 mF. Demonstrating extreme transient performance of the LEGO-PoL architecture is beyond the scope of this paper.

The maximum power rating of the converter in air cooling is 450 A with the DrMOS junction temperature below 100°C. The gate drive loss of the prototype is estimated as 5.02 W (switched-capacitor stage: 2.02 W, buck stage: 3 W).

A detailed theoretical loss breakdown is provided in Fig. 27 for 1.0 V and 1.5 V output voltage. The loss breakdown was performed with the experimental duty ratio of the buck stage

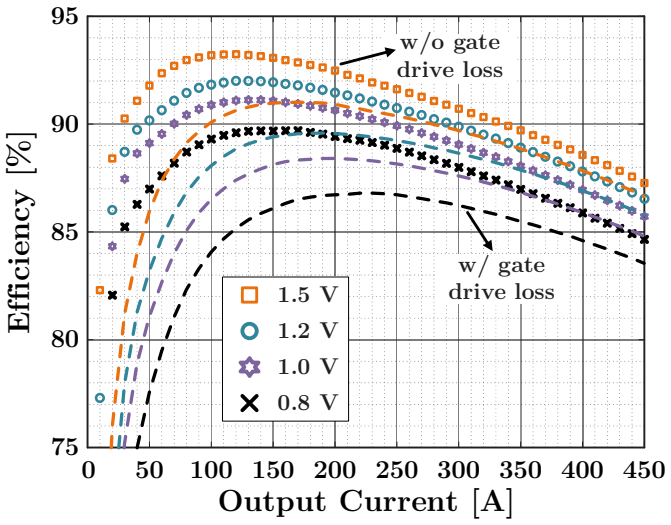


Fig. 25. Measured efficiency at 48 V input and different output voltages with air cooling and with and without gate drive loss. Two 36 CFM fans are used. The DrMOS junction temperature is kept below 100°C.

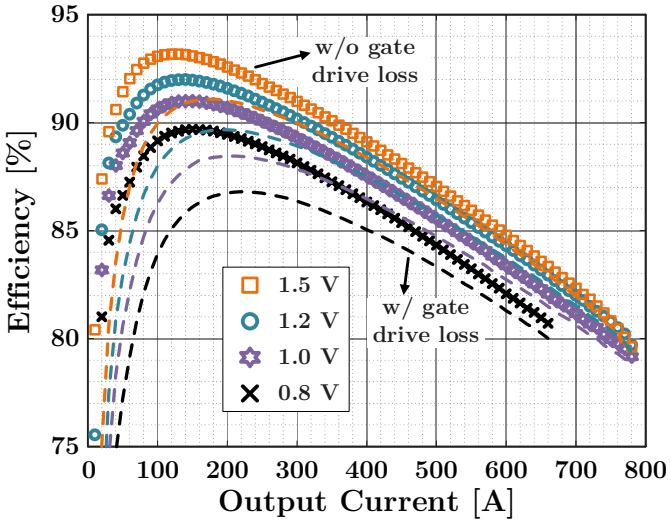


Fig. 26. Measured efficiency at 48 V input and different output voltages with liquid cooling and with and without gate drive loss. The converter is submerged in mineral oil, and a pump and two 36 CFM fans are used to circulate the liquid. The DrMOS junction temperature is kept below 100°C.

and junction temperature of DrMOS in Fig. 28b. Losses from the switched-capacitor stage include loss from the MOSFETs, the flying-capacitors, the filter capacitors, and the copper traces. Loss from the buck stage includes loss from the DrMOS, the coupled-inductor (both core loss and conduction loss), and the copper traces. The DrMOS switching and conduction loss dominates the loss of the overall system due to its high-switching-frequency operation and high output current. The switched-capacitor stage maintains high efficiency (above 95.5%) throughout the entire load range at 1 V output voltage condition. The overall system efficiency curve mirrors the shape of the buck efficiency curve, with a larger slope as the load current increases due to increased conduction loss. The converter achieves peak efficiency at around 20% full power, dominated by the efficiency curves of the buck stage.

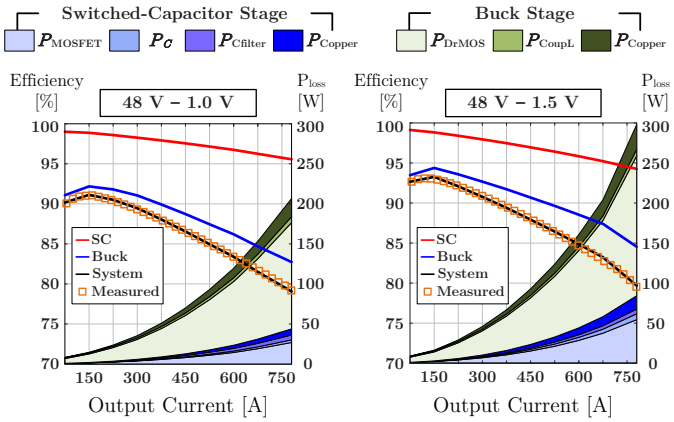
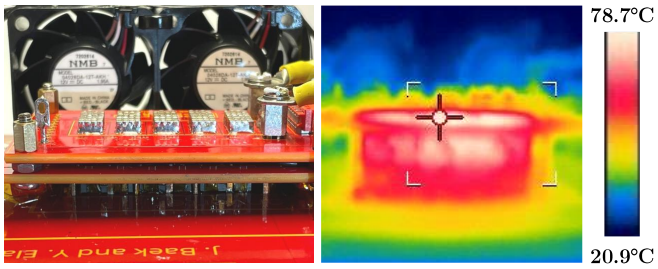
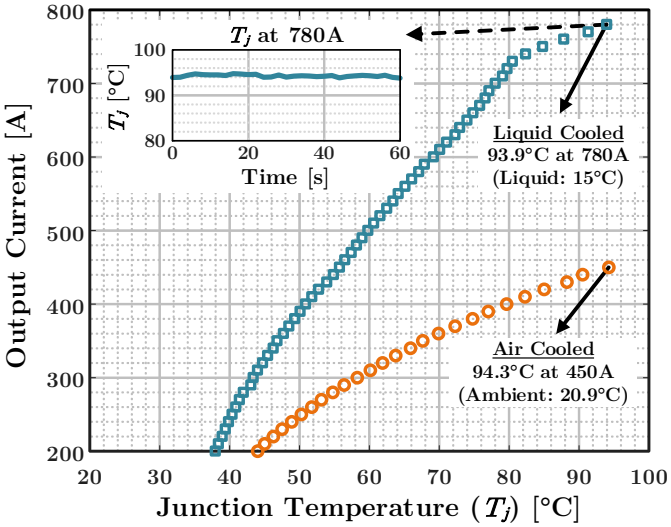


Fig. 27. Loss breakdown and calculated efficiencies of the switched-capacitor stage, buck stage, and total system at 1.0 V and 1.5 V output conditions. P_{MOSFET}, P_C, $P_{C\text{filter}}$, and P_{Copper} are the loss of MOSFETs, switched-capacitors, filter capacitors, and copper trace including connectors and PCB in the switched-capacitor stage. P_{DrMOS}, P_{CoupL}, and P_{Copper} are the loss of DrMOS, coupled inductors, and copper trace in the buck stage.



(a)



(b)

Fig. 28. (a) Thermal image of the vertical stacked LEGO-PoL converter. The thermal image was measured at 20.9°C ambient temperature with two 36 CFM fans. (b) Measured DrMOS junction temperature (from T_j sensing pin) with air cooling and liquid cooling. The junction temperature is stable at 780 A output current with liquid cooling.

With air cooling, the maximum output current of the system is 450 A. Figure 28a shows a thermal image of the converter at $V_{\text{out}} = 1.5$ V and $I_{\text{out}} = 450$ A. Two 36 CFM fans are used,

TABLE V
PERFORMANCE COMPARISON OF THE VERTICAL STACKED LEGO-POL AND OTHER 48 V TO 1 V POINT-OF-LOAD VOLTAGE REGULATOR DESIGNS

Year	Note	Output Current	Box Power Density‡	Current Area Density	Peak Efficiency	Full Load Efficiency	Switching Frequency◇	Energy Storage per Watt ($\frac{1}{2}LI^2/P$)	Including Gate Drive Loss or Size
This Work	Liquid Cooled	780 A	1000 W/in^3 510 W/in^3	1.017 A/mm^2 0.517 A/mm^2	91.1% 88.4%	79.2% 78.7%	1000 kHz	400 nJ/W	No Yes
	Air Cooled	450 A	577 W/in^3 294 W/in^3	0.587 A/mm^2 0.298 A/mm^2	91.1% 88.4%	85.7% 84.8%	1000 kHz	233 nJ/W	No Yes
2017	TI [42]	50 A	129 W/in^3	0.079 A/mm^2	90.7%	87.7%	600 kHz	3125 nJ/W	Yes
2019	MP-MIH [43]	40 A	83 W/in^3	0.044 A/mm^2	92.1%	80.4%	300 kHz	14667 nJ/W	No
2020	QSD-Buck [44]	40 A	31 W/in^3	0.024 A/mm^2	94.5%	91.1%	125 kHz	10000 nJ/W	Eff.: No Density: Yes
2020	MLB-PoL [45]	65 A	198 W/in^3	0.122 A/mm^2	91.5%	86.4%	250 kHz	9750 nJ/W	Yes
2020	Bel Power [46]	70 A	167 W/in^3	0.184 A/mm^2	91.6%	90.5%	242 kHz	N/A	Yes
2020	Sigma [16]	80 A	420 W/in^3	0.127 A/mm^2	94.0%	92.5%	600 kHz	N/A	Eff.: No Density: Yes
2020	TSAB [47]	90 A	36 W/in^3	0.023 A/mm^2	91.5%	85.0%	500 kHz	3713 nJ/W	Eff.: No Density: Yes
2020	Hybrid FCB† [26]	200 A	153 W/in^3	0.036 A/mm^2	91.4%	88.6%	205 kHz	3698 nJ/W	Eff.: No Density: Yes
2020	Vicor [48], [49]	214 A	400 W/in^3	0.202 A/mm^2	90.1%	N/A	1025 kHz	N/A	Yes
2021	On-Chip [50]	8 A	198 W/in^3	0.031 A/mm^2	90.2%	76%	2500 kHz	353 nJ/W	Yes
2021	ADI [51]	50 A	89 W/in^3	0.064 A/mm^2	90.8%	88.1%	350 kHz	4125 nJ/W	Yes
2021	24 V VIB [52]	450 A	325 W/in^3	0.219 A/mm^2	95.2%	89.1%	417 kHz	703 nJ/W	No

† The efficiency and power density of the Hybrid FCB design [26] are reported at an output voltage of 1.8 V.
‡ The power density is calculated with the box volume (defined as the maximum Length×Width×Height) of the prototype.
◇ The switching frequency of the voltage regulation stage.

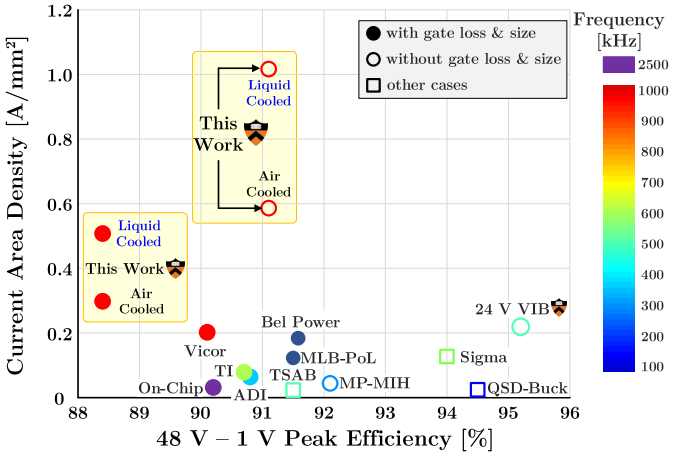


Fig. 29. Peak efficiency vs. current area density for the designs presented in Table V. Note these designs switch at different frequencies (color coded) and have different regulation capabilities. Data with gate driver loss & size are marked by filled circle and data without gate driver loss & size are marked by hollow circle. The LEGO-PoL converter switches at 1 MHz, among the highest in this comparison.

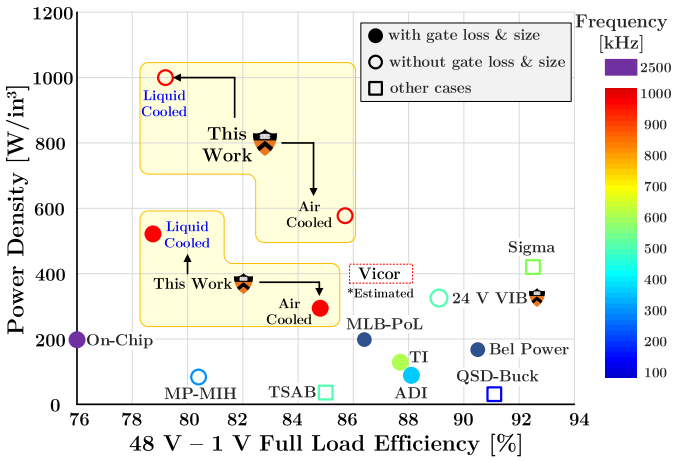


Fig. 30. Full load efficiency vs. power density for the designs presented in Table V. These designs switch at different frequencies and have different regulation capabilities. Data with gate driver loss & size are marked by filled circle and data without gate driver loss & size are marked by hollow circle. The LEGO-PoL converter switches at 1 MHz. The full load efficiency of the Vicor product is not available and is estimated.

and the PCBs reach a temperature of 78.7°C. Figure 28b shows a graph of the DrMOS junction temperature (using the built-in temperature sensing pin) for both the air cooled and liquid cooled operation at $V_{\text{out}} = 1.5$ V. The junction temperature reaches 94.3°C at $I_{\text{out}} = 450$ A. The junction temperature of the DrMOS reaches 93.9°C at $I_{\text{out}} = 780$ A in liquid cooling.

C. Performance Comparison

Table V is visualized in Fig. 29 and Fig. 30. The switching frequency is represented by a color gradient. This

work achieves the highest current area density while maintaining state-of-the-art peak efficiency, achieves the highest power density while maintaining high full-load efficiency, and switches at a high frequency of 1 MHz with interleaving.

Table V compares key metrics of the vertical stacked LEGO-PoL converter with other state-of-the-art 48 V-to-1 V point-of-load voltage regulator designs. The converter presented in this work achieves the highest reported output current capability at either 450 A with air cooling or 780 A with liquid cooling. This work achieves both the highest power density and the highest current area density, at 577 W/in^3 and 0.587 A/in^2 for air cooling and 1000 W/in^3 and 1.017 A/in^3 for liquid cooling. This is the first demonstration of a 48 V to 1 V point-of-load CPU voltage regulator to achieve over a 1 A/mm^2 current area density and the first to achieve 1,000 W/in^3 power density. This work achieves a peak efficiency of 91.1% and a full load efficiency of 85.7% with air cooling (79.2% with liquid cooling), which is comparable to other high-density designs. The switching frequency of the voltage regulation stage is 1 MHz, among the highest for a 48 V CPU voltage regulator demonstration. The coupled inductors enable the smallest transient inductance and lowest inductive energy storage per watt (defined as the total $\frac{1}{2}LI^2$ energy storage divided by the output power rating P, ignoring the current ripple) for this work when compared to other work.

V. Discussions and Further Improvements

The LEGO-PoL design presented in this paper combines many state-of-the-art technologies together to achieve extreme power density and efficiency. Some of its advantages come from the topology, architecture, and magnetics design, and other advantages come from the possibility of vertically packaging it together with the microprocessors to reduce the loss and parasitics in the interconnects, allowing more cores to be placed closer to each other with high speed communication. Both the silicon power density and server power density will continue to increase. Current area density (A/mm^2) and power density (W/in^3) are both important design targets.

The presented prototype achieves its peak efficiency at around 20% of its thermal design power (TDP). Depending on the applications, different microprocessors (e.g., CPUs, GPUs, XPUs) need performance optimized at different fractions of TDP, leading to different design tradeoffs. Different priorities among efficiency, density, and transient performance also lead to different tradeoffs. Challenges and pathways to achieving over 4.5 W/mm^2 area density – matching that of a state-of-the-art of the silicon core – while maintaining a high efficiency across the entire operation range, include:

1) The DrMOS devices we used limit current area density, efficiency, and switching frequency. Better low-voltage power devices, whether based on Si or wide-bandgap semiconductors, are expected to be instrumental in overcoming all three of these limitations.
2) The height of the LEGO-PoL prototype is limited by the vertical coupled inductors and capacitors. Switching at a higher frequency, enabled by better switches; optimizing the magnetics design with a priority on reducing thickness; and more advanced capacitor technologies can further reduce the height and weight of the system.
3) The current throughput of the prototype is limited by the thermal rating of the switches. Better cooling technology, and semiconductor devices that can work at higher temperatures (such as GaN devices), are promising techniques to improve the power density and improve the system efficiency at full load.
4) In the prototype, passive components (capacitors and magnetics) contribute an order of magnitude more volume and weight than the semiconductor devices. As shown in Fig. 31, semiconductor devices only contribute 4% of the system weight and 2% of the system volume. Devices that can efficiently switch at a higher frequency can further reduce the passive component sizes.
5) Printed circuit boards (PCBs) and copper interconnects occupy a large percentage of the system weight and volume. Advanced packaging techniques are needed to further reduce the size and improve the current density.

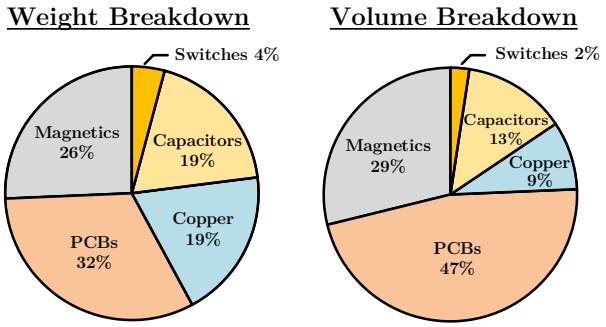


Fig. 31. Weight and volume breakdown of the LEGO-PoL prototype. The total weight of the prototype is 40 g, and the total component volume is 0.52 in^3. The switches only contribute to 4% of the weight and 2% of the volume; capacitors and magnetics each occupy about one quarter of the volume, and the PCBs and copper contribute about one-half of the weight and volume.

VI. Conclusion

This paper presents a vertical stacked 48 V to 1 V CPU voltage regulator with a linear-extendable group operated (LEGO) point-of-load architecture. By merging the operation of a switched-capacitor stage and a multiphase buck stage, the advantages of both can be leveraged while decoupling the design challenges of high efficiency, high density, and high control bandwidth. The system is highly modular and scalable. Vertical power delivery has the potential to reach the current area density of silicon microprocessors in future high performance computing. A 48 V to 1 V, 780 A CPU voltage regulator is built and tested with air cooling and liquid cooling, achieving a 91.1% peak efficiency, a 1000 W/in^3 power density, and a 1.017 A/mm^2 current area density.

Appendix I
Current Sharing and Voltage Balancing

A large signal average analysis is performed to illustrate the principle of the automatic current sharing and voltage balancing mechanisms. In the three submodule system depicted in

Fig. 3, assume the duty ratio of the buck converter, i.e., the duty ratio of high side switches, is D, L_x is connected with a series resistance R, the large-signal average current of L_x is i_x, the large-signal average voltage of C_y is v_{C_y}, where $x \in \{1,2,3\}$ and $y \in \{2,4\}$, the large-signal average models are:

$$\begin{aligned} L_1\frac{di_{L_1}}{dt} &= \langle v_{L_1}\rangle = \frac{1}{2}(V_{in}-v_{C_2})D - v_o - i_{L_1}R, \\ L_2\frac{di_{L_2}}{dt} &= \langle v_{L_2}\rangle = \frac{1}{2}(v_{C_2}-v_{C_4})D - v_o - i_{L_2}R, \\ L_3\frac{di_{L_3}}{dt} &= \langle v_{L_3}\rangle = \frac{1}{2}v_{C_4}D - v_o - i_{L_3}R. \end{aligned} \tag{3}$$

$$\begin{aligned} C_2\frac{dv_{C_2}}{dt} &= \langle i_{C_2}\rangle = \frac{1}{2}(Di_{L_1} - Di_{L_2}), \\ C_4\frac{dv_{C_4}}{dt} &= \langle i_{C_2}\rangle = \frac{1}{2}(Di_{L_2} - Di_{L_3}). \end{aligned} \tag{4}$$

Note v_{C_1}, v_{C_3}, and v_{C_5} are canceled out in (4). They do not impact the large-signal dynamics. The charge balance requirement of capacitor C_2 and C_4 leads to the automatic current sharing mechanism among L_1, L_2, and L_3. Assuming that $L_1 = L_2 = L_3 = L$ and $C_2 = C_4 = C$, the second-order differential equations for the current of the three submodule LEGO-PoL system can be obtained from (3):

$$\ddot{\mathbf{X}} + \frac{R}{L}\dot{\mathbf{X}} + \frac{D^2}{4LC}\boldsymbol{M}\mathbf{X} = 0,$$

$$\ddot{\mathbf{X}} = \begin{bmatrix} \frac{d^2 i_{L_1}}{dt^2} \\ \frac{d^2 i_{L_2}}{dt^2} \\ \frac{d^2 i_{L_3}}{dt^2} \end{bmatrix}, \ \dot{\mathbf{X}} = \begin{bmatrix} \frac{di_{L_1}}{dt} \\ \frac{di_{L_2}}{dt} \\ \frac{di_{L_3}}{dt} \end{bmatrix}, \ \mathbf{X} = \begin{bmatrix} i_{L_1} \\ i_{L_2} \\ i_{L_3} \end{bmatrix}, \tag{5}$$

$$\boldsymbol{M} = \begin{bmatrix} 1 & -1 & 0 \\ -1 & 2 & -1 \\ 0 & -1 & 1 \end{bmatrix},$$

$$\boldsymbol{Q}^{-1} = \frac{1}{6}\begin{bmatrix} 2 & 2 & 2 \\ -3 & 0 & 3 \\ 1 & -2 & 1 \end{bmatrix}, \ \boldsymbol{\Lambda} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 3 \end{bmatrix}.$$

Note $\boldsymbol{M}$ is a real symmetric matrix. $\boldsymbol{M}$ can be diagonalized as $\boldsymbol{M}=\boldsymbol{Q}\boldsymbol{\Lambda}\boldsymbol{Q}^{-1}$ where $\boldsymbol{Q}$ is a matrix composed of eigenvectors ($\boldsymbol{e_1}, \boldsymbol{e_2}$, and $\boldsymbol{e}_3$), and $\boldsymbol{\Lambda}$ is a diagonal matrix composed of eigenvalues (λ_1, λ_2, and λ_3) of $\boldsymbol{M}$. (5) can be rewritten as (6) by denoting $\boldsymbol{Y} = \boldsymbol{Q}^{-1}\mathbf{X}$:

$$\begin{aligned} \ddot{\mathbf{Y}} + \frac{R}{L}\dot{\mathbf{Y}} + \frac{D^2}{4LC}\boldsymbol{\Lambda}\mathbf{Y} &= 0, \\ \frac{d^2y_1}{dt^2} + \frac{R}{L}\frac{dy_1}{dt} + \frac{D^2}{4LC}(\lambda_1 y_1) &= 0, \\ \frac{d^2y_2}{dt^2} + \frac{R}{L}\frac{dy_2}{dt} + \frac{D^2}{4LC}(\lambda_2 y_2) &= 0, \\ \frac{d^2y_3}{dt^2} + \frac{R}{L}\frac{dy_3}{dt} + \frac{D^2}{4LC}(\lambda_3 y_3) &= 0. \end{aligned} \tag{6}$$

Since $i_{L_1} - i_{L_3}$ is linearly proportional to y_2, the second-order differential equation describing $i_{L_1} - i_{L_3}$ is:

$$\frac{d^2(i_{L_1}-i_{L_3})}{dt^2} + \frac{R}{L}\frac{d(i_{L_1}-i_{L_3})}{dt} + \frac{D^2}{4LC}(i_{L_1}-i_{L_3}) = 0. \tag{7}$$

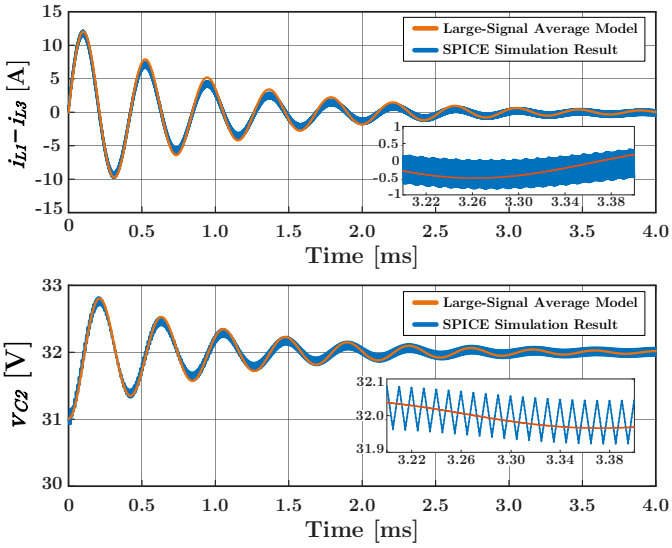


Fig. 32. Large-signal average model and SPICE simulated transient response of the automatic current sharing dynamics for the three submodule design in Fig. 3. The model was derived with $V_{in} = 48$ V, $D = 0.2$, $L_x = 1$ μH, $C_y = 45$ μF, and $R = 2$ mΩ. The initial condition of this simulation: $i_{L_1}(0) = i_{L_2}(0) = i_{L_3}(0) = 0$ A, $v_{C2}(0) = 31$ V, and $v_{C4}(0) = 15$ V. As described in (6), v_{C1}, v_{C3}, and v_{C5} have no impact on the transient dynamics. Their dc values are set by the switched capacitor mechanism due to the existence of the small C_{filter}.

This second-order differential equation describes the large-signal dynamics of the current difference between i_{L_1} and i_{L_3}. The natural frequency ω_n of this second order oscillation system is $\frac{D}{2\sqrt{LC}}$. The damping ratio ζ is $\frac{R}{D}\sqrt{\frac{C}{L}}$. The decay rate α is $\frac{R}{2L}$, the quality factor Q is $\frac{D}{2R}\sqrt{\frac{L}{C}}$. The current difference will respond to perturbations like a second-order system, and gradually decay to zero in periodic steady state. As i_{L_1} and i_{L_3} converge, based on (5), since y_3 is proportional to $i_{L1}-2i_{L2}+i_{L3}$, and y_3 damps to zero, all currents are equal in steady state. The current sharing mechanism of the LEGO-PoL converter is very similar to that of the series-capacitor buck converter [14]. As the current differences between inductors are zero, the average voltages of C_2 and C_4, v_{C_2} and v_{C_4}, reach $\frac{2V_{in}}{3}$ and $\frac{V_{in}}{3}$, respectively, because the average voltage across all switch nodes need to be equal. v_{C_1}, v_{C_3}, and v_{C_5} are set by the switched capacitor mechanism due to the small filtering capacitor C_{filter}. This guarantees automatic voltage balancing of the LEGO-PoL architecture.

Figure 32 compares the large-signal average model against SPICE simulation results. In periodic steady state, the large signal current $i_{L_1} = i_{L_3}$, and $\frac{di_{L_1}}{dt} = \frac{di_{L_3}}{dt} = 0$. This mechanism holds the large-signal average of v_{C_2} at $\frac{2}{3}V_{in}$ and the transient dynamics of the capacitor voltage follows a similar second-order transient dynamic (similar damping ratio and Q) as $i_{L_1} - i_{L_3}$ and gradually damps to $\frac{2}{3}V_{in}$ following the same oscillation. V_{C_2} will be automatically maintained at $\frac{2}{3}V_{in}$ in this example implementation.

This analysis can be extended and generalized for a LEGO-PoL converter with N submodules. Assuming that $L_1 = L_2 = \ldots = L_N = L$ with series resistance $R_1 = R_2 = \ldots = R_N = R$, $C_2 = C_4 = \ldots = C_{2(N-1)} = C$, and the duty ratio of all

buck units high side switches is D, the large-signal average model of the system is:

$$\ddot{\mathbf{X}} + \frac{R}{L}\dot{\mathbf{X}} + \frac{D^2}{4LC}\boldsymbol{M}\mathbf{X} = 0,$$

$$\ddot{\mathbf{X}} = \begin{bmatrix} \frac{d^2 i_{L_1}}{dt^2} \\ \frac{d^2 i_{L_2}}{dt^2} \\ \vdots \\ \frac{d^2 i_{L_N}}{dt^2} \end{bmatrix}, \ \dot{\mathbf{X}} = \begin{bmatrix} \frac{di_{L_1}}{dt} \\ \frac{di_{L_2}}{dt} \\ \vdots \\ \frac{di_{L_N}}{dt} \end{bmatrix}, \ \mathbf{X} = \begin{bmatrix} i_{L_1} \\ i_{L_2} \\ \vdots \\ i_{L_N} \end{bmatrix}, \tag{8}$$

$$\boldsymbol{M} = \begin{bmatrix} 1 & -1 & 0 & 0 & \cdots & 0 \\ -1 & 2 & -1 & 0 & \cdots & 0 \\ 0 & -1 & 2 & -1 & \cdots & 0 \\ \vdots & \vdots & \vdots & \ddots & \cdots & \vdots \\ 0 & 0 & \cdots & -1 & 2 & -1 \\ 0 & 0 & \cdots & 0 & -1 & 1 \end{bmatrix}.$$

$$\mathbf{X}^T \cdot \boldsymbol{M} \cdot \mathbf{X} = \sum_{k=1}^{N-1} \left(x_{k+1} - x_k\right)^2 \geq 0 \tag{9}$$

$\boldsymbol{M}$ is a $N \times N$ real symmetric matrix, so it can be diagonalized as $\boldsymbol{M} = \boldsymbol{Q}\boldsymbol{\Lambda}\boldsymbol{Q}^{-1}$, where $\boldsymbol{Q} = [\boldsymbol{e_1}, \boldsymbol{e_2}, \ldots, \boldsymbol{e_N}]$ and $\boldsymbol{\Lambda}$ is the diagonal matrix consisting of eigenvalues (λ_1, λ_2, $\ldots$, λ_N). For any non-zero $\mathbf{x} = [x_1, x_2, \ldots, x_N]^T$, $\boldsymbol{M}$ satisfies (9), so $\boldsymbol{M}$ is positive semidefinite, i.e. $\lambda_k \geq 0$, where $k \in \{1, 2, \ldots, N\}$. The rank of $\boldsymbol{M}$ is $N-1$, so there exists one and only one zero eigenvalue. Assuming $\lambda_1 = 0$, the corresponding eigenvector $\boldsymbol{e_1}$ is $[1, 1, \ldots, 1]^T$. Denoting $\boldsymbol{Y} = \boldsymbol{Q}^{-1}\mathbf{X}$, then (8) can be rewritten as (10) with explicit solutions:

$$\begin{cases} \frac{d^2 y_1}{dt^2} + \frac{R}{L}\frac{dy_1}{dt} = 0, \quad k = 1 \\ \frac{d^2 y_k}{dt^2} + \frac{R}{L}\frac{dy_k}{dt} + (\frac{D^2\lambda_k}{4LC})y_k = 0, \quad k = \{2, 3, \ldots, N\} \end{cases} \tag{10}$$

The general solutions for (10) are:

$$\begin{cases} y_1(t) = K_{11}e^{(-2\alpha t)} + K_{12}, \quad k = 1 \\ y_{k(k\geq 2)}(t) = K_{k1}e^{(-\alpha+\beta_k)t} + K_{k2}e^{(-\alpha-\beta_k)t}, \end{cases} \tag{11}$$

where K_1, K_2, K_{k1} and K_{k2} are constant coefficients, $\alpha = \frac{R}{2L}$, $\beta_k = \frac{1}{2}\sqrt{(\frac{R}{L})^2 - \frac{D^2\lambda_k}{LC}}$. There are three cases for the solution of $y_{k(k\geq 2)}(t)$: two different real roots, repeated roots, and complex roots. In all three cases, since α is positive, $y_1(t)$ damps to K_{12} and $y_{k(k\geq 2)}(t)$ damps to zero as $t \to \infty$. Therefore, in periodic steady state, the large signal inductor currents of the LEGO-PoL architecture with N submodules and total system output current I_O will settle to the same constant value $K_{12} = \frac{I_O}{N}$:

$$\begin{bmatrix} i_{L1} \\ i_{L2} \\ \vdots \\ i_{LN} \end{bmatrix} = \boldsymbol{QY} = [\boldsymbol{e_1}, \boldsymbol{e_2}, \ldots, \boldsymbol{e_N}] \begin{bmatrix} K_{12} \\ 0 \\ \vdots \\ 0 \end{bmatrix} = \begin{bmatrix} K_{12} \\ K_{12} \\ \vdots \\ K_{12} \end{bmatrix}. \tag{12}$$

Similarly, the average capacitor voltages V_{C_2}, $V_{C_4}, \ldots, V_{C_{2(N-1)}}$ damp to a balanced voltage:

$$\begin{bmatrix} V_{C_2} \\ V_{C_4} \\ \vdots \\ V_{C_{2(N-1)}} \end{bmatrix} = \frac{V_{in}}{N} \begin{bmatrix} N-1 \\ N-2 \\ \vdots \\ 1 \end{bmatrix}. \tag{13}$$

The voltages of other capacitors are then balanced by the switched capacitor mechanism due to the existence of C_{filter}. The charge balancing mechanism of the series capacitors guarantees automatic current sharing and automatic voltage balancing for the LEGO-PoL architecture with N submodules.

REFERENCES

[1] J. Baek, P. Wang, S. Jiang, and M. Chen, "LEGO-PoL: A 93.1% 54V-1.5V 300A Merged-Two-Stage Hybrid Converter with a Linear Extendable Group Operated Point-of-Load (LEGO-PoL) Architecture," *IEEE Workshop on Control and Modeling of Power Electronics (COMPEL)*, Toronto, Canada, 2019.

[2] J. Baek, P. Wang, Y. Elasser, Y. Chen, S. Jiang, and M. Chen, "LEGO-PoL: A 48V-1.5V 300A Merged-Two-Stage Hybrid Converter for Ultra-High-Current Microprocessors," *IEEE Applied Power Electronics Conference and Exposition (APEC)*, New Orleans, LA, USA, 2020.

[3] Y. Elasser, J. Baek, and M. Chen, "A Merged-Two-Stage LEGO-PoL Converter with Coupled Inductors for Vertical Power Delivery," *IEEE Energy Conversion Congress and Exposition*, Detroit, MI, USA, 2020.

[4] J. Baek, Y. Elasser, and M. Chen, "3D LEGO-PoL: A 93.3% Efficient 48V-1.5V 450A Merged-Two-Stage Hybrid Switched-Capacitor Converter with 3D Vertical Coupled Inductors," *IEEE Applied Power Electronics Conference and Exposition*, Phoenix, AZ, USA, 2021.

[5] Y. Elasser, J. Baek, K. Radhakrishnan, H. Gan, J. Douglas, H. K. Krishnamurthy, X. Li, S. Jiang, C. R. Sullivan, and M. Chen, "Vertical Stacked 48V-1V LEGO-PoL CPU Voltage Regulator with 1A/mm^2 Current Density," *IEEE Applied Power Electronics Conference and Exposition*, Houston, TX, USA, 2022.

[6] R. H. Dennard, F. H. Gaensslen, H. N. Yu, V. L. Rideout, E. Bassous, A. LeBlanc, "Design of Ion-Implanted MOSFET's with Very Small Physical Dimensions," *IEEE Journal of Solid-State Circuits*, vol. 9, no. 5, pp. 256–268, October 1974.

[7] S. Borkar and A. A. Chien, "The Future of Microprocessors," *Communications of the ACM.*, vol. 54, no. 5, pp. 67-77, May 2011.

[8] "Preventing Chips From Burning Up During Test," Semiconductor Engineering, 2021 [online]. https://semiengineering.com/preventing-chips-from-burning-up-during-test

[9] "GPU Die Size & Process Technology," PC Watch [online]. Available: https://pc.watch.impress.co.jp/img/pcw/docs/752/331/html/6.jpg.html

[10] A. Shehabi et al., "United States Data Center Energy Usage Report," Lawrence Berkeley National Laboratory, Berkeley, CA, *Tech.Rep.* LBNL-1005775, June, 2016. [online]. Available: https://eta-publications.lbl.gov/sites/default/files/lbnl-1005775_v2.pdf

[11] E. Strubell, A. Ganesh, and A. McCallum, "Energy and Policy Considerations for Modern Deep Learning Research," *Proceedings of the AAAI Conference on Artificial Intelligence*, vol. 34, no. 09, April 2020.

[12] X. Li and S. Jiang, "Google 48V Rack Adaptation and Onboard Power Technology Update," *Open Compute Project (OCP) Global Summit*, San Jose, CA, USA, 2019.

[13] K. Nishijima, K. Harada, T. Nakano, T. Nabeshima, and T. Sato, "Analysis of Double Step-Down Two-Phase Buck Converter for VRM," *International Telecommunications Conference (INTELEC)*, Berlin, Germany, 2005.

[14] P. S. Shenoy et al., "A 5 MHz, 12 V, 10 A, Monolithically Integrated Two-Phase Series Capacitor Buck Converter," *IEEE Applied Power Electronics Conference and Exposition (APEC)*, Long Beach, CA, USA, 2016.

[15] T. Xie, R. Das, G.-S. Seo, D. Maksimović, and H.-P. Le, "Multiphase Control for Robust and Complete Soft-charging Operation of Dual Inductor Hybrid Converter," *IEEE Applied Power Electronics Conference and Exposition (APEC)*, Anaheim, CA, USA, 2019.

[16] M. H. Ahmed, C. Fei, F. C. Lee, and Q. Li, "Single-Stage High-Efficiency 48/1 V Sigma Converter With Integrated Magnetics," *IEEE Trans. on Ind. Electronics*, vol. 67, no. 1, pp. 192-202, January 2020.

[17] G.-S. Seo, R. Das, and H.-P. Le, "Dual Inductor Hybrid Converter for Point-of-Load Voltage Regulator Modules," *IEEE Transactions on Industry Applications*, vol. 56, no. 1, pp. 367-377, Jan./Feb. 2020.

[18] C. Fei, M. H. Ahmed, F. C. Lee, and Q. Li, "Two-Stage 48 V-12 V/6 V-1.8 V Voltage Regulator Module With Dynamic Bus Voltage Control for Light-Load Efficiency Improvement," *IEEE Transactions on Power Electronics*, vol. 32, no. 7, pp. 5628-5636, July 2017.
[19] M. H. Ahmed, C. Fei, F. C. Lee, and Q. Li, "48-V Voltage Regulator Module With PCB Winding Matrix Transformer for Future Data Centers," *IEEE Trans. on Ind. Electron.*, vol.64, no.12, pp.9302-9310, Dec. 2017.
[20] Y. Cai, M. H. Ahmed, Q. Li, and F. C. Lee, "Optimal Design of Megahertz *LLC* Converter for 48-V Bus Converter Application," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 1, pp. 495-505, March 2020.
[21] Y. Li, X. Lyu, D. Cao, S. Jiang, and C. Nan, "A 98.55% Efficiency Switched-Tank Converter for Data Center Application," *IEEE Trans. on Industry Applications*, vol. 54, no. 6, pp. 6205-6222, Nov./Dec. 2018.
[22] S. Jiang, S. Saggini, C. Nan, X. Li, C. Chung, and M. Yazdani, "Switched Tank Converters," *IEEE Transactions on Power Electronics*, vol. 34, no. 6, pp. 5048-5062, June 2019.
[23] P. H. McLaughlin, P. A. Kyaw, M. H. Kiani, C. R. Sullivan, and J. T. Stauth, "Two-Phase Interleaved Resonant Switched-Capacitor DC-DC Converter with Coupled Inductors and Custom LC Resonator," *IEEE Applied Power Electronics Conference and Exposition (APEC)*, Anaheim, CA, USA, 2019.
[24] Z. Ye, Y. Lei, and R. C. N. Pilawa-Podgurski, "The Cascaded Resonant Converter: A Hybrid Switched-Capacitor Topology With High Power Density and Efficiency," *IEEE Transactions on Power Electronics*, vol. 35, no. 5, pp. 4946-4958, May 2020.
[25] J. Zhu and D. Maksimović, "Transformerless Stacked Active Bridge Converters: Analysis, Properties, and Synthesis," *IEEE Transactions on Power Electronics*, vol. 36, no. 7, pp. 7914-7926, July 2021.
[26] M. Ursino, S. Saggini, S. Jiang, and C. Nan, "High Density 48V-to-PoL VRM with Hybrid Pre-Regulator and Fixed-Ratio Buck," *IEEE Applied Power Electronics Conference and Exposition (APEC)*, New Orleans, LA, USA, 2020.
[27] P. L. Wong, P. Xu, B. Yang, and F. C. Lee, "Performance Improvements of Interleaving VRMs with Coupling Inductors," *IEEE Transactions on Power Electronics*, vol. 16, no. 4, pp. 499-507, July 2001.
[28] J. Li, C. R. Sullivan, and A. Schultz, "Coupled Inductor Design Optimization for Fast-Response Low-Voltage DC-DC Converters," *IEEE Applied Power Electronics Conference and Exposition (APEC)*, Dallas, TX, USA, 2002.
[29] J. Li, A. Stratakos, A. Schultz, and C. R. Sullivan, "Using Coupled Inductors to Enhance Transient Performance of Multi-Phase Buck Converters," *IEEE Applied Power Electronics Conference and Exposition (APEC)*, Anaheim, CA, USA, 2004.
[30] M. Xu, J. Zhou, K. Yao, and F. C. Lee, "Small Signal Modeling of a High Bandwidth Voltage Regulator Using Coupled Inductors," *IEEE Trans. on Power Electronics*, vol. 22, no. 2, pp. 399-406, March 2007.
[31] M. Chen and C. R. Sullivan, "Unified Models for Coupled Inductors Applied to Multiphase PWM Converters," *IEEE Transactions on Power Electronics*, accepted.
[32] C. R. Sullivan and M. Chen, "Coupled Inductors for Fast-Response High-Density Power Delivery: Discrete and Integrated," *IEEE Custom Integrated Circuits Conference (CICC)*, Austin, TX, USA, 2021.
[33] D. Zhou, Y. Elasser, J. Baek, C. R. Sullivan, and M. Chen, "Inductance Dual Model and Control of Multiphase Coupled Inductor Buck Converter," *IEEE Workshop on Control and Modeling of Power Electronics (COMPEL)*, Aalborg, Denmark, 2020.
[34] Y. Elasser, J. Baek, C. R. Sullivan, and M. Chen, "Modeling and Design of Vertical Multiphase Coupled Inductors with Inductance Dual Model," *IEEE Applied Power Electronics Conference and Exposition (APEC)*, Phoenix, AZ, USA, 2021.
[35] R. C. N. Pilawa-Podgurski, D. M. Giuliano, and D. J. Perreault, "Merged Two-Stage Power Converter Architecture with Soft Charging Switched-Capacitor Energy Transfer," *IEEE Power Electronics Specialists Conference*, Rhodes, Greece, 2008.
[36] D. M. Giuliano, M. E. D'Asaro, J. Zwart, and D. J. Perreault, "Miniaturized Low-Voltage Power Converters With Fast Dynamic Response," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 2, no. 3, pp. 395-405, September 2014.
[37] G. Roberts, N. Vukadinović and A. Prodić, "A Multi-Level, Multi-Phase Buck Converter with Shared Flying Capacitor for VRM Applications," *IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2018, pp. 68-72.
[38] J. Sun, J. Q. Lu, D. Giuliano, T. P. Chow, and R. J. Gutmann, "3D Power Delivery for Microprocessors and High-Performance ASICs," *IEEE Applied Power Electronics Conference and Exposition (APEC)*, Anaheim, CA, USA, 2007.
[39] C. Buttay, C. Martin, F. Morel, R. Caillaud, J. Le Leslé, R. Mrad, N. Degrenne, and S. Mollov, "Application of the PCB-Embedding Technology in Power Electronics - State of the Art and Proposed Development," *International Symposium on 3D Power Electronics Integration and Manufacturing (3D-PEIM)*, College Park, MD, USA, 2018.
[40] W. J. Lambert, M. J. Hill, K. Radhakrishnan, L. Wojewoda, and A. E. Augustine, "Package Inductors for Intel Fully Integrated Voltage Regulators," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 6, no. 1, pp. 3-11, January 2016.
[41] N. Sturcken *et al*., "A 2.5D Integrated Voltage Regulator Using Coupled-Magnetic-Core Inductors on Silicon Interposer," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 1, pp. 244-254, January 2013.
[42] "Using the LMG5200POLEVM-10 48V to Point of Load EVM," Texas Instruments, 2017 [online]. Available: https://www.ti.com/lit/ug/snvu520b/snvu520b.pdf
[43] R. Das, G.-S. Seo, D. Maksimović, and H.-P. Le, "An 80-W 94.6%-Efficient Multi-Phase Multi-Inductor Hybrid Converter," *IEEE Applied Power Electronics Conference and Exposition*, Anaheim, CA, USA, 2019.
[44] M. Halamicek, T. McRae, and A. Prodić, "Cross-Coupled Series-Capacitor Quadruple Step-Down Buck Converter," *IEEE Applied Power Electronics Conference and Exposition*, New Orleans, LA, USA, 2020.
[45] Z. Ye, R. A. Abramson, Y.-L. Syu, and R. C. N. Pilawa-Podgurski, "MLB-PoL: A High Performance Hybrid Converter for Direct 48 V to Point-of-Load Applications," *IEEE Workshop on Control and Modeling of Power Electronics (COMPEL)*, Aalborg, Denmark, 2020.
[46] "Main & Satellite Power Stamp 48V-to-PoL Isolated DC-DC Converters," Bel, 2020 [online]. Available: https://www.belfuse.com/resources/datasheets/powersolutions/ds-bps-48-v-to-pol-power-stamp.pdf
[47] J. Zhu and D. Maksimović, "48 V-to-1 V Transformerless Stacked Active Bridge Converters with Merged Regulation Stage," *IEEE Workshop on Control and Modeling for Power Electronics (COMPEL)*, Aalborg, Denmark, 2020.
[48] "PRM Regulator PRM48BH480T250A00," Vicor, 2020 [online]. Available: http://www.vicorpower.com/documents/datasheets/PRM48BH480T250A00_ds.pdf
[49] "VTM Current Multiplier VTM48MP010x107AA1," Vicor, 2017 [online]. Available: http://www.vicorpower.com/documents/datasheets/VTM48M_010_107AA1.pdf
[50] X. Yang et al., "An 8A 998A/inch^3 90.2% Peak Efficiency 48V-to-1V DC-DC Converter Adopting On-Chip Switch and GaN Hybrid Power Converter," *IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, USA, 2021.
[51] "LTM4664 54VIN Dual 25A, Single 50A μModule Regulator with Digital Power System Management," Analog Devices, 2021 [online], Available: https://www.analog.com/media/en/technical-documentation/data-sheets/ltm4664.pdf
[52] Y. Chen, P. Wang, H. Cheng, G. Szczeszynski, S. Allen, D. M. Giuliano, and M. Chen, "Virtual Intermediate Bus CPU Voltage Regulator," *IEEE Trans. on Power Electronics*, Accepted, DOI: 10.1109/TPEL.2021.3130213.

Jaeil Baek (Member, IEEE) received the B.S. degree in electronics and electrical engineering from Sungkyunkwan University, Suwon, South Korea, in 2011, and the M.S. and Ph.D. degrees in electrical engineering from the Korea Advanced Institute of Science and Technology, Daejeon, South Korea, in 2015 and 2018, respectively.

Since 2019, he has been a Postdoctoral Research Associate with the Department of Electrical and Computer Engineering and the Andlinger Center for Energy and the Environment, Princeton University, Princeton, NJ, USA. His current research interests include point-of-load power converters, grid interface power electronics, digital control approach of converters, and advanced power electronics architecture.

Dr. Baek received the Research Outstanding Award from the Korea Advanced Institute of Science and Technology, the Global Ph.D. Fellowship and Postdoctoral Fellowship Awards from the National Research Foundation of Korea, the First Place Award of the IEEE ECCE Best Demonstration in 2021, and an OCP (Open Compute Project) Best Paper Award in 2021.

Youssef Elasser (Student Member, IEEE) received the B.S. degree in electrical engineering and computer science with a concentration in electric power from Rensselaer Polytechnic Institute, Troy, NY, USA, in 2018. He is currently working toward the Ph.D. degree at Princeton University, Princeton, NJ, USA. His research interests include renewable energy storage systems, dc–dc power conversion, and magnetics design and optimization.

Mr. Elasser was the recipient of the Grainger Scholars Award for distinguished undergraduates studying electric power while at Rensselaer Polytechnic Institute. He has received an IEEE Transactions on Power Electronics Prize Paper award, the first place award for the IEEE ECCE Student Demonstration in 2021, the First Place Award from the 2019 Princeton Innovation Forum, and the prestigious National Science Foundation Graduate Research Fellowship while at Princeton University.

Kaladhar Radhakrishnan (Senior Member, IEEE) received the B.Tech. degree from the Coimbatore Institute of Technology, Coimbatore, India, the M.S. degree from Iowa State University, Ames, IA, USA, and the Ph.D. degree in electrical engineering from the University of Illinois at Urbana–Champaign, Champaign, IL, USA, in 1993, 1995, and 1999, respectively.

He has been with Intel Corporation, Chandler, AZ, USA, since 2000, where he is currently a Fellow with the Technology Development Group. His primary research interests include microprocessor power delivery, and computational electromagnetics which was the focus of this dissertation work. More recently, his areas of focus have been in integrated voltage regulation and magnetic inductors.

Houle Gan (Senior Member, IEEE) received the B.S. and M.S. degrees in Electronics Engineering from Zhejiang University, Hangzhou, China, in 2003 and 2006, respectively. He received the Ph.D. degree in Electrical and Computer Engineering from Purdue University, West Lafayette, IN, USA, in 2010. He is currently a Tech Lead and Senior Staff Engineer at Google, where he leads the power delivery solutions of Google's custom machine-learning platforms. Before that he was with Apple and Intel. His research interests include signal/power integrity, power management techniques, and advanced packaging. He has over 30 IEEE publications and over 10 patent applications and invention disclosures.

Jonathan P. Douglas is an Intel Fellow in the Silicon Engineering Group and director of the group's Integrated Voltage Regulator Center of Excellence at Intel Corporation. In addition to overseeing the center, he is responsible for the power delivery architecture domain for Intel's Client Computing Group and Internet of Things Group. In that capacity, he leads the development of converged system and processor power delivery architectures and circuits.

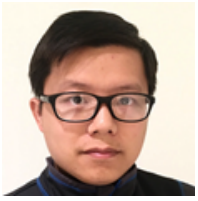
Harish K. Krishnamurthy (Senior Member, IEEE) received the Ph.D. degree in electrical engineering from Arizona State University, Tempe, AZ, USA, in 2008.

He is currently a Principal Engineer with Circuits Research Lab, Intel Labs, Hillsboro, OR, USA, working on power delivery circuits and systems. He has over 25 publications at leading IEEE conferences, over 20 issued patents, and over 30 patent applications filed to date. His research interests include topologies and digital control techniques for fully on-die switching power converters, fully synthesizable digital lowdropout regulators (LDOs), and reconfigurable power delivery.

Dr. Krishnamurthy is serving as a Technical Program Committee Member for the Power management Sub-Committee at the International Solid-State Circuits Conference (ISSCC).

Xin Li (Member, IEEE) received the B.S. and M.S. degrees in electrical engineering from the Harbin Institute of Technology University, Harbin, China, in 2005.

From July 2005 to March 2013, he was with Schneider Electric, as a Power Electronic Design Engineer and Design Manager, working on variable speed drive and active power filter design. From February 2013 to March 2015, he was with Power Integrations as a Lead Application Engineer. He is currently a Technical Lead Manager with Google, Mountain View, CA, USA, where he leads the team to develop power technologies and solutions for Google data center products. His technical interests are in power conversion system, energy storage, and backup system.



Shuai Jiang (Member, IEEE) received his B.S. from Shanghai Jiao Tong University in 2005, and his Ph.D. from Michigan State University in 2013, both in electrical engineering. From 06/2005 to 12/2008, he was a hardware engineer at Schneider Electric. From 05/2012 to 02/2015, he was with Volterra and Intersil as a Senior/Lead system engineer. He is currently a staff power engineer and architect at Google, where he leads the DC-DC technology and roadmap development from board level to chip level for all platforms hardware that goes to Google data centers. His research interests include switched capacitor converters, resonant converters, high current PoL VRs, magnetics, and high-density system integrations. He has over 30 IEEE journal and conference papers as well as over 20 patent applications and invention disclosures.

Charles R. Sullivan (S'93−M'96−SM'12−F'14) received the B.S. degree (with highest Hons.) in electrical engineering from Princeton University, Princeton, NJ, USA, in 1987, and the Ph.D. degree in electrical engineering from the University of California, Berkeley, USA, in 1996.

Between the B.S. and Ph.D. degrees, he was with Lutron Electronics designing electronic ballasts. He is currently a Professor at Thayer School of Engineering at Dartmouth, Hanover, NH, USA, where he is also director of the Power Management Integration Center. His research interests include modeling and design optimization of magnetics and other passive components for high-frequency power conversion and wireless power transfer.

Dr. Sullivan received the Power Electronics Society Modeling and Control Technical Achievement Award in 2018 and has received three Power Electronic Society Prize Paper Awards. He has 43 US patents and is a co-founder of Resonant Link, Inc.

Minjie Chen (Senior Member, IEEE) received the B.S. degree from Tsinghua University, Beijing, China, in 2009, and the S.M., E.E., and Ph.D. degrees from Massachusetts Institute of Technology (MIT), Cambridge, MA, USA, in 2012, 2014, and 2015, respectively. He is an Assistant Professor of Electrical and Computer Engineering and Andlinger Center for Energy and the Environment at Princeton University, where he leads the Princeton Power Electronics Research Lab. His research interests include complex power architecture, power magnetics, control, and machine learning methods for high performance power electronics.

Dr. Chen received three IEEE Power Electronics Society Prize Paper Awards, a COMPEL Best Paper Award, an OCP Best Paper Award, the NSF CAREER Award, a Dimitris N. Chorafas Award for outstanding Ph.D. Thesis at MIT, an Outstanding Reviewer Award from IEEE Transactions on Power Electronics, three ECCE Best Demonstration Awards, multiple APEC Outstanding Presentation Awards, a Siebel Energy Institute Research Award, a C3.ai DTI Research Award, and the First Place Award from the Innovation Forum of Princeton University. He was included in the *Princeton Engineering Commendation List for Outstanding Teaching* for multiple times.

He is the Vice Chair of IEEE PELS Technical Committee on Design Methodologies (TC10), Associate Editor of IEEE Transactions on Power Electronics, Associate Editor of IEEE Journal of Emerging and Selected Topics in Power Electronics, Associate Technical Program Committee Chair of IEEE Energy Conversion Congress and Exposition (ECCE) in 2019, Student Activity Chair of IEEE Energy Conversion Congress and Exposition (ECCE) in 2020, and the Technical Program Committee Chair of IEEE International Conference on DC Microgrids (ICDCM) in 2021.