Multitrack Power Factor Correction Architecture

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***Abstract*—Single-phase universal-input ac-dc converters are needed in a wide range of applications. This paper presents a novel power factor correction (PFC) architecture that can achieve high power density and high efficiency for grid-interface power electronics. The Multitrack PFC architecture reduces the internal device voltage stress of the power converter subsystems, allowing PFC circuits to maintain zero-voltage-switching (ZVS) at high frequency (1 MHz–4 MHz) across universal input voltage range (85 $\mathrm{V_{AC}}$–265 $\mathrm{V_{AC}}$). The high performance of the power converter is enabled by delivering power in multiple stacked voltage domains and reconfiguring the power processing paths depending on the input voltage. This Multitrack concept can be used together with many other design techniques for PFC systems to create mutual advantages in many function blocks. A prototype 150 W, universal ac input, 12 $\mathrm{V_{DC}}$ output, isolated Multitrack PFC system with a power density of 50 W/in^3 and a peak end-to-end efficiency of 92% has been built and tested to verify the effectiveness of the Multitrack PFC architecture.**

***Index Terms*—AC-DC power conversion, Power factor correction, Multitrack architecture, Grid-tied power electronics.**

I. Introduction

Single-phase universal input-voltage ac-dc converters are widely used in applications ranging from telecom servers to electric vehicle chargers [1]–[7]. Power electronics designs in these systems require high efficiency and high power density. Moreover, high power factor and wide-operation range is desirable to best extract power from the ac grid to dc loads. Increasing the switching frequency [6]–[11] (e.g., into the multi-MHz range) can reduce the size of the passive components and is an effective way of improving power density. Soft switching and reduced device stress can help preserve high efficiency [12]–[15]. This paper presents a Multitrack PFC architecture that enables high frequency ac-dc systems that operate efficiently across wide input voltage range, and can significantly reduce the passive component size to achieve high power density. The Multitrack architecture represents a new design method to improve the power density of single-phase grid interface systems which can be used in combination with many existing methods such as high frequency operation [6]–[10], bridge-less PFC with ZVS extension techniques [11], and active energy buffer technologies [16]–[18].

Figure 1 shows a typical 2-stage PFC system with a low voltage dc output. It comprises a ac-dc power factor correction (PFC) stage and a magnetic isolation stage. The PFC stage is usually implemented as a diode rectifier and a boost converter. The boost converter can be operated in continuous conduction mode (CCM), boundary conduction mode (BCM) or discontinuous conduction mode (DCM) [12]. The isolation stage is usually implemented as a series resonant converter, an LLC converter, or a dual-active-bridge (DAB) converter [19]–[21]. The isolation stage functioning as a dc transformer with relatively fixed voltage conversion ratio to improve the efficiency and power density of that stage. The twice-line-frequency energy buffer function is performed by a dc-link capacitor between the two stages.

There are multiple ways of improving the performance of this PFC architecture. To reduce the component count, single-stage PFC architectures have been explored [4]. To reduce the diode forward-voltage drop loss, bridge-less architectures such as totem-pole PFCs are widely adopted [5], [22]. With DCM

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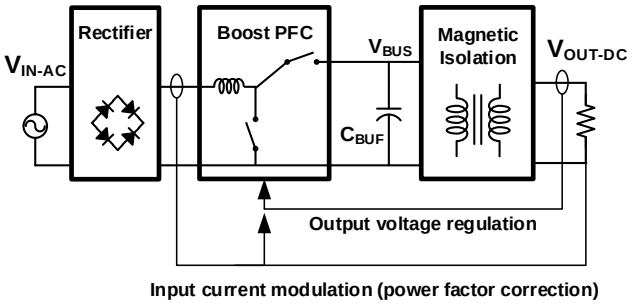

Fig. 1. A classic two-stage PFC architecture with a boost PFC and an isolation stage (e.g., a LLC converter).

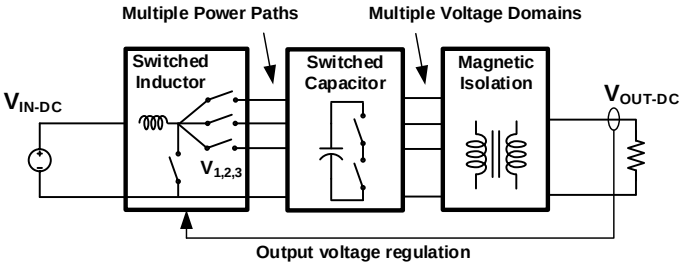

Fig. 2. Block diagram of a Multitrack dc-dc architecture [1].

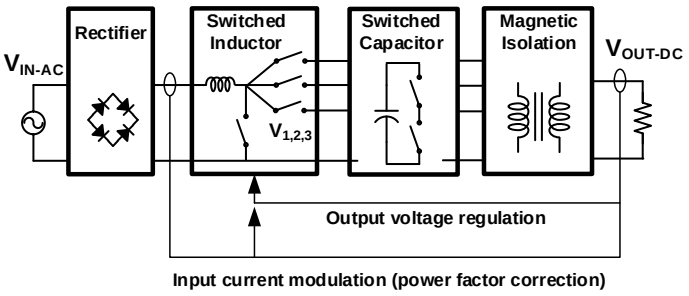

Fig. 3. Block diagram of a Multitrack PFC architecture [25].

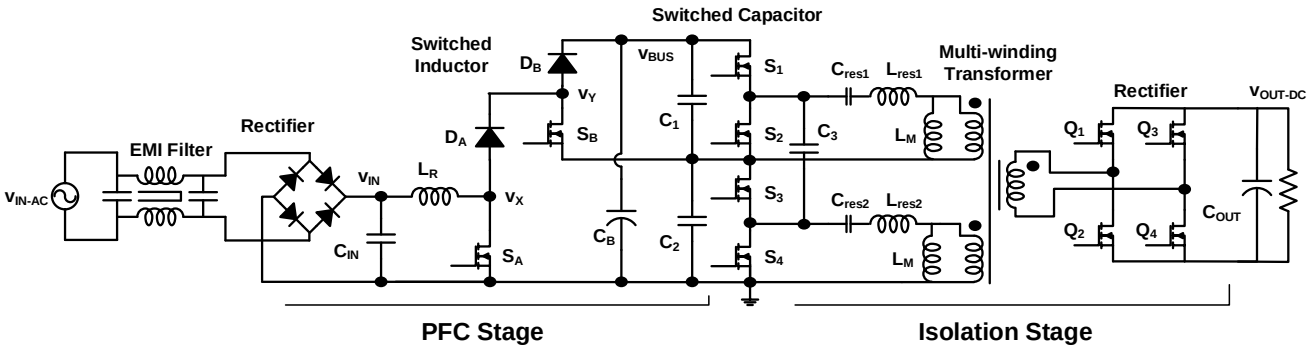

Fig. 4. Schematic of a Multitrack PFC with a grid-interface PFC stage and a merged isolation stage.

operation and valley voltage detection, zero-voltage-switching of the boost switch can be achieved at high frequency, enabling smaller inductor size and low switching loss [23]. Alternative topologies can achieve high-frequency ZVS operation over much wider ranges [9]. The dc-link capacitor can be replaced by an active energy buffer to achieve high power density [16]–[18]. By operating at high frequency, using planar magnetics, and applying dual-active-bridge techniques, the efficiency and power density of the isolation stage can be greatly improved [1], [7], [13].

This paper presents a Multitrack PFC architecture to improve the performance and reduce the size of grid-interface PFC converters. Instead of focusing on each single function block of a PFC system, this architecture creates mutual advantage across multiple function blocks by appropriately merging them together and reducing the overall power conversion stress. It can be used together with many other existing methods to achieve optimal system performance. By increasing the circuit complexity and component count, the Multitrack PFC reduces the overall switch stress, reduces the energy storage requirement, and reduces the dv/dt, and enables higher power density and smaller size while maintaining similar efficiency performance as traditional solutions.

Figure 2 shows the block diagram of a previously explored Multitrack dc-dc architecture [1], [24], which is a key building block of the proposed Multitrack PFC architecture. The Multitrack dc-dc architecture comprises a switched-inductor circuit, a switched-capacitor circuit, and a magnetic isolation circuit, with their functions partially merged. The switched-inductor circuit regulates the voltage, the magnetic isolation circuit offers isolation and voltage scaling, and the switched-capacitor circuit creates multiple intermediate bus voltages (V_1, V_2, V_3, etc) that bridge the two previous sub-circuits. These sub-circuits are not independent: the switched-inductor circuit couples into the multiple levels of the switched-capacitor circuit as the regulation stage; likewise, the switched-capacitor circuit is merged with the magnetic isolation circuit by reusing the switches of the switched-capacitor circuits to drive the shared transformer. Voltage regulation is principally performed by the switched-inductor circuit. The effectiveness of the Multitrack dc-dc architecture was previously demonstrated in a dc-dc telecom brick converter with extremely wide input voltage (>4:1) range and high power density (>450 W/in^3) [1].

The Multitrack PFC architecture as shown in Fig. 3 is an ac-dc extension of the Multitrack dc-dc concept. The Multitrack PFC architecture inherits the Multitrack dc-dc architecture's capability of efficiently handling an extremely wide input voltage range with low component stresses. Compared to the previous dc-dc implementation [1], the Multitrack PFC architecture interfaces with the ac grid, has additional voltage and current control loops to modulate the input current and regulate the output voltage, and has an energy buffer that functions as a part of the switched-capacitor circuit. The Multitrack PFC architecture leverages the advantages of the Multitrack dc-dc architecture, and address the unique challenges in achieving soft-switching at high frequencies across universal ac line voltage while performing PFC and voltage regulation. This paper is developed from our earlier conference publication [25] and presents extended theoretical analysis and experimental results.

The remainder of this paper is organized as follows: Section II presents the key principles of the Multitrack PFC architecture, including steady-state operation and mode-switching actions of the PFC stage. The details of the system control, voltage regulation, and zero-voltage-switching are presented in Section III. Section IV presents the key principles of the switched capacitor circuit and isolation stage. Section V discusses the grid interface and startup strategy. Section VI summarizes the key advantages of the Multitrack PFC architecture. Details about the prototype design and experimental results are provided in Section VII. Finally, Section VIII concludes this paper.

II. Multitrack PFC Principles

Figure 4 shows the topology of an example 2-Track Multitrack PFC converter. This topology can be further extended to include multiple tracks. The key principles are:

1) The circuits between C_B and C_{OUT} including the transformer function as a dc-transformer with fixed voltage conversion ratio (from 420V to 12V). During normal operation, the voltage on energy buffer capacitor C_B is maintain at an approximately fixed bus voltage (e.g., 420V). The 2:1 switched capacitor stage (comprising S_1-S_4 & C_1-C_3) maintains the voltage balancing of C_1-C_3 (e.g., 210V each). S_1-S_2 & S_3-S_4 formulate two half-bridge pairs that drive the two primary windings in a synchronized fashion. With a nearly fixed voltage conversion ratio, this dc-transformer can be optimized to achieve high efficiency and high power density across a

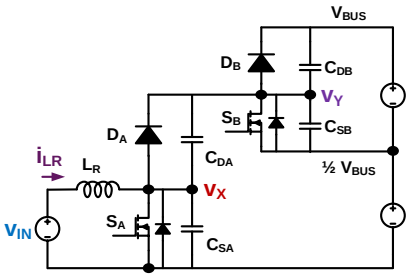

Fig. 5. Boost stage of the Multitrack PFC architecture.

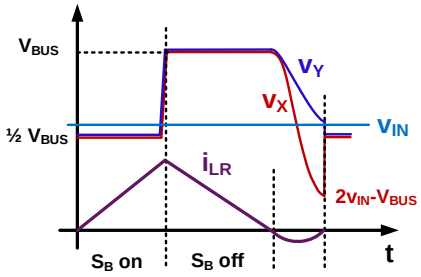

Fig. 6. Example ZVS waveforms in Mode 4 operation with S_B in ZVS.

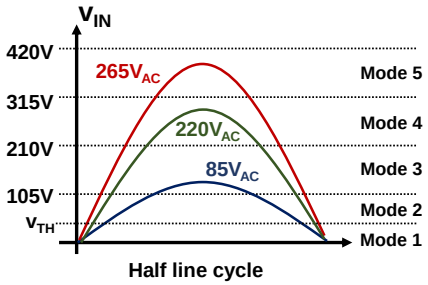

Fig. 7. Example mode switching strategy for three line input voltages.

wide power range, as demonstrated in [13]. Of course, the second stage can be modulated to compensate the ripple in the energy buffer capacitor voltage.

2) The inclusion of C_3 adds a switched capacitor mechanism in the Multitrack architecture to passively maintain the voltage balance of stacked voltage domains. Without C_3, the control of the PFC stage is coupled with the control of the isolation stage, placing challenges in controller design. As a part of the switched-capacitor circuit, the physical size of C_3 is very small. If the primary windings provide sufficient inductive impedance, or if a small inductor is added in series with C_3 to create a resonant path, C_3 is soft-charged [31] and there is no charge transfer loss. The principles of the hybrid switched-capacitor and LLC mechanism in the Multitrack architecture are shown in Fig. 8.

3) The circuit elements from C_{IN} to C_B form a PFC mechanism which can deliver current (and power) into either or both of the two stacked voltage domains (V_{C1} and V_{C2}). As a result of switched capacitor energy transfer, the voltage of C_B is twice that of C_2. In other words, if the voltage of C_B is maintained at 420V, the voltage of C_2 is naturally maintained at 210V. Selecting appropriate levels to switch v_X among reduces the voltage drop across the boost inductor L_R, reduces the dv/dt at the switching nodes, and enables zero-voltage-switching (ZVS) of S_A and S_B across wide input voltage range. These features are not achievable in a conventional boost PFC configuration.

The Multitrack PFC architecture is well suited for universal input ac-dc applications (85V_{AC}–265V_{AC}). Grid-interface PFC specifications such as EN61000-3-2 have a threshold input voltage below which the converter is turned off. We denote this threshold voltage as V_{TH}. The steady state voltage of C_B, V_{BUS}, is selected as 420V. Across the line cycle, the Multitrack PFC architecture has five operation modes:

- Mode 1: When $0\text{V} < v_{IN} < V_{TH}$, both S_A and S_B are kept off and the converter is off. V_{TH} should be optimally adjusted depending on the input voltage and power level to achieve highest efficiency while meeting the grid interface requirements.
- Mode 2: When $V_{TH} < v_{IN} < 1/4V_{BUS}$, S_B is kept on, and S_A actively switches. L_R, S_A, D_A function as a QSW (quasi-square-wave, or valley-switched) boost converter with an output voltage of $1/2V_{BUS}$. Switched capacitor energy transfer of S_1-S_4 balances the voltage of C_1 and C_2. Since v_{IN} is smaller than $1/4V_{BUS}$, the voltage at the drain of S_A can resonate to ground, enabling ZVS turn on of S_A. This configuration also reduces the dv/dt at the switch node, which facilitates the high frequency operation of the boost converter.
- Mode 3: When $1/4V_{BUS} < v_{IN} < 1/2V_{BUS}$, S_B is kept off, and S_A actively switches. L_R, S_A, D_A, D_B function as another QSW boost converter with an output voltage of V_{BUS}. Similarly, since v_{IN} is smaller than one half of V_{BUS}, ZVS turn on of S_A is enabled. In this operation mode, the PFC stage functions as a conventional boost converter feeding current into the dc voltage V_{BUS}. Note that D_A and D_B both only need to be rated at $1/2V_{BUS}$.
- Mode 4: When $1/2V_{BUS} < v_{IN} < 3/4V_{BUS}$, S_A is kept off, and S_B actively switches, L_R, S_B, D_B function as a QSW boost-derived converter delivering energy into both the $1/2V_{BUS}$ and V_{BUS} nodes, with D_A effectively operating in series with L_R. With D_A acting in series with L_R, the operation of this converter is different from a conventional boost converter. When D_A, D_B and S_A are off, L_R resonants with the lumped parasitic capacitances of D_A, D_B, S_A, and S_B. Fig. 5 and Fig. 6 illustrate the operation details. The inductor current linearly ramps up when S_B is on. When the inductor current is positive and the diodes D_A and D_B are both on, both v_X and v_Y are V_{BUS}. After the inductor current reverses its polarity, D_B and D_A are turned off. v_X and v_Y drops and v_X resonates from V_{BUS} to $2v_{IN} - V_{BUS}$. In general, the circuit can be analyzed as a capacitive voltage divider network, and the lowest voltage that v_Y can reach is $V_{BUS} - \frac{2C_{DA}(V_{BUS}-V_{IN})}{C_{DA}+C_{SB}+C_{DB}}$. With sufficient energy storage in the inductor, v_Y can drop to $1/2V_{BUS}$ and will be clamped at $1/2V_{BUS}$ by the body diode of S_B. v_X drops until i_{LR} changes direction.

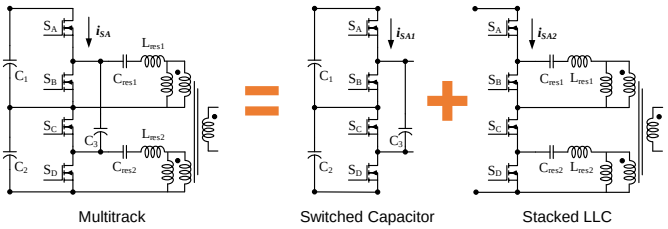

Fig. 8. Principles of the hybrid switched-capacitor LLC structure. Two stages are merged together to create mutual advantages.

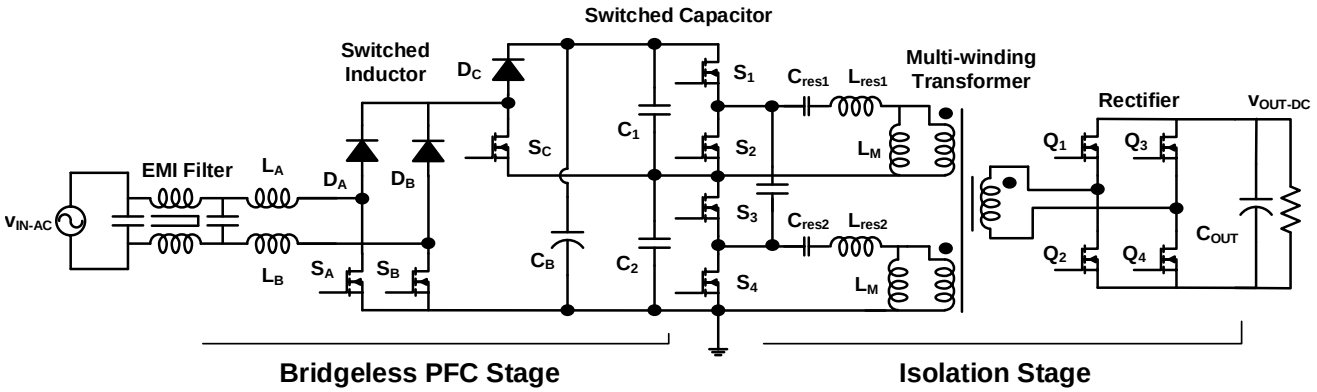

Fig. 9. Schematic of an example Multitrack bridgeless PFC.

- Mode 5: When $v_{IN} > 3/4V_{BUS}$, S_A is kept off, and S_B actively switches. In this mode S_B cannot achieve ZVS, but can achieve reduced voltage turn-on (switch when the drain voltage reaches the minimum).

Fig. 7 illustrates the mode-selection actions of the PFC converter for three different line voltages. With $85\mathrm{V_{AC}}$ input, the converter operates in Modes 1–3 in a quarter line cycle. With $110\mathrm{V_{AC}}$ input, the converter operates in Modes 1–4 in a quarter line cycle. With $265\mathrm{V_{AC}}$ ac input, the converter operates in all five modes in a quarter line cycle.

The Multitrack PFC concept can be merged together with many other approaches to further improve the performance of single-phase grid-interface systems. For example, replacing the boost diode with synchronous switches can eliminate the diode forward voltage loss, as can the use of a bridgeless front-end structure to eliminate line-frequency rectification loss. The schematic of an example Multitrack bridgeless-PFC is shown in Fig. 9. The single energy buffer capacitor, C_{BUF}, can be replaced with an active energy buffer to further reduce the system size. The height of the electrolytic capacitor is the limitation of reducing the system height. Novel active energy buffer architectures can be developed to leverage the Multitrack concept [26]. Design techniques to reduce the loss or expand the operation range of the isolation stage, such as the variable frequency multiplier (VFX) technology described in [27], can be used together with the Multitrack architecture.

The single-phase Multitrack architecture can be extended to three-phase by paralleling three bridgeless PFC stages and eliminating the diode rectifier. The isolation stage doesn't need to be changed. The twice-line-frequency energy buffer is not needed. The Multitrack concept scales well to kilo-watt applications because: 1) it allows the usage of low voltage rating devices in high voltage applications; 2) it reduces the voltage drop across the inductor and reduces the inductor size; 3) it reduces the dv/dt at the switch nodes, mitigating the challenges of driving high voltage semiconductor devices; 4) it reduces the effective common-mode capacitance of the isolation transformer. For high voltage high power applications, the Multitrack architecture shares similar advantages as Modular Multilevel Converters (MMCs) and Flying Capacitor Multilevel Converters (FCMLs) concepts, and uniquely focuses on merging switched-capacitor circuits with multi-winding magnetic structures.

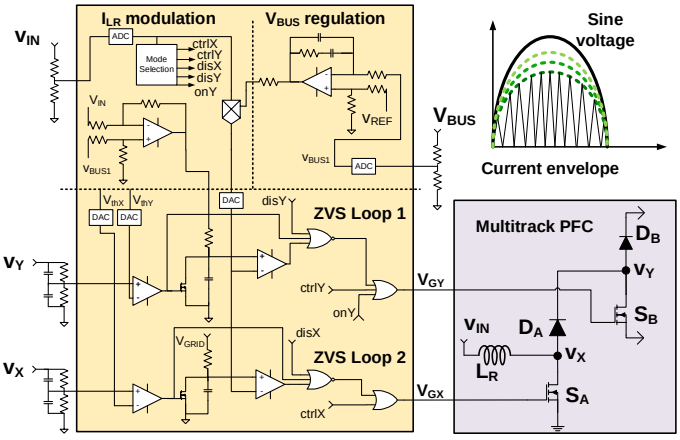

Fig. 10. Control diagram of the Multitrack PFC stage. V_{IN}, V_{BUS}, V_X and V_Y are measured and the two gate signals, V_{GX} and V_{GY}, are the outputs.

III. System Control and Zero-Voltage-Switching

The implemented Multitrack PFC system has four control loops – two high frequency ZVS loops to control ZVS timing of S_A and S_B, respectively; one feedback loop which regulates the bus voltage C_B; and one feedback loop that modulates the input current to follow a sinusoidal pattern. Fig. 10 shows the control framework of the Multitrack PFC. V_{IN}, V_{BUS}, V_X and V_Y are measured and the two gate signals, V_{GX} and V_{GY}, are the outputs. Each of the two ZVS control loops comprises two comparators with programmable thresholds and a few logic gates. One comparator senses the voltage of the switch node and sets the turn-on timing to achieve ZVS, while the other comparator is used to realize switch on-time based control to approximately implement inductor current control and sets the turn-off timing. [6]–[9] show the key operation principles of this ZVS detection circuit, and provide other examples of this general on-time-based current control strategy. These comparator-based controls operate at multiple MHz and maintain ZVS of the two switches regardless of the circuit parameters. The inductor current control loop and the bus voltage regulation loop are implemented in a micro-controller. The voltage control loop of the Multitrack PFC is implemented as a PI controller, the 60Hz current modulation is controlled by setting the on-time of the switch, which is similar to a DCM boost PFC.

When the input voltage is close to the boundary between two modes, a hysteresis margin needs to be implemented to avoid system oscillation between two modes. In a 2-track Multitrack converter, the mode-switching boundaries are $\frac{1}{4}V_{BUS}$, $\frac{1}{2}V_{BUS}$, and $\frac{3}{4}V_{BUS}$. When the system operates close to the mode-switching boundary, the ZVS detection circuit may not be triggered [6], thus the ZVS valley detection circuit should be disabled and the switched are hard-switched. A wide hysteresis margin guarantees smooth transition, at the cost of higher switching loss. In our prototype, a hysteresis margin of 5% V_{BUS} around the mode-switching boundary can safely enable smooth mode transition.

One key advantage of the proposed Multitrack PFC architecture is that it significantly extends the ZVS range of universal-input single-phase PFC converters. In a conventional boost PFC system with valley switching, the maxiumum input voltage for the boost switch to achieve ZVS is $1/2V_{BUS}$, i.e., the input voltage has to be lower than one half of the dc bus voltage to realize ZVS. In a 2-Track Multitrack PFC, the maximum input voltage for ZVS is extended to $3/4V_{BUS}$, covering a very wide input voltage range. The ZVS range can be further extended with more stacked tracks. Depending on the input voltage and the operating current, there are six possible ZVS states of the Multitrack PFC as shown in the six sub-figures of Fig. 11:

- *State A*: S_B is kept on, and S_A is switching. The PFC stage function as a boost converter with $1/2V_{BUS}$ as the output voltage. If v_{IN} is lower than $1/4V_{BUS}$, ZVS on S_A is achived as if S_A was in a typical boost converter. During the ZVS transition period, C_{DA} and C_{SA} are effectively connected in parallel and resonant with L_R. The ZVS transition resonant angular frequency is $\omega_{ZVS} = 1/\sqrt{L_R(C_{DA}+C_{SA})}$.
- *State B*: S_B is kept off, and S_A is switching. The PFC stage functions as a boost converter with V_{BUS} as the output voltage. If v_{IN} is lower than $1/2V_{BUS}$, and if v_x reaches ground before v_Y reaches $1/2V_{BUS}$, ZVS on S_A is achived as if S_A was in a boost converter. During the ZVS transition period, C_{SB}, C_{DB} and C_{DA} formulates a capacitor network which is connected in parallel with C_{SA} to resonant with L_R. The ZVS transition resonant angular frequency is $\omega_{ZVS} = 1/\sqrt{L_R(C_{SA}+C_{DA}||(C_{DB}+C_{SB}))}$.
- *State C*: S_B is kept off, and S_A is switching. v_Y reaches $1/2V_{BUS}$ and is clamped by the body diode of S_B before v_X reaches ground. The voltage transition of v_X has two piecewise steps. Before v_Y reaches $1/2V_{BUS}$, C_{DB} and C_{SB} are connected in parallel, then connected in series with C_{DA}, and connected in parallel with C_{SA} and resonant with L_R. The ZVS transition resonant angular frequency is $\omega_{ZVS} = 1/\sqrt{L_R(C_{SA}+C_{DA}||(C_{DB}+C_{SB}))}$. After v_Y reaches $1/2V_{BUS}$, v_Y is clamped at $1/2V_{BUS}$ by D_B, and L_R is only connected in parallel with C_{DA} and C_{SA}. The ZVS transition resonant angular frequency becomes $\omega_{ZVS} = 1/\sqrt{L_R(C_{DA}+C_{SA})}$. Fig. 11C shows the two-step ZVS transient of v_X - the slope of the resonant curve changes when v_Y crosses $1/2V_{BUS}$.
- *State D*: S_A is kept off, and S_B is switching. The voltage transition of v_Y has multiple steps. After S_B is switched off, v_Y starts to drop from V_{BUS} to $1/2V_{BUS}$, and v_X starts to drop from V_{BUS} to ground but may not be able to reach ground. As v_X drops, C_{SA}, C_{DA}, C_{SB} and C_{DB} function as a voltage divider that determines the transients of v_X and v_Y. After v_Y reaches $1/2V_{BUS}$, S_B can be turned on with ZVS. The inductor first resonate with C_{DA} and brings v_X back to $1/2V_{BUS}$, then is charged

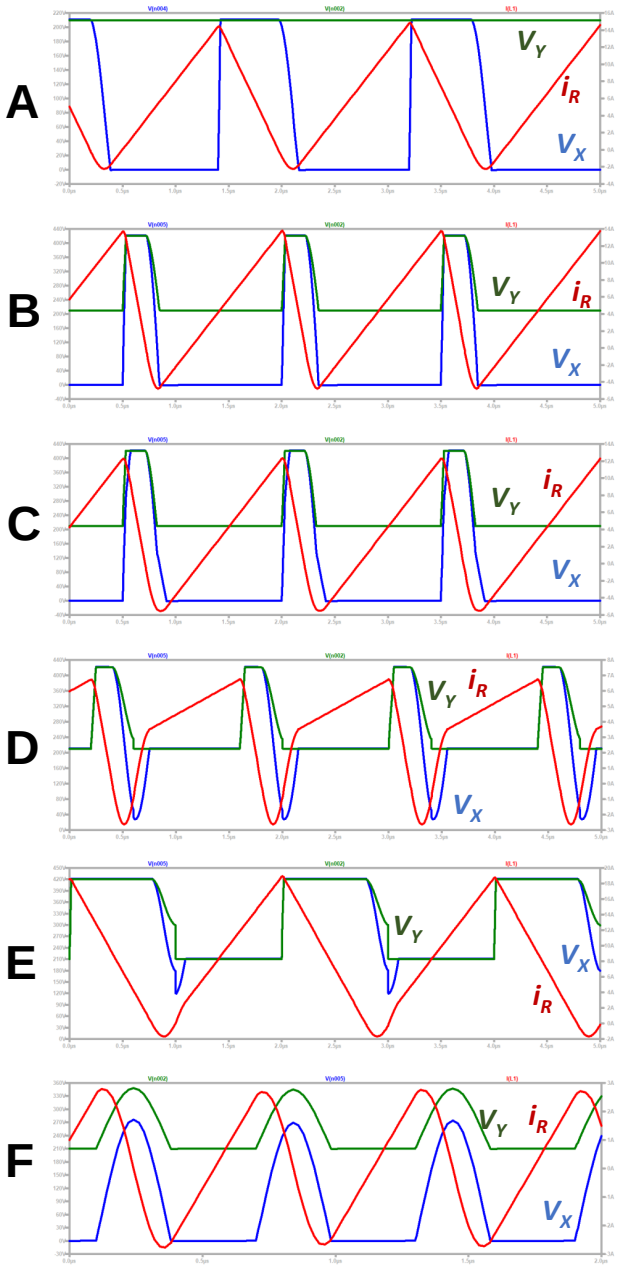

Fig. 11. Six ZVS operating states of the Multitrack PFC: A) S_A achieves ZVS with $v_{IN} < 1/4V_{BUS}$; B) S_A achieves ZVS with $1/4V_{BUS} < v_{IN} < 1/2V_{BUS}$ while v_Y does not reach $1/2V_{BUS}$; C) S_A achieves ZVS with $1/4V_{BUS} < v_{IN} < 1/2V_{BUS}$ while v_Y is clamped at $1/2V_{BUS}$; D) S_B achieves ZVS with $1/2V_{BUS} < v_{IN}$; E) S_B doesn't achieve ZVS but switch as low drain-to-source voltage; F) Input current is not high enough to force the diode on.

up linearly while connected between v_{IN} and $1/2V_{BUS}$.
- *State E*: When v_{IN} is close to $3/4V_{BUS}$, v_Y cannot reach $1/2V_{BUS}$. ZVS of S_B cannot be achieved. However, the voltage across S_B is still lower than $1/2V_{BUS}$, allowing S_B to be turned on with reduced drain-to-source voltage.
- *State F*: When the input current is very low, the inductor current i_{LR} may not be high enough to charge up v_X and v_Y and force the diode on. The system is trapped in a resonant mode without transferring energy between the input and the output. In the prototype system, an internal control loop detects this condition and stops this operation. The action of the circuit will restart when the input voltage reaches a higher level in a line cycle.

IV. Switched Capacitor and Isolation Stage

In the merged isolation stage, the combination of the switched capacitor circuits and the MISO transformer (the *hybrid switched-capacitor/magnetics* circuit structure [1]) creates both soft-switching and soft-charging opportunities [28]–[31] for the switched-capacitor switches . As shown in Fig. 4, the operation of S_1-S_4 can be interpreted as the superposition of a switched-capacitor circuit and two series-resonant circuits. The switched-capacitor circuit comprises S_1–S_4, and C_1–C_3. S_1 and S_2 are one pair of half bridge switches. S_3 and S_4 are another pair of half bridge switches. S_1 and S_3 are synchronously switched as one phase, and S_2 and S_4 are synchronously switched as the other phase. Energy is transferred by C_3 across the two voltage domains. The utilization of switched-capacitor energy transfer enables high efficiency and high power density.

At the same time, S_1, S_2, C_{res1}, L_{res1} formulate one LLC circuit, and S_3, S_4, C_{res2}, L_{res2} formulate the other LLC circuit. The two LLC circuit are coupled by the magnetizing inductance L_M of the transformer, adding one additional path for energy transfer between the two voltage domains. We utlize a series-resonant isolation stage here, but it will be recognized that other isolation stage designs could likewise be used. This transformer in the prototype system is efficiently implemented as a printed-circuit-board (PCB) embedded transformer with well controlled parameters [13]. The switched capacitor energy transfer and the resonant energy transfer function together. When the input voltage is low, significant power is processed by the switched-capacitor mechanism – the switches consequently see a net capacitive load and are hard-switched; when the input voltage is high, the power is processed by the series-resonant mechanism (and delivered to the output) is sufficient to offset the capacitive energy transfer such that the switches have a net inductive load, enabling ZVS, which is beneficial for high frequency designs.

The two half-bridge resonant converters stacked in the two voltage domains are designed to form an LLC converter with a resonant tank with low quality factor - Q. A low Q tank can tolerate the small mismatch between the two leakage inductances of the transformer primary windings, allowing balanced current sharing between the two half-bridge resonant converters. A high Q tank can provide voltage regulation capability on the isolation stage to compensate for the voltage ripple on the buffer capacitor, or provide longer hold-up time. Similar to a LLC design, one can make trade-offs among the switching loss, conduction loss and magnetics loss by sizing the magnetizing inductance of the transformer.

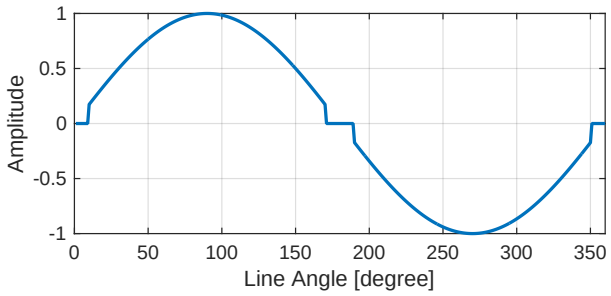

Fig. 12. A sinusoidal waveform with a cutoff angle of 10° near the zero-crossing. A cutoff angle enables wider ZVS range and higher system efficiency.

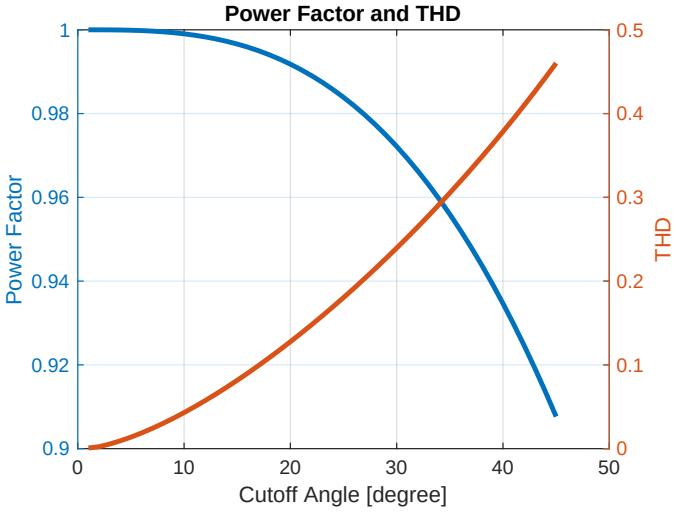

Fig. 13. Power factor and total harmonic distortion (THD) of a Multitrack PFC with a cutoff angle between 0° and 45°. A cutoff angle of 10° leads to a power factor of 99.9% and a THD of 4.3%.

V. Grid Interface and Startup Strategy

The Multitrack PFC interfaces with the ac grid through boundary-conduction-mode (BCM) operation. When the line voltage is very low (near zero-crossing), with high power factor grid-interface, the peak inductor current may not be high enough to fully charge/discharge the parasitic capacitance and enable ZVS. As a result, it is preferable to implement a cut-off angle near the zero-crossing of the line voltage. During this cutoff period, the PFC is kept off. Fig. 12 shows a sinusoidal waveform with a cutoff angle of 10° near the zero-crossing. Fig. 13 shows the power factor and the total-harmonic-distortion (THD) for a sinusoidal waveform with a cutoff angle between 0 degree and 45 degree. A cutoff angle of 10° leads to a power factor of 99.9% and a THD of 4.3%.

The switched capacitor circuit needs to be be precharged to enable steady state operation of the ZVS detection circuit. To charge the bus voltage smoothly to the pre-determined V_{BUS}, a four-step startup strategy has been developed.

TABLE I
DESIGN SPECIFICATIONS OF THE PROTOTYPE PFC.

Specifications	Values
Input Voltage	85 V_{AC} – 265 V_{AC}
Output Voltage	Isolated & regulated 12 V_{DC}
Rated Power	150 W
Volume	3 inch^3, 3.5 in $\times$2.15 in$\times$0.4 in
DC Bus Voltage	420 V_{DC}
PFC Frequency	1 MHz – 4 MHz
Isolation Stage Frequency	500 kHz – 700 kHz
Boost Inductor Size	10 μH
Buffer Capacitor Size	66 μF

- *Step 1: High-side Switch PWM Mode.* Switch S_B is operated with a fixed duty ratio and S_A is kept off until the bus voltage reach $1/2V_{BUS}$. The converter runs in open-loop and senses v_{BUS}.
- *Step 2: Low-side Switch PWM Mode.* Switch S_A is operated with a fixed duty ratio and S_B is kept off until bus voltage reach $3/4V_{BUS}$. The converter runs in open-loop and senses v_{BUS}.
- *Step 3: Voltage Regulation & Non-ZVS Mode.* PI voltage regulation of the bus is initiated, but operating the boost stage as a PWM converter with variable on-time and fixed off-time. The converter runs in closed-loop, senses v_{BUS} and regulates i_{LR}.
- *Step 4: Voltage Regulation & ZVS Mode.* The converter runs in closed-loop, senses v_{BUS}, regulates i_{LR}, and operates in ZVS.

The switched capacitor half-bridge switches S_1-S_4 are kept operating during the entire startup process. C_1 and C_2 are charged simultaniously with low loss and low inrush current.

When the input voltage is close to the boundary between two modes, a hysteresis margin needs to be implemented to avoid system oscillation between two modes. In a 2-track implementation, the mode-switching boundaries are $\frac{1}{4}V_{BUS}$, $\frac{1}{2}V_{BUS}$, and $\frac{3}{4}V_{BUS}$. A $5\%V_{BUS}$ hysteresis margin is sufficient to maintain smooth mode-transition. Note the ZVS valley detection circuit may not trigger when the voltage is close to the mode-boundary. If the ZVS valley detection circuit doesn't trigger, the system is lock in one mode and the converter will stop functioning. We disabled the ZVS valley detection circuit and hard switch the switches when the input voltage is within the hysteresis margin. This strategy is implemented in our design and the hard-switching loss is negligible.

VI. ADVANTAGES OF THE MULTITRACK PFC

In summary, the proposed Multitrack PFC architecture has the following advantages:

- *Extended ZVS range*: In a conventional boost PFC architecture, the boost converter cannot achieve ZVS when the input voltage is larger than one half of the bus voltage. The Multitrack architecture enables wider ZVS range.
- *Smaller boost inductor size*: The Multitrack architecture can significantly reduce the voltage drop across the boost inductor and reduce the required inductor size.

TABLE II
BILL OF MATERIALS (BOM) OF THE PROTOTYPE CONVERTER.

Device Symbol	Component Description
S_1–S_4, S_A–S_B	GaN Systems 650V 66502B
D_A–D_B	2x CREE C3D1P7060 SiC Schottky
L_R	10μH EQ13 3F45 core
C_{in}	X5R Ceramic, 500V, 100nF
C_1, C_2	X7R Ceramic, 500V, 2μF
C_3	X7R Ceramic, 500V, 2 μF
C_{BUF},	Panasonic 450V electrolytic
C_{out}	X5R Ceramic, 25V, 1000 μF
C_{res1}, C_{res2}	C0G ceramic, 250V, 7nF
L_{res1}, L_{res2}	11μF, 10 turns, 3F45, ER11
MISO Transformer	EQ30, 3F45, ratio 8:8:1, 6-layer PCB
Q_1–Q_4	8x EPC2023C GaNFETs

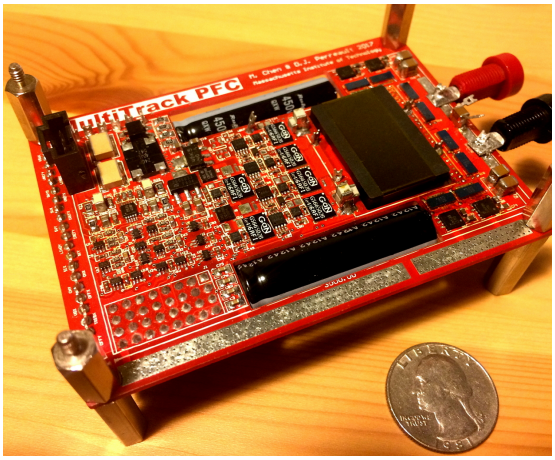

Fig. 14. A prototype Multitrack PFC and a US quarter. This converter can take universal ac input and produce isolated 12V_{DC} output with 150 W maximum power. The power density is 50W/inch^3.

- *Reduced dv/dt on switches*: Benefiting from the multiple stacked voltage domains, the dv/dt at the many switch nodes are lower than the dv/dt at the switch nodes of conventional PFC architectures. The reduced dv/dt also reduces the common-mode current injection from the primary windings to the secondary windings.
- *Reduced voltage rating*: Similar to the Multitrack dc-dc converter, the voltage rating of the switches in a Multitrack PFC are also reduced, leading to lower conduction losses and smaller parasitics, and further facilitating high-frequency operation.
- *Better heat distribution*: The Multitrack power conversion architecture naturally distributes heat on the printed circuit board, pushing the fundamental efficiency/power-density tradeoff boundaries.

VII. PROTOTYPE AND EXPERIMENTAL RESULTS

A prototype Multitrack PFC converter has been built and tested. The key design parameters of the prototype are listed in Table I. The Bill-of-Material (BoM) of the prototype is listed in Table II. These component values are jointly optimized and experimentally tuned to achieve the highest performance across the wide operation range. The power stage of the converter is built following the schematic of Fig. 4,

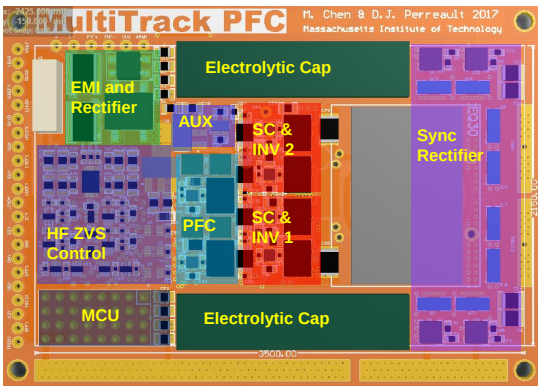

Fig. 15. PCB layout of the prototype Multitrack PFC with key components labeled. AUX: auxiliary circuits; SC & INV: switched capacitor and inverter.

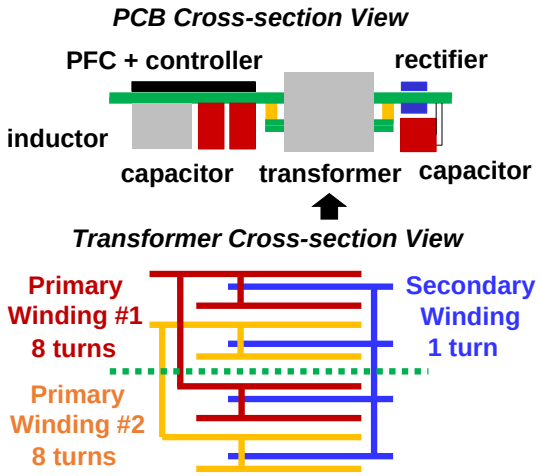

Fig. 16. Cross-section view of the PCB embedded transformer and the prototype Multitrack PFC converter.

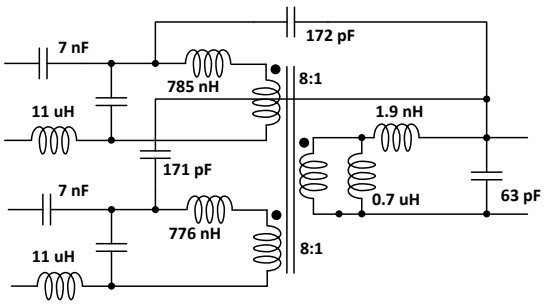

Fig. 17. Lumped circuit model of the PCB planar transformer with two primary windings and one secondary winding [13].

with GaN switches (GaN Systems and EPC), gate drives, analog control logic and other auxiliary circuits. A TI Piccolo F28069 microcontroller was utilized for voltage regulation, grid synchronization, startup control, and mode switching. Fig. 14 shows a picture of the prototype. The prototype achieves a power density of 50W/inch^3 with universal ac input voltage and isolated 12V$_{\rm DC}$ output voltage. Fig. 15 shows the general component layout of the printed-circuit-board. The area occupied by the high frequency ZVS control circuitry can be integrated and further miniaturized to increase the power density of this system. The printed-circuit-board (PCB) transformer is implemented with a ELP30 core with 3F45 material from Ferroxcube. The electrolytic capacitors are mounted through a hole on the PCB board to minimize the overall system height (1cm as set by the electrolytic capacitor). Figs. 16-17 show the cross-section of the prototype and lumped circuit model of the PCB embedded transformer. Two 11μH inductors are connected in series with the two primary windings of the transformer to assist in ZVS.

The parasitic capacitance of the transformer impacts the operation of the isolation stage through common-mode current injection at the switching frequency [1]. In a planar transformer, splitting a winding with a high number of turns into multiple windings with lower number of turns can reduce the common-mode current injection [13]. Due to the existence of the energy buffering capacitor C_B, the parasitic capacitance has no impact on the operation of the PFC stage.

Figs. 18-20 shows the measured waveforms of the Multitrack PFC system with ZVS operation. With different input voltages, the system operates in different modes with different ZVS transients as described in Section III. The ZVS range is greatly extended as expected. Fig. 21-23 shows the line voltage and line current of the prototype in three different operation modes. The implemented system does not have a current sensor. A state-machine with pre-calibrated multiplier indices act as a look-up table is implemented in the microcontroller to modulate the sinusoidal input current as a part of the voltage regulation loop. Figs. 24-25 shows the ZVS operation of the merged switched capacitor circuit and the isolation-stage inverters. The PFC stage and the isolation stage operate at different frequencies. The dynamics of the PFC stage and isolation stage are decoupled by the energy buffer capacitor.

Fig. 26 shows the startup waveforms of the prototype. The start-up of the system is realized following the 4-step method described in Section V. As demonstrated, this start-up sequence can smoothly charge the energy buffer capacitor and ensure the system enters steady state operation with low inrush current. A look-up table was implemented in the microcontroller to set appropriate current modulation index and voltage thresholds during the startup process. During the startup, an auxiliary ac-dc power converter with low power rating and small size supports the operation of the control and driver circuits. After the system enters steady state operation, the control and driver circuitry are powered by an auxiliary winding on the isolation transformer. The half-bridges in the Multitrack architecture naturally refers to a few dc voltage levels. The drivers and control circuitry in each of the voltage domain can receive power from the buffer capacitor that holds the voltage for this domain without other auxiliary circuits. In the prototype design, auxiliary power for the two stacked domains are taken from C_1 and C_2, respectively. Fig. 27 shows the measured transient waveforms of the prototype with the load current stepping from 4 A to 9 A. Fig. 28 shows the measured output voltage and switch node voltage for 2.5 line cycles.

Fig. 29 shows the measured efficiency of the full PFC system from universal ac input voltage to isolated 12V$_{\rm DC}$ output voltage. The full PFC reaches a peak efficiency of 92% at around 120W with 220V$_{\rm AC}$ input voltage. The peak

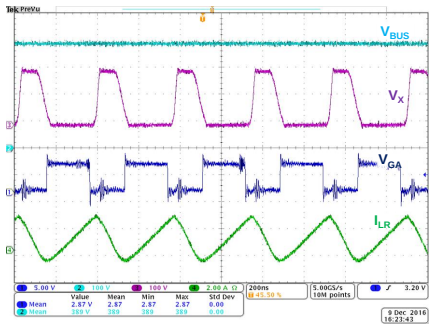

Fig. 18. ZVS waveforms with $100V_{AC}$ input and $12V_{DC}$ output at 100W.

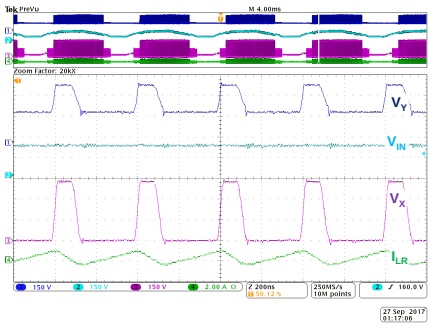

Fig. 19. ZVS waveforms with $150V_{AC}$ input and $12V_{DC}$ output at 100W.

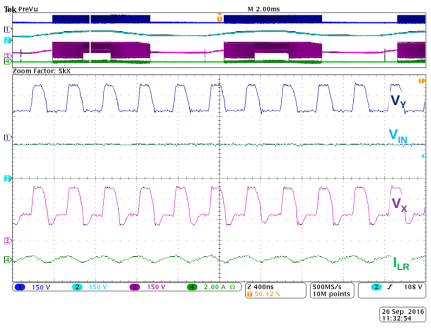

Fig. 20. ZVS waveforms with $250V_{AC}$ input and $12V_{DC}$ output at 100W.

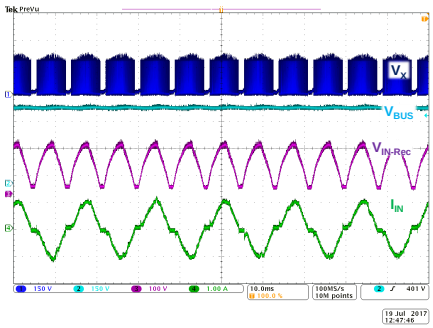

Fig. 21. Grid-interface waveforms with $140V_{AC}$ input at 50W.

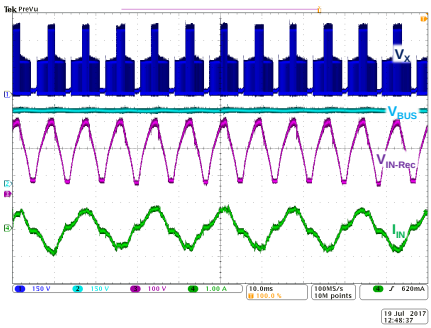

Fig. 22. Grid-interface waveforms with $220V_{AC}$ input at 100W.

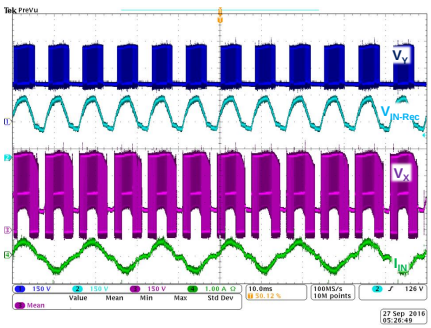

Fig. 23. Grid-interface waveforms with $250V_{AC}$ input at 120W.

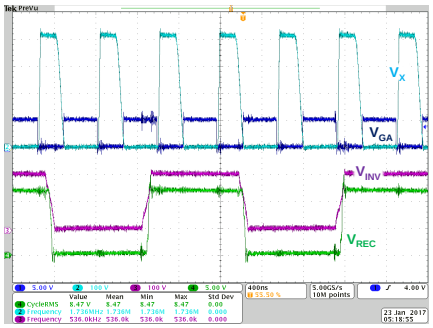

Fig. 24. ZVS of both the PFC stage and the isolation stage.

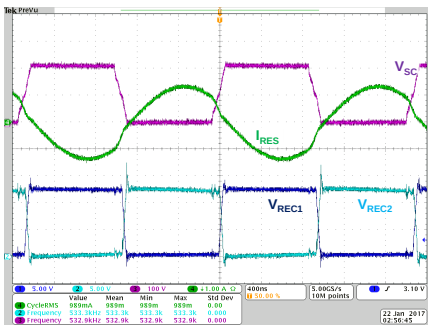

Fig. 25. ZVS of the switched capacitor circuit and the resonant current.

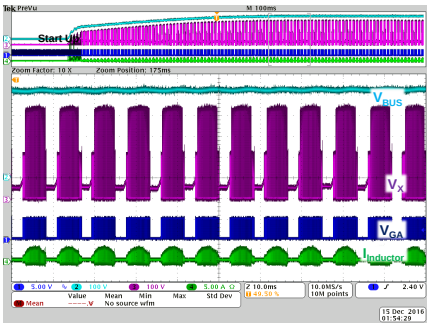

Fig. 26. Waveforms with $120V_{AC}$ input and $12V_{DC}$ output at 100W.

efficiency with $110V_{AC}$ input voltage is 90.5%. The isolation stage reaches a peak efficiency of 97% at around 150 W. In this design, we carefully optimized the system to target a power density of 50 W/in^3. Increasing the input inductor size and the transformer size and reducing the frequency would increase the efficiency, at the cost of reduced power density.

Fig. 30 shows the measured harmonic current of the prototype normalized to the limits required by EN61000-3-2:2014. The 150 W universal input PFC have the current harmonics below 65% of the standard limits and the THD is maintained below 16%. Current waveforms of the three operating conditions are shown in Fig. 21-23. The mode switching actions show up in the $3^{rd} - 9^{th}$ harmomics, depending on the operating conditions.

Fig. 31 shows the modeled loss breakdown of the Multitrack PFC as a function of the output power. When the output power is low (smaller than 50W), there is not enough current to enable the soft-switching of the switched-capacitor circuit. Thus the hard-switching loss of the hybrid switched capacitor and inverter circuit dominates the loss (over 70%). The core loss is also a major loss contributor in this regime, as expected. The difference between the modeled efficiency and the measured efficiency can be at least partially explained by the un-modeled charge-transfer loss of the switched capacitor circuit, as well as the un-modeled trace resistance on the prototype. In the medium-high power range (higher than 50W), the switched-capacitor circuit is soft-switching and the switching loss is rapidly reduced. The loss on the PFC stage becomes the major

TABLE III
PERFORMANCE COMPARISION OF MANY RECENTLY PUBLISHED PFC DESIGNS AND THE MULTITRACK PFC.

	[32]	[33]	[34]	[35]	[36]	[37]	[38]	[39]	Multitrack
Year	2014	2015	2016	2016	2017	2017	2018	2018	2018
Power	310W	400W	50W	65W	60W	600W	250W	250W	150W
Universal	Yes	Yes	No	No	Yes	Yes	Yes	Yes	Yes
Output V	28V	400V	12V	25V	12V	24V	24V	48V	12V
Output I	11.0A	1.0A	4.2A	2.6A	5.0A	25.0A	10.4A	5.2A	12.5A
Frequency	200kHz	200kHz	5MHz	1MHz	250kHz	500kHz	2MHz	500kHz	2MHz
Efficiency	93%	96%	88%	94%	92%	92%	95%	94%	92%
Density	10W/in^3	20W/in^3	50W/in^3	44W/in^3	20W/in^3	28W/in^3	35W/in^3	20W/in^3	50W/in^3
PF	99%	98%	85%	N/A	N/A	N/A	95%	99%	96%

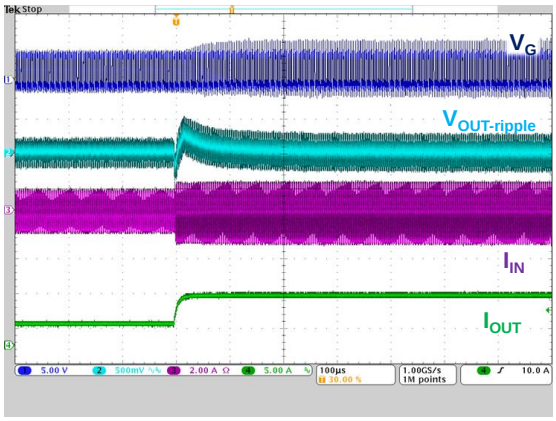

Fig. 27. Measured transient waveforms with a load current step from 4 A to 9 A. The output voltage has a peak-to-peak transient ripple of 500 mV.

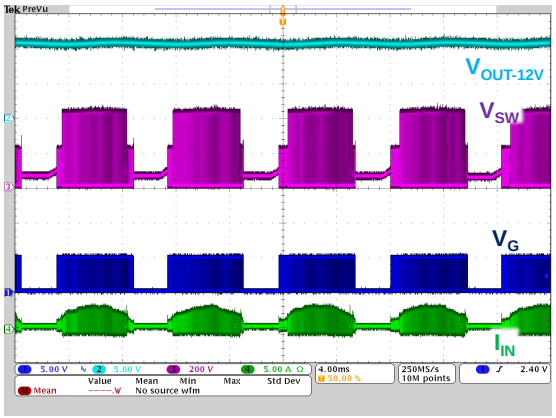

Fig. 28. Measured output voltage across the line cycle. The energy buffering capacitor C_B decouples the PFC and the isolation stage and no low frequency ripple was observed at the output.

loss in the medium power range (between 50W and 100W). This is due to the diode forward voltage drop loss of the boost diode and the conduction loss of the boost inductor. When the output power is high (higher than 100W), the conduction loss of the output rectifier starts dominating (due to the high output current). The transformer contributes about 20%–30% of the overall loss across the full power range.

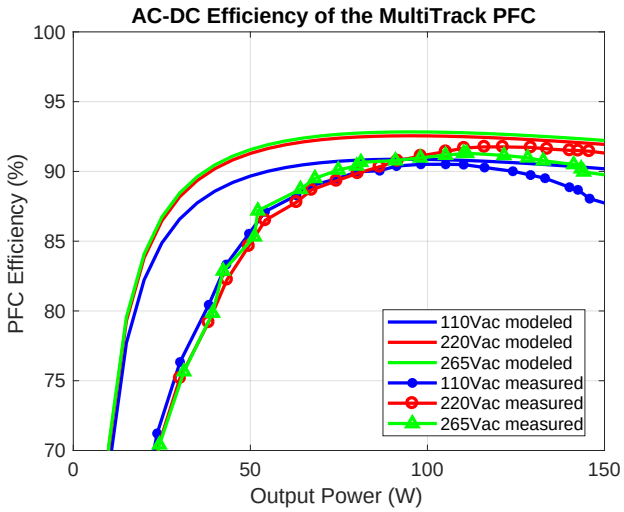

Fig. 29. Measured (circled) and modeled (solid) efficiency of the Multitrack PFC with with $110V_{AC}$ (solid), $220V_{AC}$ (circle) and $265V_{AC}$ (triangle) input and $12V_{DC}$ output.

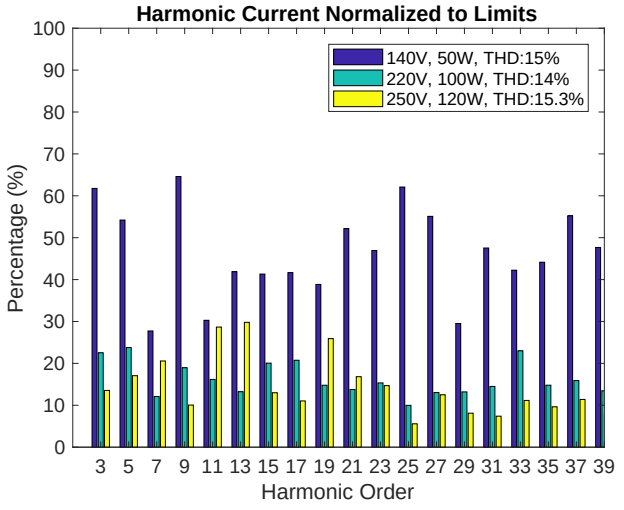

Fig. 30. Harmonic current normalized to the limits required by EN61000-3-2:2014.

VIII. CONCLUSIONS

This paper presents a Multitrack PFC architecture which offers many advantages compared to conventional PFC archi-

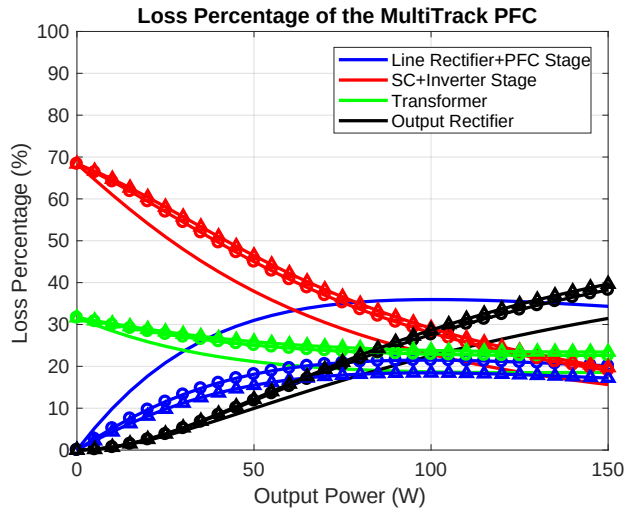

Fig. 31. Estimated loss break down of the Multitrack PFC with $110V_{AC}$ (solid), $220V_{AC}$ (circle) and $265V_{AC}$ (triangle) input and regulated $12V_{DC}$ output.

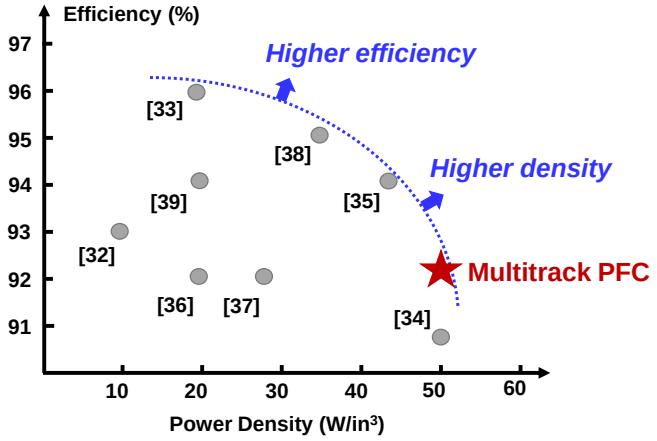

Fig. 32. Efficiency and power density of a few recent state-of-the-art PFC designs. With low output voltage (12V), and low power rating (150W), the Multitrack PFC prototype offers the highest power density ($50W/in^3$) while achieving 92% efficiency.

tectures. The Multitrack architecture leverages the advantages of switched-inductor, switched-capacitor, and magnetic isolation circuits, and gains mutual benefits from the way they are merged together by processing power in multiple voltage domains and current channels. Advanced control methodologies for maintaining ZVS across wide operation range is presented. A prototype universal ac input, 12 V_{DC} output, 150 W, 50 $W/inch^3$ PFC system was designed and tested and achieved 92% of efficiency. The concept of Multitrack PFC is applicable to a wide range of ac-dc grid interface applications targeting high efficiency and very high power density.

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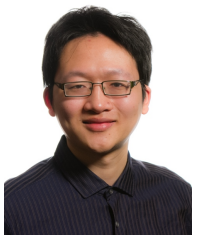

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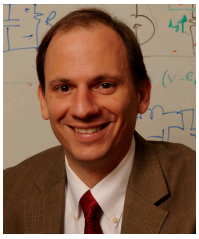

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