Design Considerations for 48-V VRM: Architecture, Magnetics, and Performance Tradeoffs

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Abstract—The energy demand of future computing gives rise to new challenges in high current voltage regulator modules (VRMs). This paper reviews the recent development in architecture and magnetics for 48-V VRMs, with a focus on achieving high efficiency, high power density, high control bandwidth, and compact system packaging. The strengths and weaknesses of many representative solutions are compared. We highlight the key opportunities and challenges and present comprehensive co-design guidelines for 48-V VRM architecture and magnetics.

Index Terms—voltage regulation module (VRM), power architecture, magnetics, packaging, switched-capacitor, transformer

I. Introduction

Voltage regulation modules (VRMs) with high efficiency, high power density, and high control bandwidth are needed to support future microprocessors [1], [2]. Figure 1 shows the principles a future vision where the VRM can be embedded between the motherboard and the microprocessor. Figure 2 shows data on 50 years of microprocessor development highlighting the rapid growth in power demand [3]. As Moore's Law and Dennard Scaling approach to the end [4]–[6], future computers comprise many large-scale microprocessors near each other with high speed data link. Holistic innovations in architecture, magnetics, packaging, and control are needed to improve the efficiency and power density of VRMs [7], [8].

One emerging trend in point-of-load power delivery is to feed the low-voltage high-current processors (e.g., <1-V, >500-A) with high voltage (e.g., 48-V) from the computer racks to leverage the existing telecom power ecosystems [9], [10]. Multiphase interleaved buck converter is one of the most widely adopted 12-V VRM solutions [2]. However, with the input voltage increasing to 48-V, it can no longer offer satisfactory efficiency, power density, or control bandwidth. Various topologies for high voltage conversion ratio high current VRM applications have been proposed, including hybrid-switched-capacitor-based designs [11]–[20], transformer-based designs [21]–[23], multicell multi-stage designs [24]–[26]. Delivering massive current to a constrained space, the power converters need to be co-designed with the packaging with thorough power integrity and signal integrity considerations.

Figure 3 listed the important milestones for the 48-V VRM. The recent demand of 48-V VRM architecture was triggered from 2012 by the adoption of the classic 48-V voltage bus from telecom standards. In 2016, Google's 48-V architecture was announced, followed by the disclosure of the switch-tank-converter [12] as a representation of the early exploration of the hybrid switched capacitor approach. Later, STMicro [27],
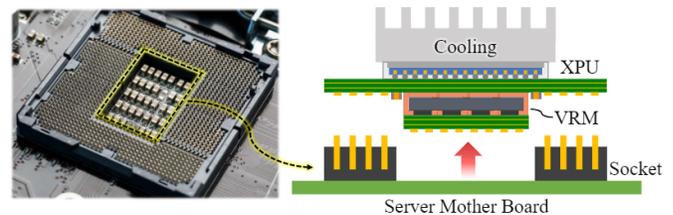

Fig. 1. Ultra-thin VRM embedded in microprocessors packaging for extreme efficiency, density, and control bandwidth.
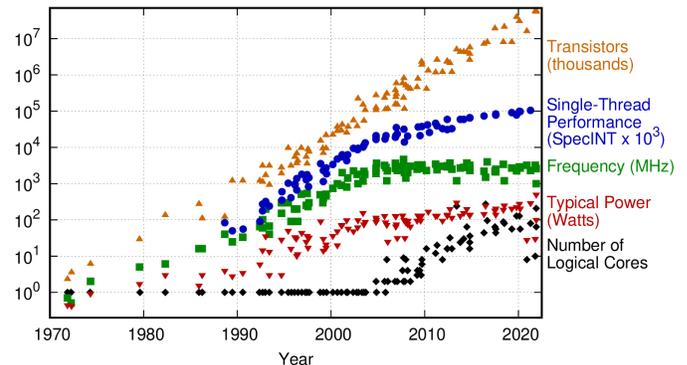

Fig. 2. 50 years of microprocessor trend data [3]. Microprocessors consume more power in a large die area with billions of transistors. The number of cores increases together with the thermal determined power (TDP) per core.

Analog Devices [28], Texas Instruments [29], MPS [30], Infineon [31] also released 48-V VRM solutions, followed by the launching of the Power Stamp Alliance [32]. In 2018, Nvidia's 48-V GPU (DGX-2), with Vicor's two-stage solution motivated extreme performance and miniaturized size. Intermediate bus solutions other than 12-V are emerging [16], [25], [30]. In most of these designs, magnetic components are limiting the system size, efficiency, and control bandwidth. Coupled inductors [33]–[37], together with the Trans-inductor Voltage Regulator (TLVR) concept [38], were gradually adopted to achieve fast transient while improving efficiency and power density. Since 2021, with the annocuement of Intel PowerVia [39] and Tesla Dojo [40], 2.5D/3D packaging and vertical power delivery are becoming the next focuses. The current area density of 48-V VRMs is about 1-A/mm^2, while peak current area density is about 5-A/mm^2 [4], [5], [24], [41].

This paper reviews the recent development in architecture and magnetics for 48-V voltage regulation modules, with a focus on highlighting the strengths and limitations of various options and providing comprehensive design guidelines.
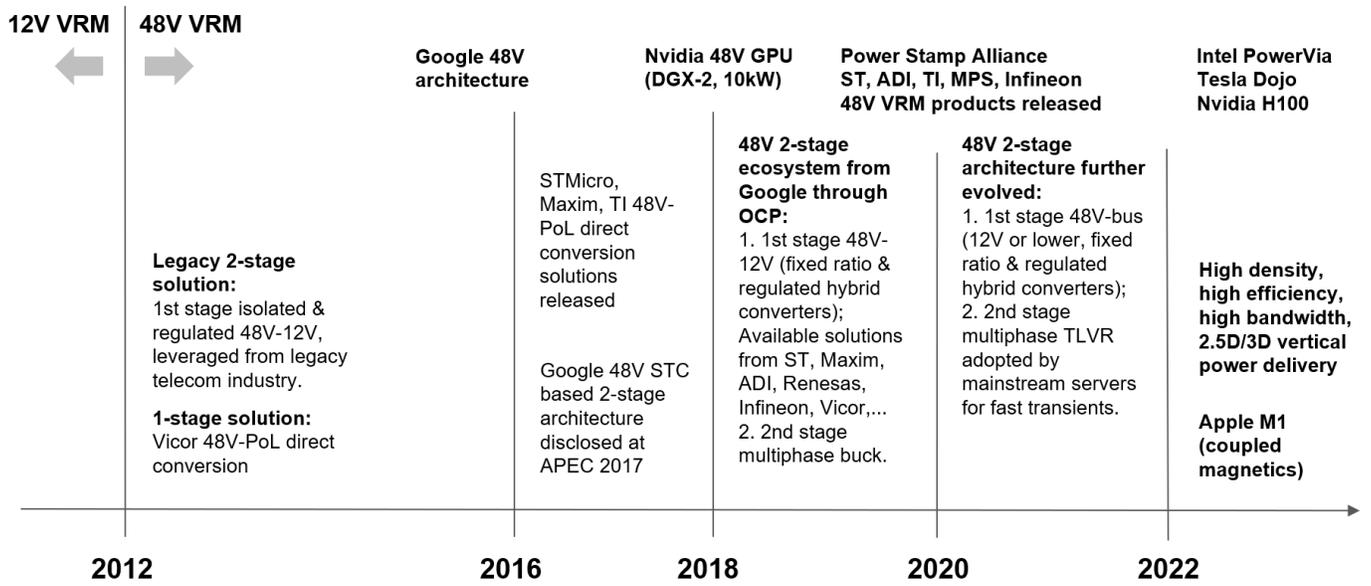
Fig. 3. Important industry milestones for the 48-V VRM development. The announcement of the Google's data center 48-V architecture and Nvidia's high power 48-V GPU are two key industry milestones to drive the development of the 48-V VRM ecosystem.

II. ARCHITECTURE CONSIDERATIONS FOR 48-V VRM

Many factors need to be considered when designing 48-V VRMs, including area, efficiency, height, control bandwidth, thermal, signal integrity, and power integrity. Different architectures offer different options when making performance tradeoffs. There are four major design choices when selecting the power conversion architectures for 48-V VRMs:

- **Number of stages: single-stage or multi-stage?** For multistage designs, the classic two-stage intermediate bus architecture (IBA) uses 12-V as the intermediate voltage bus. 24-V, 8-V, 6-V, and 4-V are all emerging options.
- **Energy transfer mechanism: capacitor-based, inductor-based, or transformer-based?** Switched-capacitor-based topologies have the potential to achieve high power density; switched-inductor-based topologies have mature control models and offer superior transient performance; transformer-based topologies have the lowest stress on semiconductor devices.
- **Operation waveform: PWM or resonant?** Some topologies operate in pulse-width-modulation (PWM) with energy processed as pulsed square wave, and other topologies operate in resonant with energy in sinusoidal or piece-wise sinusoidal. PWM topologies tend to be more widely used with more mature control solutions; resonant topologies offer soft-switching opportunities and can achieve higher energy efficiency.
- **Regulation mechanism: current source or voltage source output?** Sometimes the VRM needs to perform dynamic voltage scaling. Sometimes the VRM needs to behave as a fast current source to maintain small voltage ripple. The current control functions can be performed close to the input, in the middle, or near the output of the VRM system. One can also parallel a current regulation converter with a dc voltage transformer.

All these options require holistic design considerations. Many factors may co-exist and co-impact the system's performance. Combining many circuit cells and merging their strengths enables new opportunities to achieve high efficiency, high power density, and high control bandwidth, with higher component count and potentially higher cost.

A. Single-Stage Power Architecture

We define a *single-stage* power conversion architecture as one with (1) all switches operate at a single frequency; and (2) all the non-input/output passive components process energy in similar ways with similar duty cycles. They are building blocks for more complicated systems. Figure 4 shows four example single-stage topologies, including: (a) multiphase buck family [2]; (b) transformer-based family [21], [42] (e.g., LLC, Forward, DFX, DAB); (c) series-capacitor buck family [18], [44], [45]; and (d) switch-tank family [13], [43], [46]:

1) **Multiphase buck and other PWM converters** are the most well-understood and widely used building blocks for many composite topologies. It offers simple implementation and can be controlled by mature methods, but suffers high power conversion stress and narrow duty ratio.
2) **Transformer-based topologies** rely on turns ratio and flux distribution to realize voltage conversion. The parasitic components of the circuits can often be absorbed into circuit operation to reduce the loss. However, transformer-based topologies usually have more complicated control dynamics than PWM topologies.
3) **Single stage hybrid PWM converters**, such as the series-capacitor buck converter, load the switched-capacitor cells with an inductor to create a current source output. The regulation of the inductor current is achieved by adjusting the duty ratios. One limitation of series-capacitor buck converters is the segmented duty ratio regions which add more complexity to system control.

(a) Multiphase Buck / PWM

(b) Transformer-based Resonant / PWM

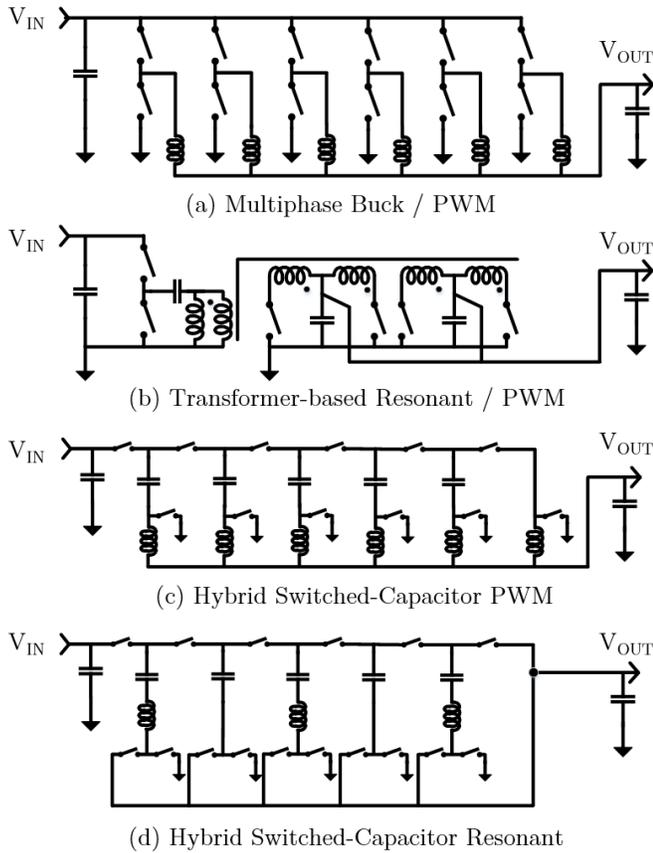(c) Hybrid Switched-Capacitor PWM

(d) Hybrid Switched-Capacitor Resonant

Fig. 4. Four single-stage topologies for 48-V to 1-V VRM: (a) Multiphase buck/PWM converter [2]; (b) Transformer-based converter (LLC, Forward, DFX, DAB) [42]; (c) Series-capacitor buck converter [18]; (d) Switch-tank converter [43]. The unit cells of these topologies can be used as building blocks to synthesize more complicated topologies.

4) **Single stage hybrid resonant converters**, such as the switch-tank converter. Many inductor-capacitor resonant tanks are configured in a way such that energy is transferred between them in a resonant manner with very low loss. Similar to transformer-based resonant topologies, switch-tank converters are also usually non-regulated.

B. Multi-Stage Power Architecture

We define a *multi-stage* architecture as one that (1) has multiple standalone "single-stage" units. The frequency, duty ratio, and other mechanisms of different stages are not coupled and can be freely adjusted; (2) has one or more dc intermediate voltage buses with large decoupling capacitors and small voltage ripple. In a multi-stage design, regulation is usually performed by one stage and other stages only function as dc transformers (DCXs) for voltage conversion. Figure 5 shows three example two-stage solutions for 48-V VRM, including:

1) **A regulation stage followed by a transformer-based current multiplier**, such as the fractional power architecture (FPA) developed by Vicor [47]. By moving the regulation stage to the front, the regulation module can be placed at any location on the motherboard while the critical current delivery module can be placed very close.

(a) PWM + Transformer-based

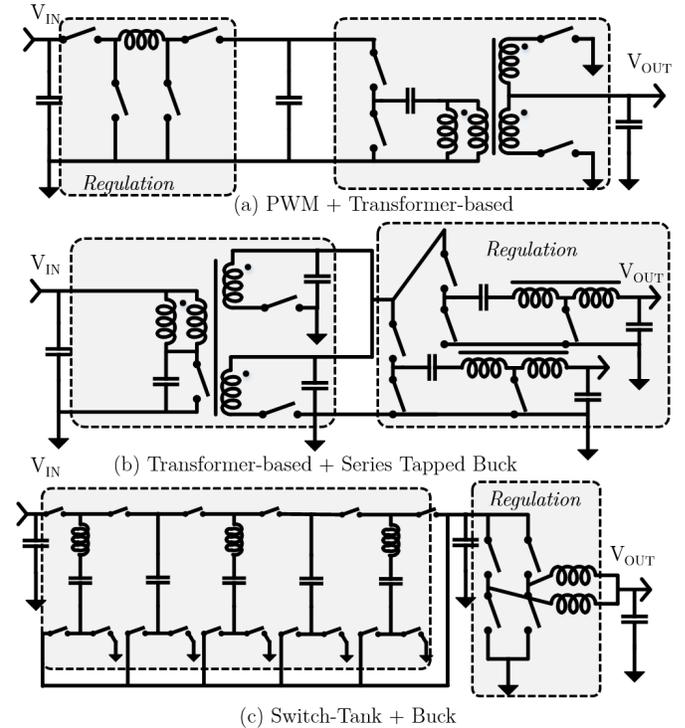(b) Transformer-based + Series Tapped Buck

(c) Switch-Tank + Buck

Fig. 5. Three two-stage topologies with an intermediate voltage bus: (1) A 1:1 buck-boost regulation stage followed by a 48:1 dc transformer [47] with inductors at the front; (2) A 12:1 minimum-switch DPX architecture [48] followed by a two-phase series tapped buck converter with tapped inductors [49]; (3) A 6:1 switch-tank converter followed by an 8:1 multiphase buck [43], [50] with inductors in the middle and at the end.

2) **A transformer-based DCX followed by a PWM regulation stage**, such as the DPX architecture developed by Differential Power SL [48]. A novel transformer-based DCX topology with a very low component count was developed to leverage the recent development of wide-bandgap (WBG) devices in blocking high voltage with a low duty ratio and features a new segmented transformer technology to handle the very high output current.

3) **A switch-capacitor DCX followed by a PWM regulation stage**, such as the Google 48-V power architecture [43], [50]. The switched capacitor stage can be implemented in many different ways including charge pumps or resonant switched capacitor circuits. The regulation stage can be implemented as three-level buck or flying capacitor multilevel converters (FCMLs), and can be integrated on-chip [51] with low voltage rating devices.

C. Stacked and Crosslinked Power Architecture

A third way to interface with the high input voltage (e.g., 48-V) with low voltage rating devices is to stack multiple power conversion cells. Figure 6 shows a few examples of stacked and crosslinked power architecture with different building blocks. These conversion cells can be stacked series-capacitor buck converters [19], Dickson converters [52], FCML converters [53], LLC converters [54], and resonant switched-capacitor converters [55]. The operation of all switches in a stacked and crosslinked topology is usually coordinated.
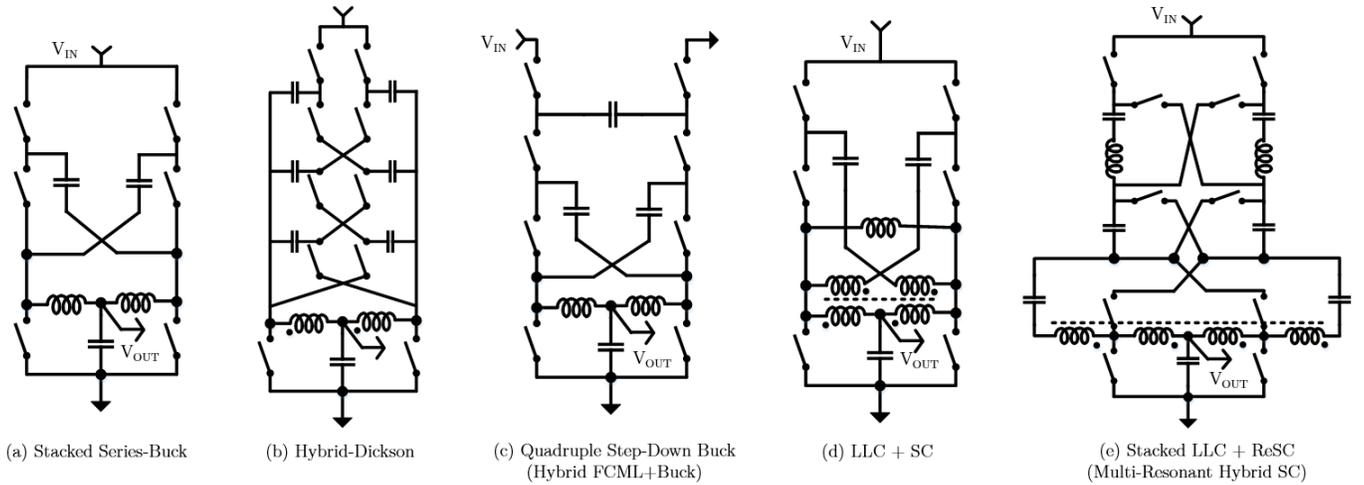
Fig. 6. Stacked and crosslinked power architecture: (a) crosslinked series-buck converter [18], [19]; (b) crosslinked Dickson converter [52]; (c) crosslinked FCML and buck converter [53]; (d) crosslinked LLC converter [54]; and (e) crosslinked LLC and resonant switched capacitor converter [55]. These converters can be designed as a single-stage solution for 48-V-1V conversion, or be included as a part of a multi-stage solution to create an intermediate bus voltage.

D. Cascaded Architecture with Virtual Intermediate Bus

We define a *virtual intermediate bus* architecture as one that (1) has multiple merged "single-stage" units whose operations need to be synchronized; (2) does not have obvious dc intermediate voltage buses or large decoupling capacitors. The virtual intermediate bus approach is usually used to merge a switched-capacitor stage with a switched-inductor stage to enable soft-charging of the switched capacitors [11], [14], so that smaller capacitors and lower switching frequencies can be used, leading to higher efficiency and power density. Figure 7 shows four example virtual intermediate bus solutions for 48-V to 1-V VRM, including:

1) A merged-multi-stage structure with a 2:1 charge pump as the dc transformer and a multiphase buck converter as the regulation stage [56], [57].
2) A virtual-intermediate-bus (VIB) architecture with a 2:1 charge pump as the first stage and a higher order series-capacitor buck converter as the regulation stage [25].
3) A multistack switched-capacitor (MSC) architecture with a stackable 2:1 charge-distributor as the first stage and a higher order series-capacitor converter buck as the regulation stage [58] .

The drawbacks of the virtual intermediate bus approach include (1) increased voltage stress on many switches due to the larger intermediate bus voltage ripple; (2) the circuit cells that interface with the virtual intermediate bus need to reject significant dynamic voltage ripple; (3) the soft charging current loops are usually long with non-negligible parasitic inductance and $\frac{1}{2}LI^2$ switching loss [25], which motivates transformer-based or hybrid resonant topologies with zero-current-switching (ZCS) opportunities [16], [21], [59], [60].

E. Sigma / Series-Input Parallel-Output Architecture

A series-input parallel-output architecture allows different transistors and passive components to be used for different purposes, maximizing the design flexibility with optimized efficiency, power density, and control bandwidth.
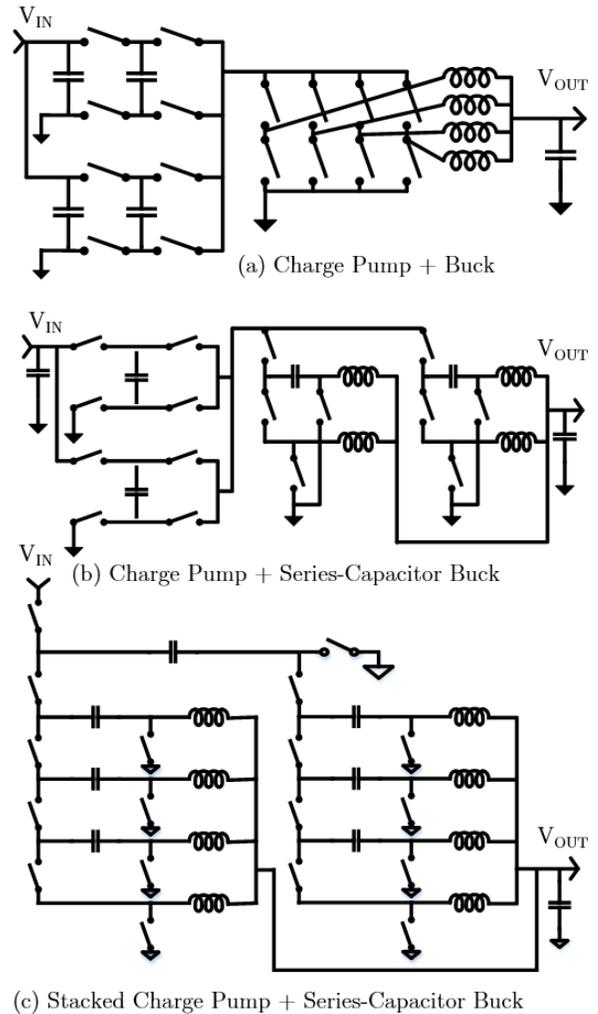

Fig. 7. Three two-stage topologies with virtual intermediate voltage buses: (1) A charge pump stage followed by a multiphase buck converter [56], [57]; (2) A pair of 2:1 charge pump stage followed by two 24:1 series-capacitor buck converters [25]; (3) Stacked charge-distributor / Dickson followed by series-capacitor buck converters [58], [61].
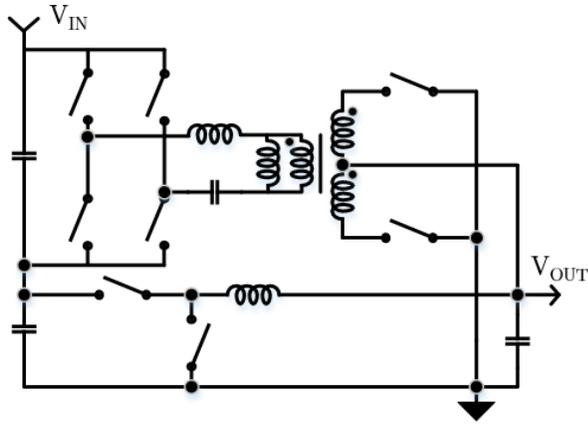
Fig. 8. LEGO-PoL composite power architecture with switch-tank front-end and multiphase-buck regulation stage [41].
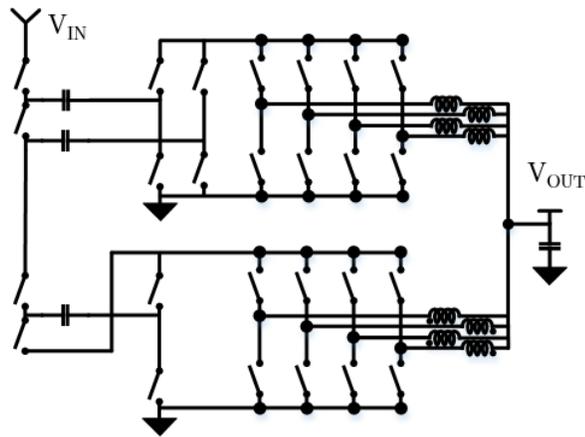

Fig. 9. LEGO-PoL composite power architecture with switch-tank front-end and multiphase-buck regulation stage [24].
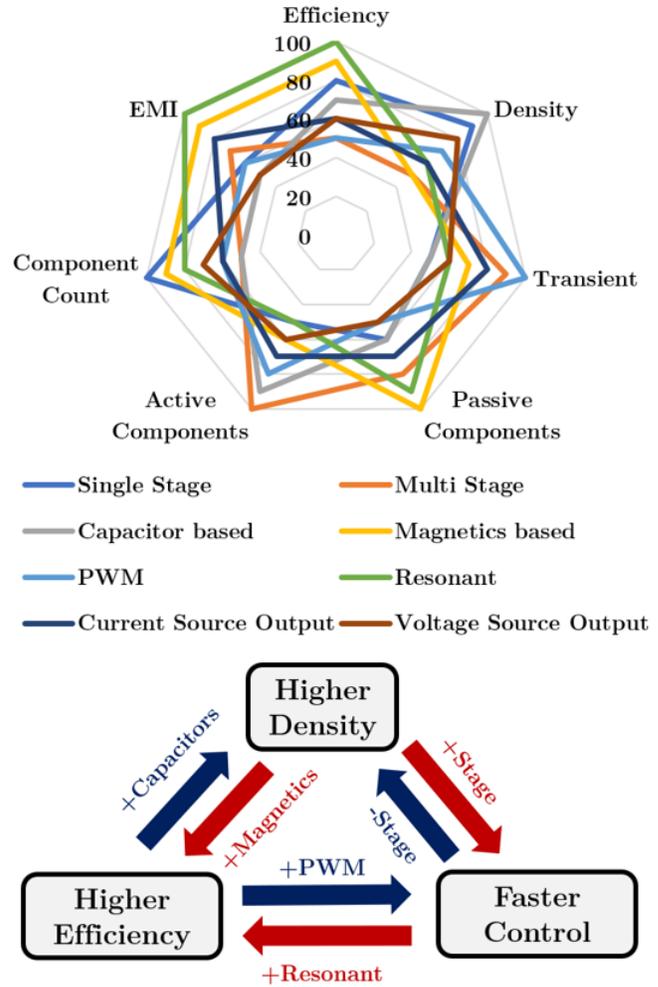

Fig. 10. Design guidelines for 48-V to 1-V VRM (efficiency, density, bandwidth) and six major design options (switched-cap, transformer, single-stage, multi-stage, resonant, PWM) with performance tradeoffs. Adding more capacitive energy transfer and reducing the number of stages tend to increase power density; Adopting more magnetic energy transfer and more resonant mechanism tend to increase efficiency; Increasing the number of stages and operate more stages in PWM tend to improve the control bandwidth.

The Sigma converter [41] is a quasi-parallel converter that connects two converters in series on the input side, and in parallel on the output side. One of the converters is an unregulated isolated dc transformer that carries the bulk power, and the other is a nonisolated converter responsible for regulating the output voltage with fast di/dt capability.

The LEGO-PoL converter [24] is a series-input parallel-output converter that uses series stacked switched capacitor cells for dividing the input voltage and parallel multiphase buck converters for sharing the output current. LEGO-PoL architecture features (1) complete soft charging of the switched-capacitor stage for high efficiency and high power density; (2) complete di/dt capability across the full current range; (3) automatic voltage balancing and current sharing among switching modules; and (4) scalable voltage and current rating for higher output power.

F. Architecture Selection and Performance Tradeoffs

A 48-V VRM design may need to be optimized for efficiency, power density, and control bandwidth. A design option that improves one design target may improve or reduce other aspects. Different applications place different priorities

in different targets. Multiple design options may co-exist in multiple stages of the power converter. Figure 10 summarizes the general design considerations for 48-V VRM.

1) The **number of power conversion stages** has a strong impact on the performance tradeoff between power density and transient speed. Leveraging the lower component count, single-stage designs can usually achieve higher density than multi-stage designs. However, multi-stage designs allow a part of the system to operate at frequencies that are much higher than others, increasing the control bandwidth. Merged-multi-stage designs offer new opportunities for balancing power density and transient performance with increased complexity.

2) The **energy transfer mechanism of each stage** determines the efficiency and power density tradeoff. In general, transformer-based designs have the potential to achieve high efficiency and switched capacitor-based designs have the potential to achieve high power density.
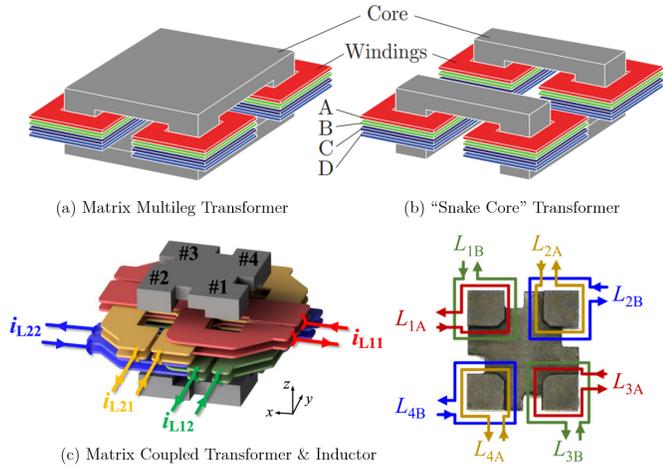
(a) Matrix Multileg Transformer

(b) "Snake Core" Transformer

(c) Matrix Coupled Transformer & Inductor

Fig. 11. Example implementation of the matrix coupled transformers and inductors, including: (a) matrix multileg transformer [22], [41]; (b) "Snake Core" transformer [68]; and (c) matrix coupled SEPIC inductors [58].

(a) Vertical Coupled Magnetics

(b) Planar Coupled Magnetics
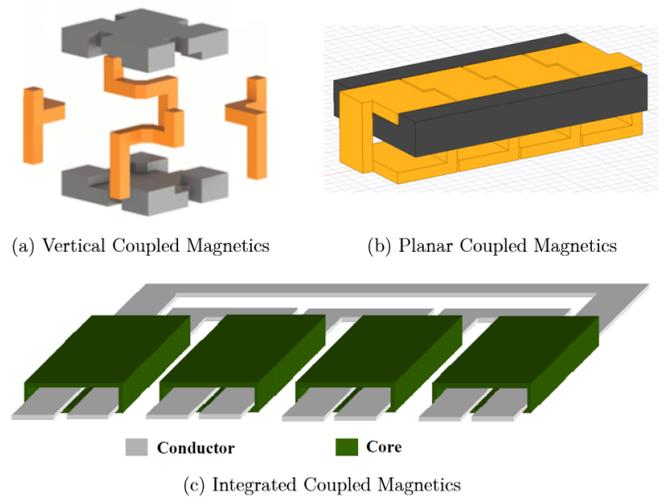
(c) Integrated Coupled Magnetics

Fig. 12. Example implementation of the multiphase coupled inductors: (a) vertical coupled inductor [24]; (b) planar coupled inductor [37]; and (c) integrated coupled inductor [75].

Switched-capacitor circuits can be designed as less dense and more efficient if large capacitors are used (with lower charge sharing loss), or if magnetic components are included for soft switching or soft charging. Transformer-based designs require good magnetic coupling to achieve high performance. The availability of high permeability, low-loss magnetic materials may limit the highest frequency that a transformer-based design can achieve. The energy storage density of magnetic components is usually lower than capacitors [62]. However, magnetic components are usually deep-cycled in typical power converter design. The performance metrics of magnetic components increase as their physical size increases, making small and efficient power inductors rare [63].

3) **How the converter is operated – resonant or PWM** – impacts the tradeoff between efficiency and transient performance. Resonant circuit topologies usually can achieve higher efficiency due to the zero-voltage and zero-current switching opportunities, at the cost of higher control complexity for fast and precise regulation. The electromagnetic interference (EMI) performance of resonant topologies is usually better. Control strategies for classic PWM topologies have been well explored, while control strategies for many resonant, hybrid, and coupled inductor topologies are still limited [64]–[67].

III. HIGH VOLTAGE CONVERSION RATIO TRANSFORMERS

Transformer-based circuit topologies, such as LLC converter, dual-active-bridge (DAB) converter, and phase-shift full bridge (PSFB) converters, have been widely used in high voltage conversion ratio dc-dc applications. Transformer-based designs leverage the low component count of inverter and rectifier circuits, and can offer low device stress [69], [70]. The following techniques can be applied to achieve a high voltage conversion ratio through a transformer-based design:

1) **Primary-series secondary-parallel:** A well coupled primary-secondary winding pair shares the same dv/dt per turn for all windings. One can split a high turns ratio transformer into multiple lower turns ratio transformers with the primary side connected in series and the secondary side connected in parallel, and explore opportunities to merge the magnetic core and share the flux path [68], [71], [72].

2) **Segmented flux:** Most VRM secondary windings are single turn. Distributing the central flux into multiple parallel paths can extend the voltage conversion ratio. Splitting the magnetic flux reduces the $d\Phi/dt$ and reduces the volt-per-tern, allowing lower voltage to be achieved on the rectifiers. The split flux concept is well illustrated by the matrix [22] and VIRT [73] structures.

3) **Winding placement:** Minimizing the leakage inductance is critical to improving the performance of 48-V VRM when the output current is very high. Compact packaging of windings can reduce the leakage inductance [48].

4) **Merged multi-transformer configuration:** Merging many magnetic components into one often creates opportunities for improved magnetic performance [63]. Similar to buck or other PWM converters, transformer-based topologies can also benefit from multiphase interleaving at the cost of increased component count [74].

IV. MULTIPHASE COUPLED INDUCTORS

Low current ripple and fast transient cannot be achieved simultaneously with discrete inductors. Discrete inductors suffer very high static $\frac{1}{2}LI^2$ energy storage when the output current is very high with a small current ripple. This static energy storage necessitates higher core volume and reduces the system's transient speed. Multiphase coupled inductors, capable of reducing the dc flux in the magnetic core and greatly improving the transient performance, is a natural fit for high-performance miniaturized VRMs [37], [89], [90]. Multiphase coupled inductors are compatible with a wide range of multiphase buck and PWM operated hybrid-switched-capacitor circuits [24], [55], [58], [74], and can be imple-

TABLE I
PERFORMANCE COMPARISON OF A FEW RECENT 48 V TO 1 V POINT-OF-LOAD VRM DESIGNS

Year	Note	Output Current	Box Power Density‡	Current Area Density	Peak Efficiency	Full Load Efficiency	Switching Frequency‡	Including Gate Drive Loss	Including Gate Drive Size
2017	TI [76]	50 A	129 W/in^3	0.079 A/mm^2	90.7%	87.7%	600 kHz	Yes	Yes
2019	MP-MIH [77]	40 A	83 W/in^3	0.044 A/mm^2	92.1%	80.4%	300 kHz	No	No
2020	QSD-Buck [78]	40 A	31 W/in^3	0.024 A/mm^2	94.5%	91.1%	125 kHz	No	Yes
2020	MLB-PoL [79]	65 A	198 W/in^3	0.122 A/mm^2	91.5%	86.4%	250 kHz	Yes	Yes
2020	Bel Power [80]	70 A	167 W/in^3	0.184 A/mm^2	91.6%	90.5%	242 kHz	Yes	Yes
2020	Sigma [41]	80 A	420 W/in^3	0.127 A/mm^2	94.0%	92.5%	600 kHz	No	Yes
2020	TSAB [81]	90 A	36 W/in^3	0.023 A/mm^2	91.5%	85.0%	500 kHz	No	Yes
2020	Hybrid FCB† [50]	200 A	153 W/in^3	0.036 A/mm^2	91.4%	88.6%	205 kHz	No	Yes
2020	Vicor [82], [83]	214 A	400 W/in^3	0.202 A/mm^2	90.1%	N/A	1025 kHz	Yes	Yes
2021	On-Chip [84]	8 A	198 W/in^3	0.031 A/mm^2	90.2%	76%	2500 kHz	Yes	Yes
2021	ADI [85]	50 A	89 W/in^3	0.064 A/mm^2	90.8%	88.1%	350 kHz	Yes	Yes
2021	24 V VIB [86]	450 A	325 W/in^3	0.219 A/mm^2	95.2%	89.1%	417 kHz	No	No
2022	Symmetric DIH [87]	105 A	598 W/in^3	0.131 A/mm^2	83.5%	71.5%	750 kHz	No	Yes
2022	Dickson Squared [88]	270 A	360 W/in^3	0.142 A/mm^2	93.8%	88.4%	280 kHz	No	Yes
2022	LEGO-PoL [24]	450 A	577 W/in^3 294 W/in^3	0.587 A/mm^2 0.298 A/mm^2	91.1% 88.4%	85.7% 84.8%	1000 kHz	No Yes	No Yes

† The power density is calculated with the box volume (maximum length × width × height) of the prototype, including the gate drive and auxiliary circuitry.
‡ The switching frequency of the voltage regulation stage.

mented in many different ways (Fig. 12). The multiphase coupled inductors may resonate with the switched capacitors in hybrid-switched-capacitor coupled inductor circuits [67]. A coupled inductor is sensitive to phase current imbalance. As a result, topologies with automatic current sharing capabilities are sometimes preferable [25]. The following step-by-step method can be used to design multiphase coupled inductors:

1) **Step #1: Determine the number of phases** based on the circuit topology, the load current, the ripple reduction target, and the device current rating.
2) **Step #2: Determine the maximum required phase leakage inductance** based on the number of phases, the targeted di/dt. A higher number of phases and a smaller leakage inductance lead to faster di/dt.
3) **Step #3: Determine the required coupling coefficient** based on the acceptable phase current ripple. A higher coupling coefficient and a larger number of phases lead to lower phase current ripple.
4) **Step #4: Design a magnetic structure** with appropriate shared and independent reluctance paths to achieve the target phase leakage inductance and coupling coefficient, while minimizing the core loss.
5) **Step #5: Optimize the winding configuration** to minimize the dc resistance and ac resistance.
6) **Step #6: Verify the flux density and saturation limits** by simulating the core with phase current mismatch.
7) **Step #7: Fine tune the core structure**. Increasing the leakage inductance can make the core more robust against saturation and reduce the di/dt. Increasing the coupling coefficient reduces the current ripple but may lead to larger core volume and higher core loss.

V. VERTICAL POWER DELIVERY

The power density of a VRM needs to be higher than the power density of processors for vertical power delivery. Higher power density further stresses the importance of high energy efficiency and thermal management. The current area density of microprocessors is approaching 5-A/mm^2, while the current area density of 48-V VRM is still far behind (close to 1-A/mm^2). The limiting factors for achieving higher area current density range from devices and circuits, to packaging [1]. On the device level, the performance of low voltage silicon MOSFETs [7] still cannot meet the demand of future computing. GaN-based technologies are emerging [91]. The miniaturization of discrete, in-package, and integrated magnetics is still limited by material characteristics [36]. On the circuit level, series-input parallel-output composite/sigma architectures [24], [41] and multilevel multiphase flying capacitor architectures are rapidly improving [67]. However, they still require thorough investigation on startup, protection, regulation, voltage and current balancing, and fast transient control. Advanced control algorithms are needed to fully exploit the strengths of the emerging circuit topologies. Power/signal integrity and EMI issues are still unexplored for most solutions.

VI. CONCLUSIONS

This paper presents a comprehensive review and discussion on the recent development of architecture and magnetics for 48-V VRM. We grouped the typical architectures into a few categories according to their main operation mechanisms and compared their strengths and weaknesses. Design guidelines for achieving high performance with proper architecture selection and magnetics integration are streamlined.

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