Virtual Intermediate Bus CPU Voltage Regulator

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***Abstract*—This paper presents a merged-two-stage 48 V–1 V point-of-load (PoL) architecture with a 24 V virtual intermediate bus (VIB) for CPU voltage regulator applications. The VIB-PoL architecture includes two power conversion stages linked by a 24 V virtual intermediate bus with significant voltage ripple. The first stage is a 2:1 interleaved charge pump which converts 48 V to 24 V. The second stage comprises multiple interleaved 4-level series-capacitor buck modules with coupled inductors, converting 24 V to regulated 1 V with an equivalent voltage conversion ratio of 6:1. The VIB-PoL architecture achieves high efficiency and high power density by reducing the power conversion stress of both stages and eliminating the intermediate bus capacitors. A 48 V–1 V 640 A CPU voltage regulator with a peak power stage efficiency of 95.2% (93.3% including gate driver loss), a full load efficiency of 84.4% (83.1% including gate driver loss) and a power density of 463 W/in^3 (at 1 V output with liquid cooling) is built and tested to demonstrate the VIB-PoL architecture.**

***Index Terms*—DC-DC, point-of-load, switched-capacitor converter, coupled inductor, voltage regulator.**

I. Introduction

THE energy consumption of modern data centers continues to grow with increasing demands for computing and communication. High efficiency and high power density are needed in nearly all types of power electronics. Modern high performance microprocessors (e.g., CPUs, GPUs, TPUs) operate at few GHz and consume hundreds of amperes of current at very low voltage (i.e., $\leq$1 V). Delivering power at 48 V is an emerging trend in future data centers with the benefits of reduced distribution loss and the possibility of leveraging the existing 48 V telecom ecosystems [1].

One challenge of 48 V point-of-load power conversion is to address the high input voltage stress and the high output current stress. Typical solutions include: a) using a transformer with high turns ratio; b) using flying capacitors to provide large voltage conversion ratio; c) cascading multiple stages with series input and parallel output; d) a combination of the above three methods. Single-stage architectures [2]–[6] usually adopt (a) and (b), in which the voltage stress and current stress are transferred from semiconductor devices to passive components (magnetics and capacitors). They are attractive for applications that require a low component count. In a two-stage design [7]–[14], the first stage interfaces with the high input voltage and provides a fixed voltage conversion ratio. The second stage is usually implemented as a multi-phase buck voltage regulator module (VRM) to manage the rapid load current step. There are also 48 V PoL topologies which have a pre-regulation stage and a second stage functioning as a dc transformer (DCX) [15]–[17]. Two-stage architectures decouple the design challenges for voltage conversion and control functions such as precise voltage regulation and fast response.

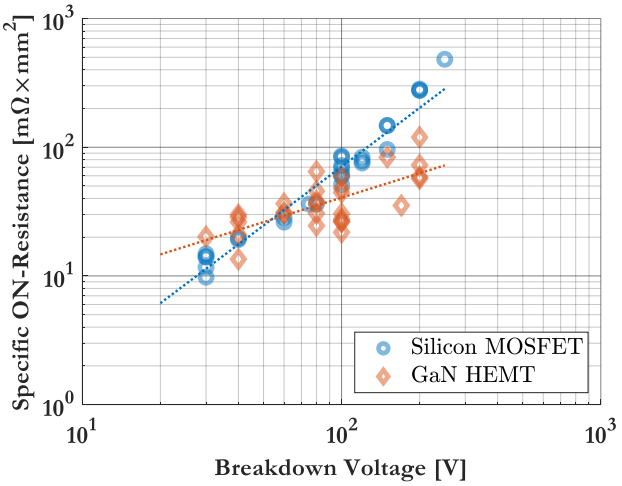

Fig. 1. Specific on-resistance of example N-channel silicon MOSFET bare die products [20] and GaN HEMTs [21].

In most typical two-stage 48 V solutions, a 48 V–12 V unregulated DCX is placed between the 48 V bus and the 12 V buck VRMs [8]–[11]. Recently, there is a trend to reduce the intermediate bus voltage of two-stage 48 V PoL converters [12]–[14]. Lower intermediate bus voltage allows the use of semiconductor devices with lower breakdown voltages that have reduced on-resistance and switching losses [18], [19]. Figure 1 shows the specific on-resistance of a group of N-channel silicon MOSFET bare die and GaN HEMTs [20], [21]. The specific on-resistance is defined as the product of the switch's on-resistance and the die area. The device with lower breakdown voltage has lower specific on-resistance, which means higher current capacity for the same die area. Lower bus voltage also enables higher switching frequency to further reduce the size of passive components and improve the transient response of the VRMs and potentially enable fully VRM integration such as Intel's Fully Integrated Voltage Regulators (FIVR) [22].

This paper presents a *Virtual Intermediate Bus Point-of-*

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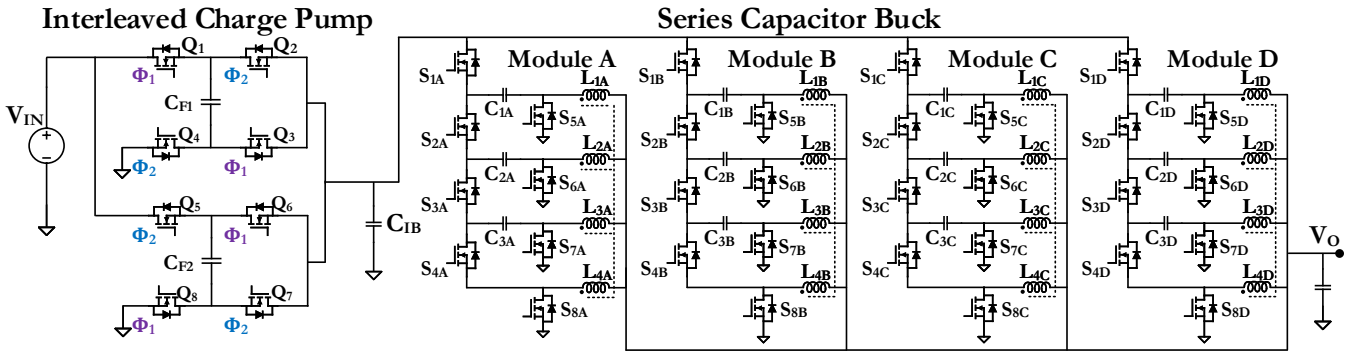


Fig. 2. A 48 V-1 V VIB-PoL topology with a 24 V VIB: a front-end interleaved charge pump and a second series-capacitor buck stage with four parallel modules for high current load. The intermediate bus capacitor C_{IB} is very small. The output inductors of each series-capacitor buck module are coupled.

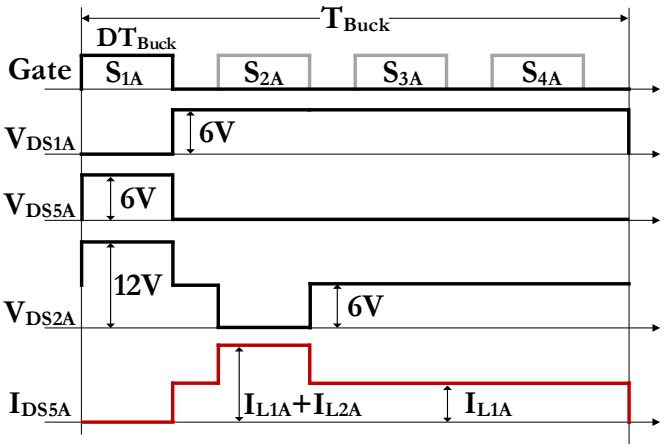


Fig. 3. Gate driver signals, drain-source voltage, and drain-source current of a series-capacitor buck module with 4-phase interleaving.

Load (VIB-PoL) architecture for high efficiency and high power density 48 V–1 V applications. The virtual intermediate bus voltage is placed at 24 V. As illustrated in Fig. 2, the first stage of the VIB-PoL architecture is a 2:1 switched-capacitor charge pump. The second stage comprises four paralleled 4-cell series-capacitor buck modules, which is equivalent to a 16-phase 6:1 buck VRM with comparable power conversion stress [23], [24]. The inductors in each series-capacitor buck module are coupled to improve the transient response [25], [26]. Leveraging the merged two-stage soft-charging concept [27]–[33], the charge pump and the series-capacitor buck converter are jointly operated. The flying capacitors of the charge pump are reused as the input capacitors of the regulation stage. The VIB-PoL architecture has three major advantages: 1) reduced equivalent voltage conversion ratio and reduced device stress in both the charge pump and the voltage regulation stages; 2) eliminated inductors in the charge pump stage and eliminated intermediate bus capacitors; 3) utilization of series-stacked low voltage rating devices for high voltage conversion ratio applications. A 48 V–1 V switched-capacitor (SC) voltage regulator with VIB-PoL architecture is designed and tested to deliver 640 A of output current with 0.8 V–1.2 V output voltage range. The prototype achieved a peak power stage efficiency of 95.2% and a full load efficiency of 84.4% at an output voltage of 1 V. The current area density is 0.311 A/mm^2 and the power density is 463 W/in^3 at 1 V, 640 A output with liquid cooling. The peak efficiency, full load efficiency, and the box power density including gate driver loss and volume at 450 A, 1 V output with air cooling are 93.3%, 88.1%, and 231 W/in^3, respectively.

The remainder of this paper is organized as follows: Section II introduces the circuit topology of the VIB-PoL architecture. Section III details its operation mechanisms. Section IV presents the design guidelines for the 48 V–1 V hybrid voltage regulator. Section V derives the small-signal model of the series-capacitor buck stage. Experimental results are shown in Section VI. Section VII presents a loss analysis, comparison, and discussion. Finally, Section VIII concludes this paper.

II. Topology Overview

Figure 2 shows an example topology of the 48 V–1 V VIB-PoL voltage regulator. The charge pump stage and the series-capacitor buck stage are connected through the 24 V virtual intermediate bus with a small filter capacitor C_{IB}. The voltage ripple on the 24 V virtual intermediate bus with a small C_{IB} is higher than that in a traditional decoupled two-stage architecture in heavy load condition. The charge pump stage is controlled by a pair of complementary gate drive signals Φ_1 and Φ_2 with 50% duty ratio. The two flying capacitors C_{F1} and C_{F2} are swapped in cycle and are always connected in series between the 48 V input and ground. The output of the charge pump is the midpoint of the two stacked flying capacitors. The voltage conversion ratio is 2:1.

The second stage comprises four parallel-connected series-capacitor buck modules for 24:1 voltage conversion and output regulation. Each module comprises four sets of buck switching cells. The four switching cells are configured as a four-level series-capacitor buck converter with their inductors coupled. In the top three cells, a series-capacitor is connected between the source of the high-side switch and the drain of the low-side switch. The series-capacitors support the dc bias for the stacked phases and also function as the input source for each phase. Figure 3 shows the gate driver signals, the drain-source voltage, and the drain-source current of one four-level series-capacitor buck module. The high-side switches and their

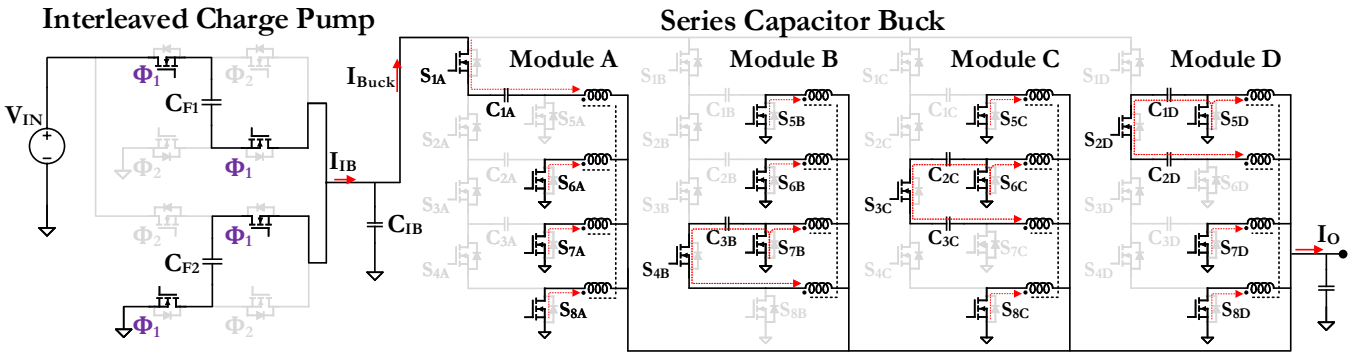
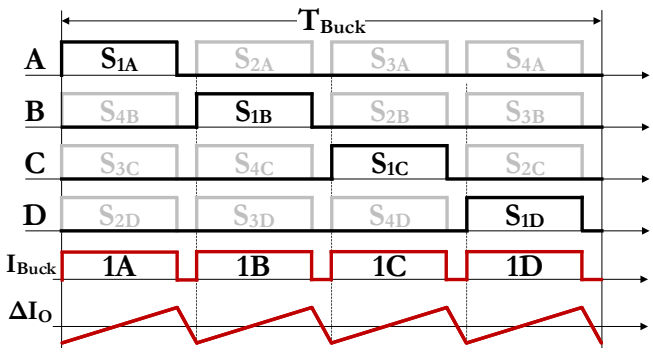


Fig. 4. Current flow condition when the charge pump control signal Φ_1 is enabled and the top switching cell of module A is conducting. There is only one series buck module activated at one time to extract energy from the charge pump flying capacitors if the duty ratio is below 25%.



(a) 4-module interleaving

(b) 16-cell interleaving

Fig. 5. Gate driver signals, input current and output current ripple of the series-capacitor buck stage with 4-module or 16-cell interleaving. There are many different ways of interleaving the many modules and cells.

complementary low-side switches are controlled in the same way as a four-phase interleaved buck converter.

In periodic steady state, the dc bias voltages of the three series-capacitors are 18 V, 12 V, 6 V from top to bottom. The effective input voltage of each cell in steady state is 6 V. All high-side switches and low-side switches are switching at 6 V, similar to a 6 V buck VRM. The three high-side switches (S_{2X}–S_{4X}) need to block a maximum voltage of 12 V (e.g., $V_{DS2A} = V_{IB} - V_{C2A} = 12$ V when S_{1A} and S_{6A} are conducting). Similarly, the three low-side switches (S_{5X}–S_{7X}) need to carry both the current of themselves and the charging current of the neighboring cell for a period of DT_{Buck}, where T_{Buck} is the switching period and D is the duty ratio of the series-capacitor buck. The switch stress of this four-phase series-capacitor buck converter is slightly higher than a 6 V–1 V four-phase buck converter.

The duty ratio of the series-capacitor buck stage is set below 25% to ensure no adjacent high-side switches conduct simultaneously in the four-cell interleaved operation. Otherwise, the voltage stress of high-side switches and low-side switches will increase to 18 V and 12 V (e.g., $V_{DS2A} = V_{IB} - V_{C3A} = 18$ V and $V_{DS6A} = V_{IB} - V_{C2A} = 12$ V when S_{1A} and S_{2A} conduct simultaneously), reducing the benefits of the series-capacitor topology. In this 4-level series-capacitor design with 24 V VIB, the maximum output voltage is 1.5 V when $D \leq 25\%$ with 48 V input voltage. [24] systematically compares the series-capacitor buck converter with a multiphase buck converter. [34] presents a modulation strategy with a 50% maximum duty ratio and two-cell interleaving operation for the four-level series-capacitor buck module.

One can adopt interleaving to reduce the input/output ripple and enhance the transient performance. For the intermediate bus, one option is to evenly interleave the four top switching cells (1A, 1B, 1C, 1D) in one switching cycle by 90°. As shown in Fig. 4 and Fig. 5(a), only one top switching cell is conducting to discharge the intermediate bus capacitor. The input current I_{Buck} of the series-capacitor buck stage is a square wave pulse without overlap. The 4-module interleaving also reduces the root-mean-square (RMS) current of I_{IB} and the conduction loss of the charge pump stage with small C_{IB}. One can further interleave the 16 series-capacitor cells to gain more advantages on the output ripple and transient performance. As shown in Fig. 5(b), the 16-cell interleaving can multiply the output ripple frequency by 16 times, enabling significant ripple reduction compared with the 4-module interleaving.

III. Operation Principles of the VIB-PoL Architecture

Since the 24 V virtual intermediate bus is always connected to the midpoint of the two stacked flying capacitors, the flying capacitors can be considered as the input capacitor of the second stage. This allows the merged-two-stage operation of the VIB-PoL architecture and offers many advantages [28]–[30]. In principle, the converter only has one magnetic component

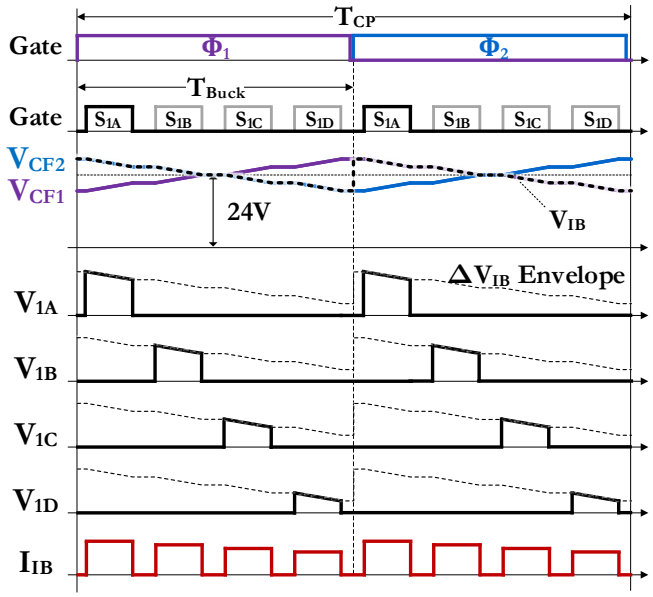


Fig. 6. Gate signals with 4-module interleaving, the flying capacitor voltages, the intermediate bus voltage V_{IB}, the effective input voltage of the series buck stage V_{1A}–V_{1D} and the output current of the charge pump I_{IB}.

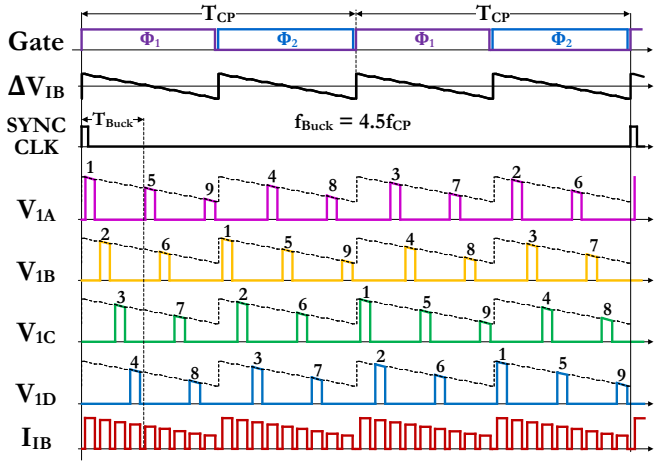


Fig. 7. Operation principles of phase rotating module-level current balancing in the series-capacitor buck stage with 4-module interleaving. Each module sequentially activates at the peak of the VIB voltage.

– the output inductor – there is no other discrete magnetic component. Figure 6 shows the operational waveforms of the VIB-PoL topology with the 4-module interleaving. T_{CP} is the switching cycle of the charge pump stage and T_{CP} equals $2T_{Buck}$ in this example. Assume large series capacitance and small voltage ripple, the ripple of the effective input voltage at the top switch node is mostly contributed by the voltage ripple on the intermediate bus. As illustrated in Fig. 6, the effective input voltage of each top phase is different due to the interleaved operation among modules. Unlike in a two-stage architecture with large decoupling capacitors, the charge pump stage and the series-capacitor stage need to be coordinated to achieve soft-charging and voltage balancing of the flying capacitors, as well as current balancing among modules.

A. Soft-Charging

Charge-sharing loss happens when two capacitors with a voltage difference are forced in parallel. The charge-sharing loss can be reduced by increasing the capacitor size or increasing the switching frequency, and can be eliminated by using current source to soft charge the capacitors. In the VIB-PoL topology, the two flying capacitors C_{F1} and C_{F2} are always connected in series. As a result, there is no charge-sharing loss between them. Under ideal conditions with no parasitic elements, the intermediate bus capacitor is not needed. The output current of the charge pump stage I_{IB} equals the top cell current of the series-capacitor buck stage, which is a square wave current source. In practical designs, parasitics are unavoidable. A small filter capacitor is included at the intermediate bus to function as a filter. This capacitor should be large enough to ensure the voltage balancing of the flying capacitors of the charge pump, and small enough to avoid adding significant charge-sharing loss to the system.

B. Voltage Balancing of the Flying Capacitors

In both operation phases of the charge pump stage, two flying capacitors are always connected in series and their total voltage is clamped to the 48 V input bus, yielding $\mathrm{d}v_{CF1}/\mathrm{d}t = -\mathrm{d}v_{CF2}/\mathrm{d}t$. If $C_{F1} = C_{F2}$, two flying capacitors can equally share the charge pump output current I_{IB}. In order to maintain the charge balance for each flying capacitor, the number of the charge pulses and discharge pulses must be equal (e.g., four in Fig. 6). The amplitude of the four current pulses in the operation phase 1 (when Φ_1 is enabled) also should be equal to their corresponding pulses in phase 2 (when Φ_2 is enabled). Therefore, strict frequency matching and gate signal synchronization are required between the charge pump stage and the series-capacitor buck stage. The gate signals of four top switches (S_{1A}–S_{1D}) are synchronized to the rising edge of Φ_1 and Φ_2 with a proper delay, which also enables zero-current switching (ZCS) for the charge pump switches. The relationship between the switching frequencies of the charge pump stage (f_{CP}) and the series buck stage (f_{Buck}) with the 4-module interleaving operation is:

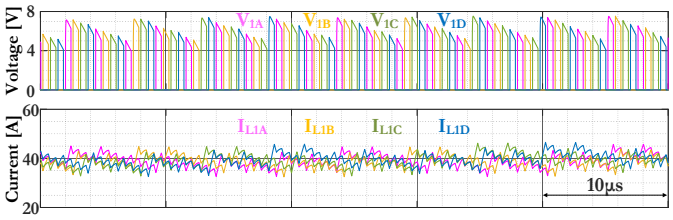
$$\frac{1}{2f_{CP}} = \frac{K}{4f_{Buck}}, K = 1, 2, 3, \cdots \tag{1}$$

For the 16-cell interleaving mode the relationship is:

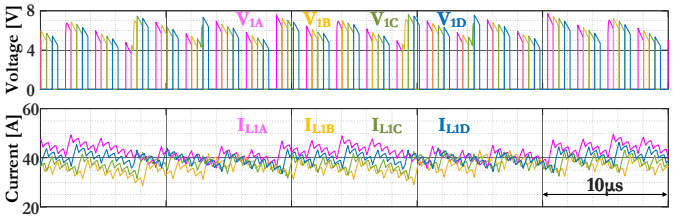
$$\frac{1}{2f_{CP}} = \frac{K}{f_{Buck}}, K = 1, 2, 3, \cdots \tag{2}$$

C. Current Balancing of the Series-Capacitor Buck Stage

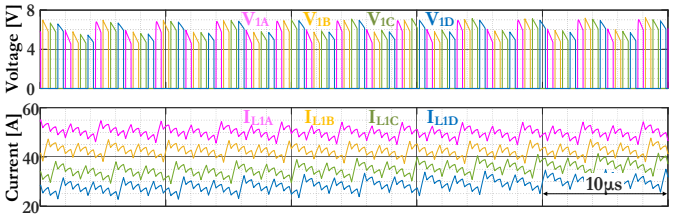
Current balancing of the second stage includes two levels: cell-level and module-level. The cell-level current balancing within a series-capacitor module is maintained by the charge balance requirement of three series-capacitors. One series-capacitor is charged by the inductor current of the same cell for a period of DT_{Buck}, and discharged by the inductor current of the next cell for another period of DT_{Buck} in the same switching cycle. The net charge of each series capacitor has to be zero to balance the current across all cells if all cells



(a) f_{Buck}=4.5f_{CP} with 4-module interleaving. Current is well balanced.



(b) f_{Buck}=4.5f_{CP} with 16-cell interleaving. Current oscillation is observed.



(c) f_{Buck}=4f_{CP} with 4-module interleaving. Current imbalance is observed.

Fig. 8. Simulated effective input voltage V_{1A}–V_{1D} and the inductor current I_{L1A}–I_{L1D} of the top cell of each series-capacitor buck module. The module-level current balancing of the series-capacitor buck stage can be achieved by setting f_{Buck}=4.5f_{CP} with 4-module interleaving. As expected, with 16-cell interleaving, current oscillation is observed in (b). With f_{Buck}=4f_{CP}, current imbalanced is observed in (c). Current balancing can also be achieved by active current control.

are controlled by the same duty ratio. The cell-level current balancing mechanism of the series-capacitor buck topology has been systematically studied in [35], [36].

There is no intrinsic current balancing mechanism between parallel series-buck modules. The component placement needs to be carefully designed to ensure symmetrical trace routing and equal impedance. Furthermore, the large voltage ripple on the intermediate bus may cause current mismatch at the module level. In the case of Fig. 6 where T_{CP} equals $2T_{Buck}$, the effective input voltage of phase 1A is always the highest, and the effective input voltage of phase 1D is always the lowest. Active current balancing methods, including current mode control, can be applied to mitigate this impact.

We present an example module-level current balance strategy for the series-capacitor buck stage. The key principle is to rotate the switching position of all top cells. As illustrated in Fig. 7, the ripple cycle of the intermediate bus voltage is $0.5T_{CP}$, during which the top cells of the second stage switch odd times (e.g., 9 times when $T_{CP} = 4.5T_{Buck}$). The top switch of the series-buck modules will activate sequentially at the peak of the virtual intermediate bus. In addition, 4-module interleaving is required to evenly distribute the switching positions of top switches in one ripple cycle. This configuration enables identical average effective input voltage across all series-buck modules in $2T_{CP}$. To enable automatic current balancing, the relationship between f_{CP} and f_{Buck} is:

$$f_{Buck} = \frac{2K+1}{2} f_{CP}, K = 1, 2, 3, \cdots \tag{3}$$

Equation (3) also covers the requirement of (1). In our implementation, the gate signals of the charge-pump stage and the series-capacitor buck stage are synchronized at the beginning of every two charge pump cycles.

Figure 8(a) shows a few SPICE simulation results for module-level current balancing. The frequency of the series buck stage is 4.5 times higher than that of the charge pump stage. The four modules are interleaved. The average current of the coupled inductor current of each top cell in the series-capacitor buck stage is equal. The currents of the four phases within a series-buck converter module are intrinsically balanced [35], [36]. If the switching positions of each top cell are not evenly distributed, or if the switching frequencies of the two stages are not carefully selected, the module-level current balancing may not be achieved, as shown in Fig. 8(b) and Fig. 8(c).

IV. VIB-PoL Converter Design

We introduce the design principles of the 48 V–1 V 640 A VIB-PoL voltage regulator. The circuit schematic of the prototype is shown in Fig. 2, including a 48 V–24 V interleaved charge pump converter and four 24 V–1 V series-capacitor buck modules. Table I lists the bill-of-material (BOM) of the prototype. Figure 9 shows the layout of the prototype with most switches, capacitors, and gate drivers placed on the top side. The coupled inductors with four charge pump switches are placed on the bottom side. The PCB area of the power stage is 23.5 mm × 43.8 mm × 2 = 2,058.6 mm^2 (66 mm × 43.8 mm = 2890.8 mm^2 including the gate drivers).

A. Interleaved Charge Pump Stage

The charge pump stage performs 48 V–24 V voltage conversion and operates at around 100 kHz. Silicon MOSFETs with a 40 V breakdown voltage are used for Q_1–Q_8. C_{F1} and C_{F2} should be sized equal to maintain the voltage balance between them. The peak-to-peak voltage ripple of the flying capacitors ($C_{F1} = C_{F2} = C_F$) is:

$$\Delta V_{CF} = \frac{P_{IN}}{2V_{IN} f_{CP} C_F}. \tag{4}$$

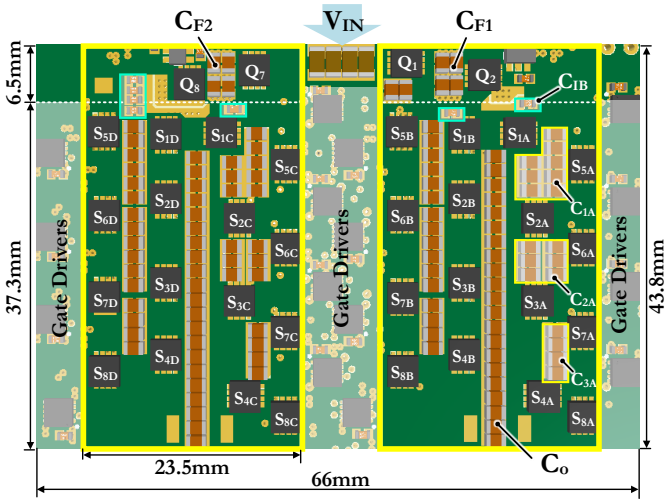
Assume the full load efficiency of the converter is 85% at 1 V and 640 A, the input power of the charge pump stage is around 750 W. In this case, 16 multilayer ceramic capacitors (MLCC) are connected in parallel as one flying capacitor with an effective capacitance of 23.4 µF. The peak-to-peak voltage ripple ratio at full load is 14%.

B. Series-Capacitor Buck Stage with Coupled Inductors

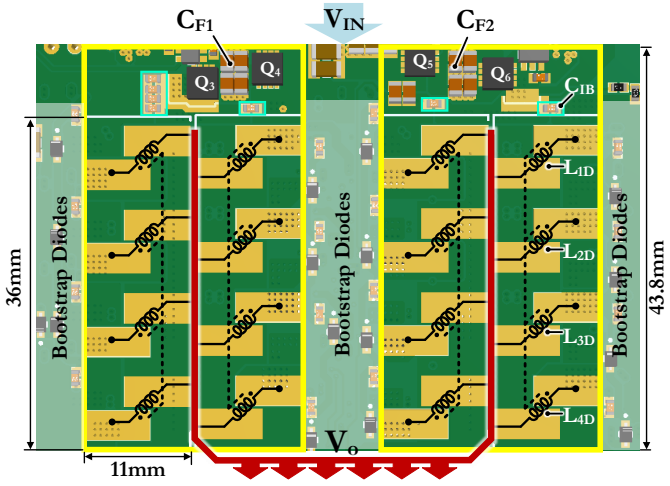
There are four parallel series-capacitor modules in the second stage. Each four-phase series-capacitor module can deliver a maximum output current of 160 A. The maximum current of each phase is 40 A. The four inductors in one

TABLE I
BILL-OF-MATERIAL OF THE VIB-POL PROTOTYPE

$Q_1 - Q_8$	Infineon BSZ024N04LS6, 40 V/2.1 mΩ
C_{F1}&C_{F2}	0805 X5R 35 V/22 µF×16, C_{eff}=23.4 µF
C_{IB}	0603 X5R 35 V/4.7 µF×22, C_{eff}=10 µF
C_{1X}	0805 X7S 25 V/10 µF×8, C_{eff}=21.6 µF
C_{2X}	0805 X7S 25 V/10 µF×6, C_{eff}=25.2 µF
C_{3X}	0805 X7S 25 V/10 µF×4, C_{eff}=29.2 µF
C_o	0805 X5R 2.5 V/100 µF×44, C_{eff}=4 mF
$L_{1X} - L_{4X}$	Eaton CL1108-4, 4-Phase Coupled, L_K=50 nH
$S_{1X} - S_{4X}$	Infineon BSZ031NE2LS5, 25 V/2.6 mΩ
$S_{5X} - S_{8X}$	Infineon BSZ011NE2LS5I, 25 V/0.82 mΩ



(a) Top side with switches and capacitors



(b) Bottom side with coupled inductors

Fig. 9. Components placement and power stage layout. The PCB area of the power stage is 23.5 mm × 43.8 mm × 2=2,058.6 mm^2 and 66 mm × 43.8 mm = 2890.8 mm^2 including the gate drivers.

module are coupled. A four-phase coupled inductor with a per-phase current rating of 50 A (Eaton CL1108-4-50TR) is used in each module. The magnetizing inductance is 300 nH, the leakage inductance is 50 nH and the dc resistance is 0.28 mΩ

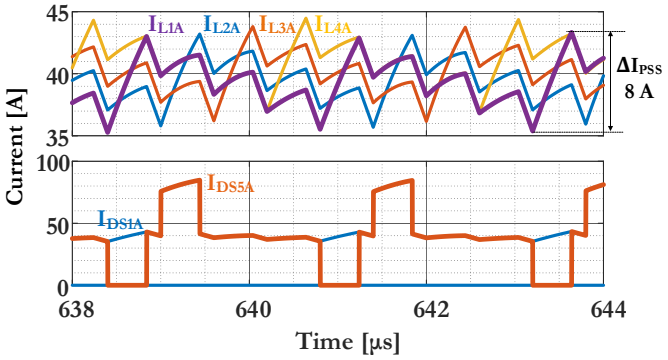


Fig. 10. Simulated current waveforms of the coupled inductor, the high-side switch and the low-side switch. The low-side switch needs to carry both its own current and the current of the next cell for a period of DT_{Buck}.

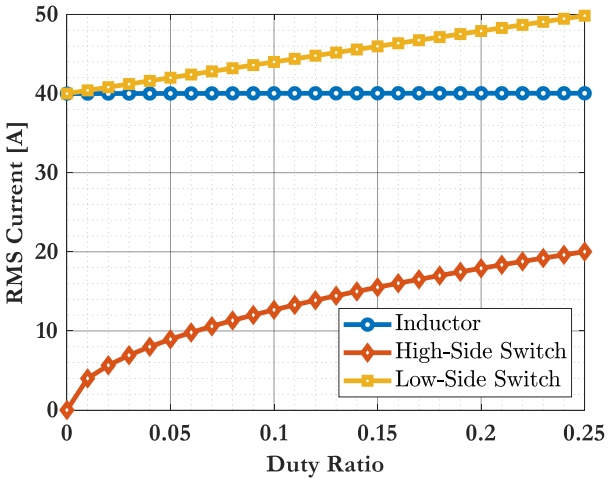


Fig. 11. Simulated per-phase RMS current of the coupled inductor, the high-side switch and the low-side switch at the full load per-phase current of 40 A.

per phase. Compared to four discrete 50 nH inductors, the coupled inductor reduces the phase current ripple by about 5 times [37]–[39]. The per-phase steady state peak-to-peak current ripple is 8 A with the duty ratio $D = 1/6$ at 417 kHz.

Figure 10 illustrates the simulated phase current waveforms of the coupled inductor and its corresponding high-side switch and low-side switch. Their RMS currents at the 40 A full load are calculated and shown in Fig. 11. The RMS current of the low-side switch increases as the duty ratio increases because it needs to carry the currents of two cells for a period of DT_{Buck}. The device voltage stress in the series-capacitor buck stage is 12 V and 6 V. Two 25 V silicon MOSFETs are selected for the high-side switches and low-side switches.

The size of each series-capacitor is 20 µF for a peak-to-peak voltage ripple of 0.8 V at 1 V output and full load. Multiple X7S MLCC capacitors are connected in parallel (×8, ×6, ×4 for C_{1X}, C_{2X}, C_{3X}) for the series capacitors. Their dc derated capacitance is 21.6 µF, 25.2 µF, 29.2 µF, respectively.

Figure 12 shows the gate drive circuit of the series-capacitor buck module. A pair of high-side switch and low-side switch are controlled by a half-bridge gate driver (TI UCC27201A). The internal bootstrap diode of three of the drivers only takes effect during the startup. Three cascaded bootstrap diodes are

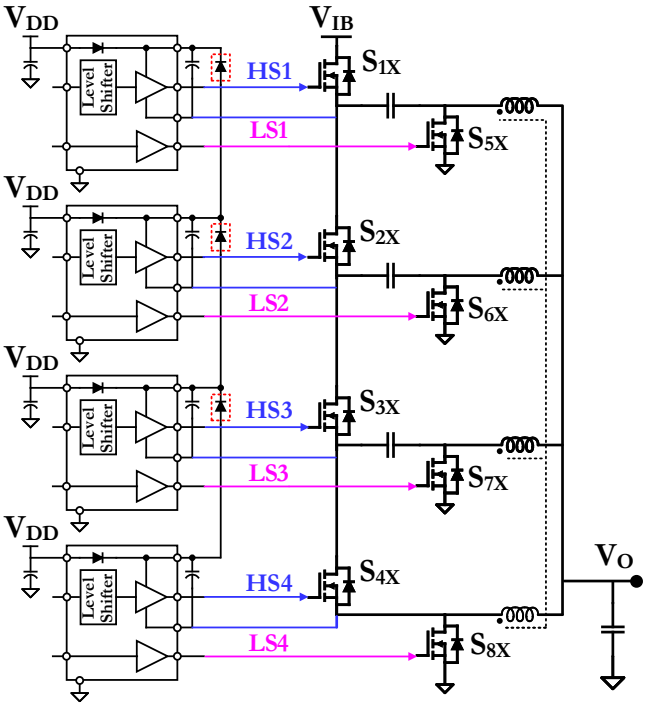


Fig. 12. Gate drive circuit of the series-capacitor buck module with half-bridge gate driver IC UCC27201A and three series-stacked bootstrap diodes.

connected in series to provide the high-side bias voltage from the bottom to the top in steady state.

C. Virtual Intermediate Bus Design

Complete soft-charging can be achieved if the capacitance between the intermediate bus and the reference ground is zero. In practical designs, a small filter capacitor C_{IB} is needed to mitigate the switching ripple of the series-capacitor buck stage, damp the voltage/current ringing induced by the parasitic inductance, and balance the flying capacitor voltage. Figure 13 compares the simulated operation waveforms of the charge pump stage with a small C_{IB} and a large C_{IB}. The flying capacitors experience small voltage change during the charge-sharing with small C_{IB}, and large voltage change with large C_{IB}. The flying capacitor voltage change ΔV_1 and the bus capacitor voltage change ΔV_2 after the charge-sharing can be calculated by applying the charge balance to C_F and C_{IB}:

$$\Delta V_1 = \frac{C_{IB}}{2C_F + C_{IB}} \Delta V_{CF}, \Delta V_2 = \frac{2C_F}{2C_F + C_{IB}} \Delta V_{CF}. \quad (5)$$

The total charge transferred during the charge-sharing is:

$$Q_{CS} = 2C_F \Delta V_1 + C_{IB} \Delta V_2 = \frac{2P_{IN}}{\left(\frac{2C_F}{C_{IB}} + 1\right) V_{IN} f_{CP}}. \quad (6)$$

A larger C_{IB} will introduce higher charge transferred as well as the charge sharing loss. The impact of the size of C_{IB} on conduction loss is analyzed by PSIM simulations. The parasitic inductance L_{PCB} is 0.82 nH as extracted from the measured waveform of the bus voltage ripple. A variety of different values of C_{IB} are simulated with results shown in Fig. 14. The voltage balance mechanism of the flying capacitors is

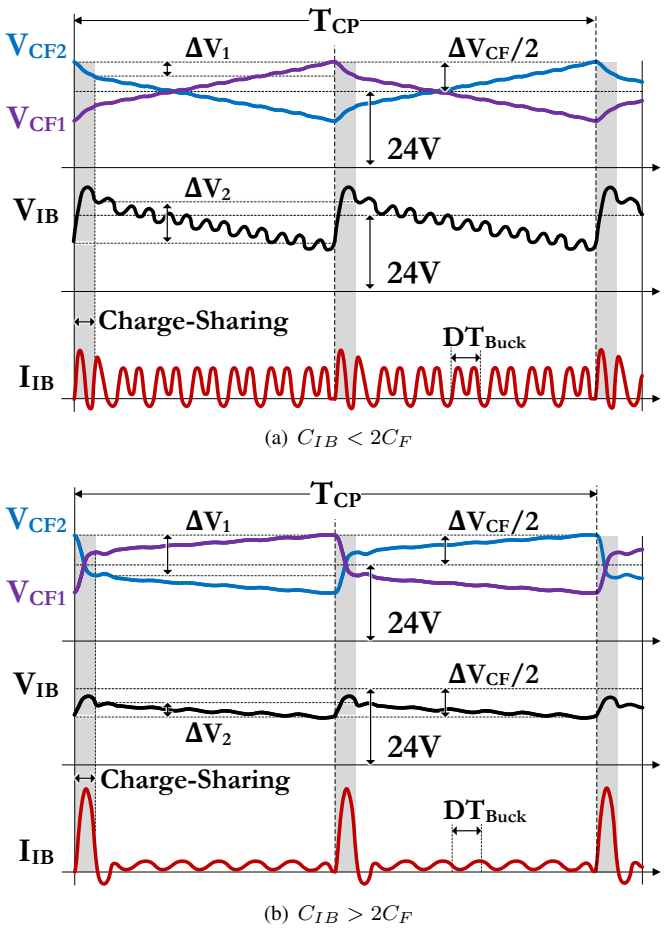


Fig. 13. Flying capacitor voltage, intermediate bus voltage and charge pump output current with different value of C_{IB}. The current waveforms with different intermediate capacitance values are plotted based on simulations.

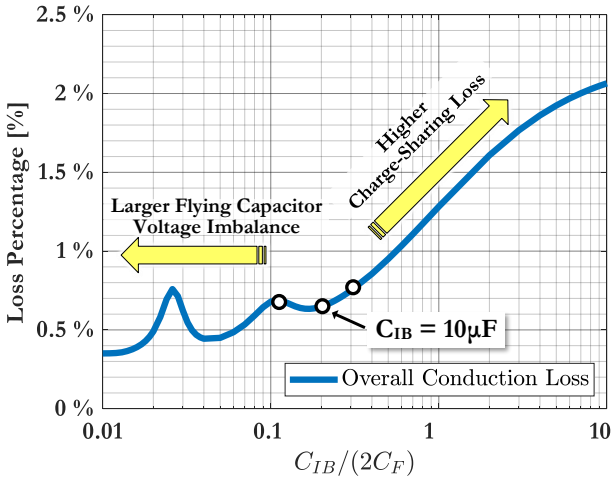


Fig. 14. Simulated overall conduction loss of the charge pump stage at 48 V-24 V/400 W/96.15 kHz, C_F is 23.4 μF. If C_{IB} is small, the voltage of the flying capacitors may be imbalanced. If C_{IB} is large, the system may suffer significant charge sharing loss.

weakened with very small C_{IB}, and the loss increases as C_{IB} increases. In this design, C_{IB} is selected as 10 μF after jointly considering the conduction loss and the voltage balancing.

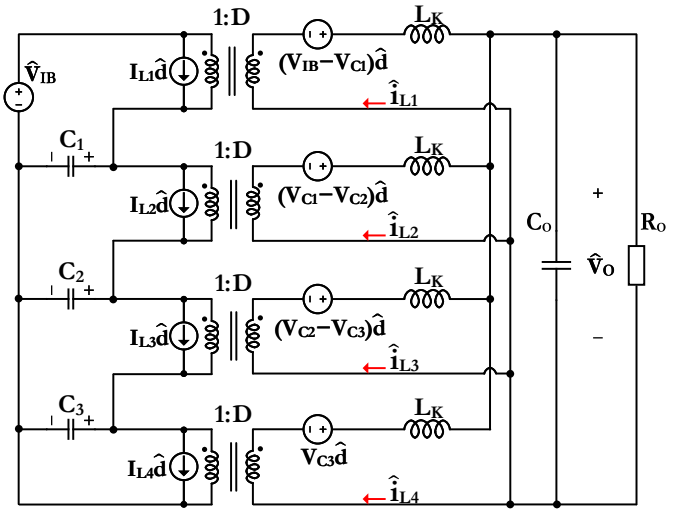


Fig. 15. Small-signal ac model of a four-level series-capacitor buck module. Assuming large enough flying capacitors, the transfer function of a four-level series-capacitor buck module is similar to that of a four-phase interleaved buck converter. They can be controlled in a similar way.

V. Modeling of the Series-Capacitor Buck Stage

Figure 15 shows the state-space average model of a four-level series-capacitor buck module. In this small-signal ac analysis, the inductor value of each switching cell is set to be the leakage inductance of the four-phase coupled inductor L_K [40]. The following equations can be obtained by applying KVL and KCL to the average model:

$$D\left(\hat{v}_{IB}-\hat{v}_{C1}\right)+\left(V_{IB}-V_{C1}\right)\hat{d}-sL_K\hat{i}_{L1}=\hat{v}_o, \quad (7)$$

$$D\left(\hat{v}_{C1}-\hat{v}_{C2}\right)+\left(V_{C1}-V_{C2}\right)\hat{d}-sL_K\hat{i}_{L2}=\hat{v}_o, \quad (8)$$

$$D\left(\hat{v}_{C2}-\hat{v}_{C3}\right)+\left(V_{C2}-V_{C3}\right)\hat{d}-sL_K\hat{i}_{L3}=\hat{v}_o, \quad (9)$$

$$D\hat{v}_{C3}+V_{C3}\hat{d}-sL_K\hat{i}_{L4}=\hat{v}_o. \quad (10)$$

Combining (7)–(10):

$$D\hat{v}_{IB}+\hat{v}_{IB}\hat{d}-sL_K\sum_{n=1}^{4}\hat{i}_{Ln}=4\hat{v}_o. \quad (11)$$

Equation (11) can be extended to the entire series-capacitor buck stage with 4 modules and 16 switching cells:

$$4D\hat{v}_{IB}+4V_{IB}\hat{d}-\left(sL_K+r_s\right)\left(\frac{\hat{v}_o}{R_O}+\frac{\hat{v}_o}{\frac{1}{sC_o}}\right)=16\hat{v}_o. \quad (12)$$

Here R_O is the equivalent load resistance. r_s is the equivalent series resistance (ESR) of each switching cell. (12) implies that the series-capacitors have no effect on the small-signal ac model because their voltage variations all cancel out. The bus-to-output transfer function $G_v(s)$ and the control-to-output transfer function $G_d(s)$ are:

$$G_v(s)=\frac{\hat{v}_o(s)}{\hat{v}_{IB}(s)}=\frac{4D}{s^2L_KC_o+s\left(\frac{L_K}{R_o}+C_or_s\right)+\frac{r_s+16R_o}{R_o}}, \quad (13)$$

$$G_d(s)=\frac{\hat{v}_o(s)}{\hat{d}(s)}=\frac{V_{IB}}{D}G_v(s). \quad (14)$$

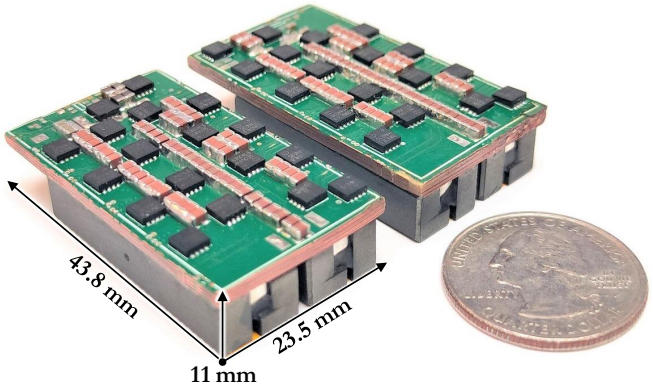


Fig. 16. Picture of the 48 V-1 V/640 A VIB-PoL CPU voltage regulator. The coupled inductors dominate the system volume and weight.

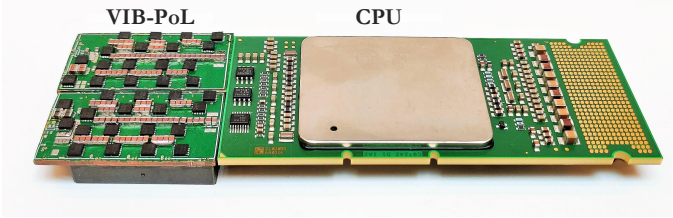


Fig. 17. Mechanical demonstration of the 48 V-1 V 640 A VIB-PoL voltage regulator placed next to a server CPU (Intel Itanium 9150, 105 W).

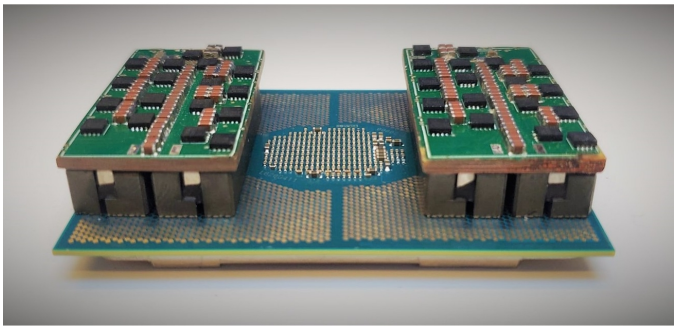


Fig. 18. Mechanical demonstration of the 48 V-1 V 640 A VIB-PoL voltage regulator vertically stacked with a server CPU (Intel Xeon Gold 6130, 125 W).

The transfer functions are very similar to that of a 16-phase interleaved buck converter, albeit with a different gain from the input voltage due to the series-stacked input (a factor of 4). Therefore, the series-capacitor buck stage with a coupled inductor can be controlled in a similar way as a typical multiphase buck converter with uncoupled inductors, if voltage mode control is to be adopted. The four-level series buck module implemented in this work has a maximum duty ratio of 25%, which may limit the transient response of the system as compared to a four-phase buck converter. Advanced modulation technique [34] can be used to extend the duty ratio beyond this limit.

VI. Experimental Results

A. Prototype and Test Bench

A 48 V to 1 V, 640 A VIB-PoL voltage regulator is fabricated and tested. Figure 16 shows the power stage of

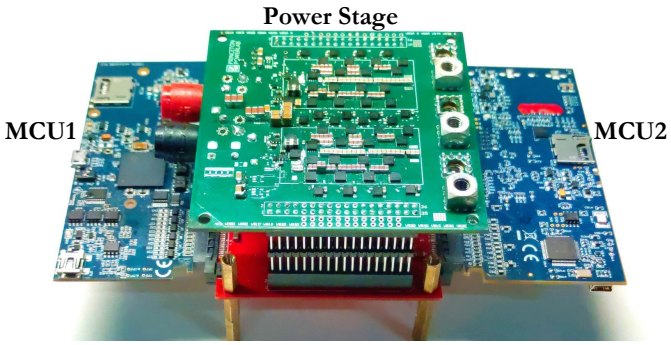


Fig. 19. Picture of the 48 V-1 V/640 A VIB-PoL voltage regulator including a power board, an interface board and two microcontroller boards.

the VIB-PoL prototype. The PCB area of the power stage is 2058.6 mm^2 (2890.8 mm^2 including the gate drivers). The maximum height of the component on the top side is 1 mm. The thickness of the PCB is 2 mm. The highest components on the bottom side are four coupled inductors with an 8 mm height. The overall height of the power stage is 11 mm. The box volume is 2058.6 mm^2 $\times$ 11 mm = 22,644 mm^3 (2890.8 mm^2 $\times$ 11 mm = 31,799 mm^3 including the gate drivers). Figure 17-18 show the lateral and vertical mechanical assembly of the VIB-PoL prototype and a CPU. Figure 19 shows a picture of the prototype including one power stage board, one motherboard, and two microcontroller (TI TMS320F28388D) boards.

Figure 20 shows the test bench and the measurement equipment. Four digital multimeters (Agilent 34401A) are used to measure the voltages and currents (through Rideon RSN-50 and Rideon RSC-1000 current shunts). The data is automatically acquired by the desktop through the BenchVue software for efficiency measurement. Four 12 V server fans with the air flow of 36 CFM (cubic feet per minute) are used for air cooling. Liquid cooling is used for higher output current. Two electronic loads, a Chroma 63103A 240 A load and a Chroma 63203 600 A load, are used. Figure 21 shows the liquid cooling setup with the power stage immersed in mineral oil. The microcontroller boards and the interface board are placed outside of the container. Two low-speed fans help circulate the oil and remove heat from the power stage.

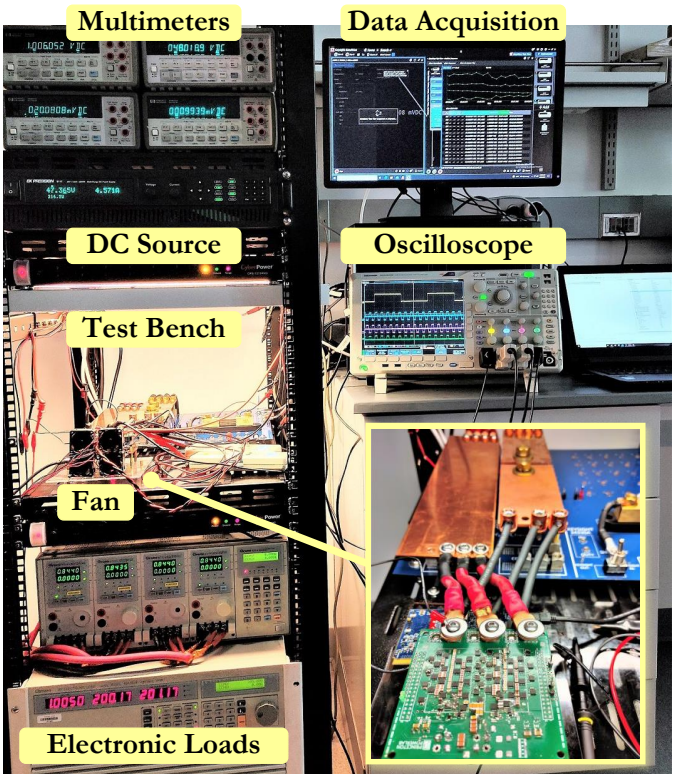


Fig. 20. Picture of the test bench and the measurement setup, including multimeters, a computer for data acquisition, dc source, two electronics loads and a high-current busbar with the input and output current shunts.

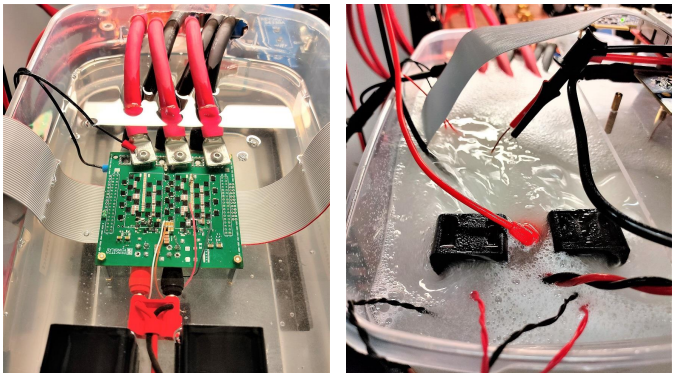


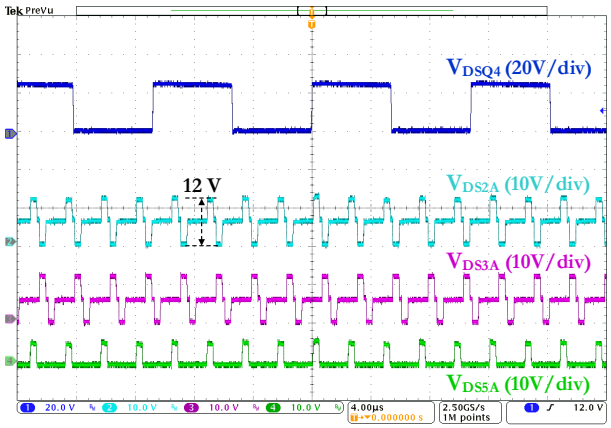
Fig. 21. Pictures of the liquid cooling setup. Left: the power stage is immersed in the mineral oil; Right: two low speed fans are circulating the oil.

B. Steady State Operation

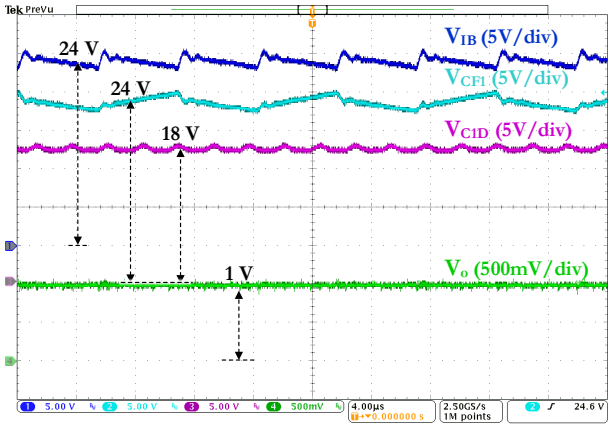
The series-capacitor buck stage is tested with three different switching frequencies: 417 kHz, 625 kHz, and 833 kHz. The corresponding switching frequency of the charge pump stage is 92.59 kHz, 96.15 kHz, and 98.04 kHz with the frequency ratio of 4.5, 6.5, and 8.5 to follow the voltage/current balance requirement of (3).

Figure 22(a) shows the drain-source voltage waveforms of MOSFETs. The high-side switches S_{2A} and S_{3A} of the series-capacitor buck stage need to block a maximum voltage of 12 V, and switch at 6 V. The voltage stress of the low-side switch S_{5A} is 6 V, and the voltage stress of the charge pump switch Q_4 is 24 V. Figure 22(b) shows the voltage waveforms of C_{IB}, C_{F1}, C_{1D}, C_o. The peak-to-peak voltage ripple of the intermediate bus as well as the flying capacitor is around 2.4 V with 400 A output current. The top series-capacitor C_{1D} has an average voltage of 18 V with a smaller ripple. The switch node voltages of four top cells (source nodes of S_{1A} – S_{1D}) in the 4-module interleaving mode are shown in Fig. 22(c). The switching positions of four top switching cells are evenly distributed at 0°, 90°, 180° , 270° in one switching cycle. The top switching node voltage has the same variation envelope as the intermediate bus voltage.

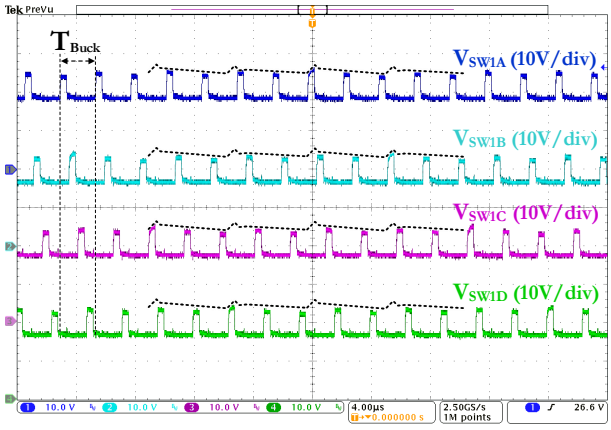
Figure 23 compares the ripple voltage under different interleaving modes. The output voltage ripple frequency is $4f_{Buck}$ with 4-module interleaving, and $16f_{Buck}$ with 16-cell interleaving. The peak-to-peak output voltage ripple with 4-



(a) Drain-source voltage waveforms of the switches.

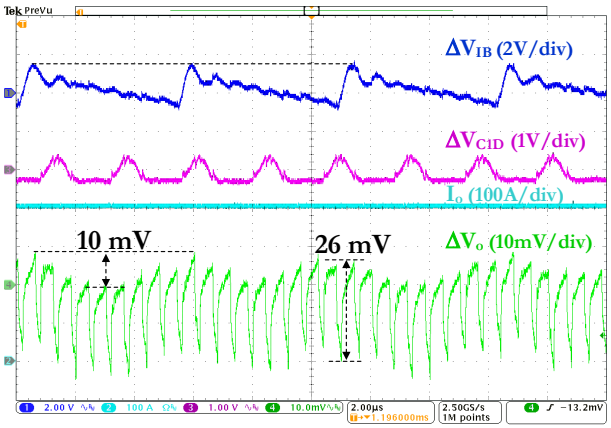


(b) Voltage waveforms of capacitors $C_{IB}, C_{F1}, C_{1D}, C_o$.

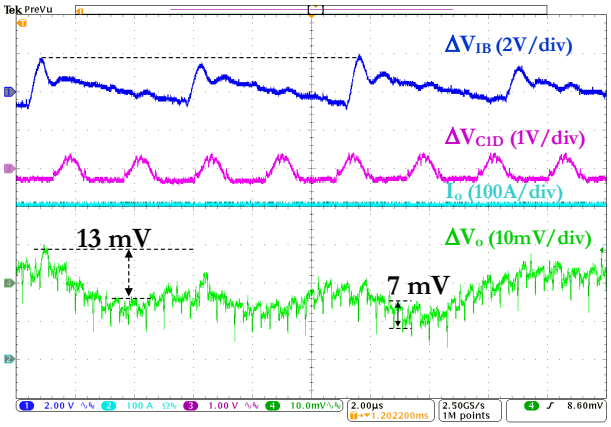


(c) Voltage waveforms of top switching nodes (S_{1A}, S_{1B}, S_{1C}, S_{1D}).

Fig. 22. Voltage waveforms of the VIB-PoL topology in the 4-module interleaved mode, $f_{CP} = 92.59$ kHz, $f_{Buck} = 417$ kHz, $I_o = 400$ A.



(a) 4-module interleaving.



(b) 16-cell interleaving.

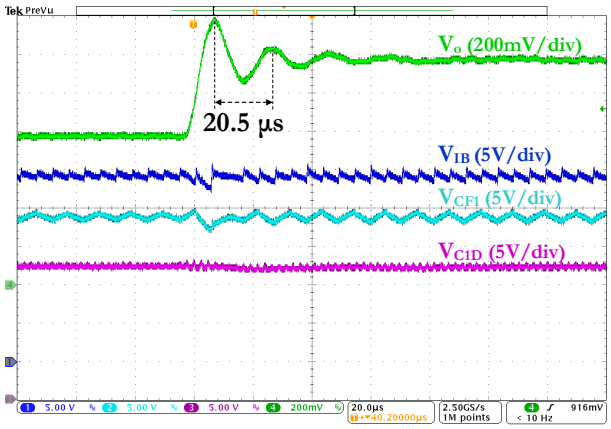
Fig. 23. Open-loop ripple voltage of C_{IB}, C_{1D} and C_o, $f_{CP} = 92.59$ kHz, $f_{Buck} = 417$ kHz, $V_o = 1$ V, $I_o = 400$ A.

module interleaving is almost 4 times of the ripple with 16-cell interleaving. The bus voltage ripple also causes low frequency ($2f_{CP}$) variation on the output voltage.

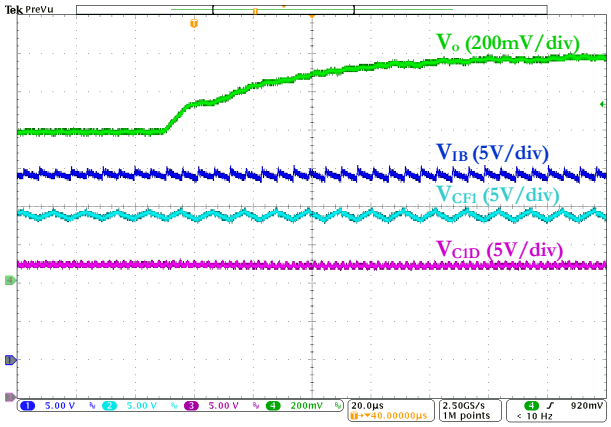
C. Transient Operation

The transient test includes the step change in output voltage and the step change in output current. Figure 24 shows the measured voltage waveforms of the output voltage step change at an output current of 200 A. The step change of the duty ratio from 13.33% to 20% results in an oscillation on the output voltage in open loop. The measured oscillation cycle is 20.5 µs, and the corresponding oscillation frequency is 48.8 kHz, which is close to the theoretical resonant frequency (45 kHz) of the control-to-output transfer function $G_d(s)$. A classic PI controller was implemented to examine the close-loop behavior. The close-loop step response is smooth without oscillation, but the settling time is longer.

Figure 25 shows the measured waveforms when the output current steps from 50 A to 350 A with a ramp-down rate of about 4 A/µs. The output voltage remains stable with the voltage mode close-loop control during the step change of the output current. With a classic voltage loop control implemented in the microcontroller, an 80-mV peak-to-peak voltage excursion is observed during the step-down transient. The intermediate bus voltage, the flying capacitor voltage, and the series-capacitor voltage are all stable during the step change of the output voltage and output current. The purpose of the transient test is to verify this merged-two-stage VIB-PoL topology can be controlled in a similar way as the traditional two-stage topology that has large decoupling capacitors. Demonstrating the extreme transient performance of the VIB-PoL architecture is beyond the scope of this paper.

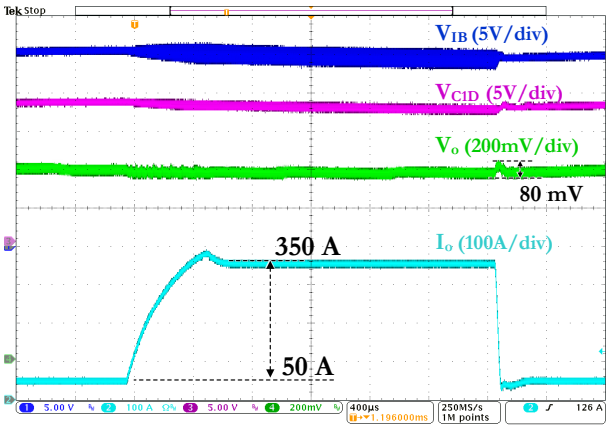


(a) Open-loop duty ratio step from 13.33% to 20%.

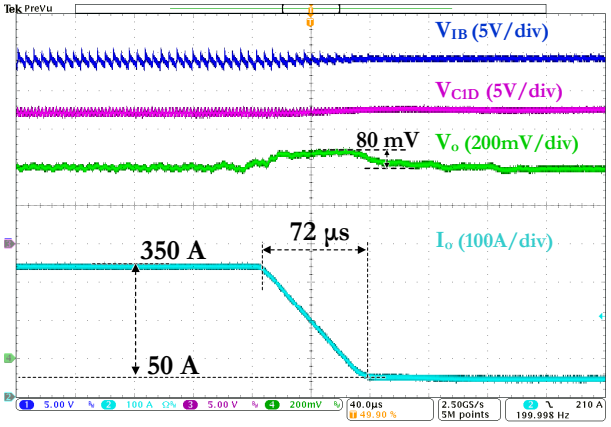


(b) Close-loop output voltage reference step from 0.8 V to 1.2 V.

Fig. 24. Open- and close- loop voltage step change of the VIB-PoL topology, $f_{CP} = 92.59$ kHz, $f_{Buck} = 417$ kHz, $I_o = 200$ A.



(a) The entire load current transient.



(b) Zoom-in waveforms during current falling.

Fig. 25. Close loop output current transient from 50 A to 350 A, $f_{CP} = 92.59$ kHz and $f_{Buck} = 417$ kHz.

D. Efficiency Measurement

The efficiencies of the VIB-PoL prototype are measured at multiple switching frequencies and output voltages. The gate drivers are powered separately by an auxiliary power source and their losses are not included. Figure 26 shows the measured 48 V to 1 V efficiency of the VIB-PoL prototype with air cooling. The overall efficiency drops as the switching frequency of series-capacitor buck stage increases because of the switching loss and the dead-time loss. The peak power stage efficiency of the VIB-PoL prototype is 95.2% at 1 V/108 A/417 kHz and the efficiency at 450 A is 89.1%. The efficiency of the VIB-PoL prototype with 16-cell interleaving operation is also measured and compared in Fig. 27. The result shows a similar light load efficiency as the 4-module interleaving, and an efficiency drop around 0.1% to 0.2% when the output current is higher than 250 A.

Figure 28 shows the thermal image of the VIB-PoL prototype with air cooling. The thermal image is captured after the component temperature stabilizes. The ambient temperature is around 25°C. The highest component temperature is 81.8°C when the output current reaches 450 A. With liquid cooling, the output current reaches 640 A, which is the current rating of the buck switches. Figure 29 shows the measured efficiency with liquid cooling. The efficiency with liquid cooling is

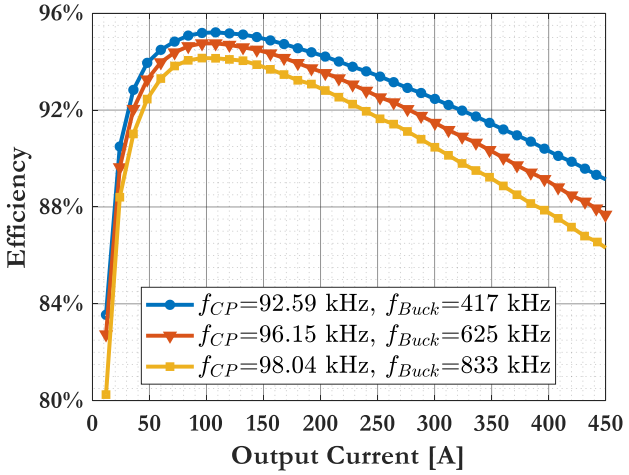


Fig. 26. Measured 48 V to 1 V efficiency of the VIB-PoL prototype with different switching frequencies under air cooling. The VIB-PoL prototype operates in 4-module interleaving mode. Gating losses are not included.

similar to the air cooling efficiency at low output current, and slightly improved at high output current.

Figure 30 shows the measured efficiency of the VIB-PoL prototype with and without including the gate drive loss, and with different gate drive voltage levels. The efficiency of the

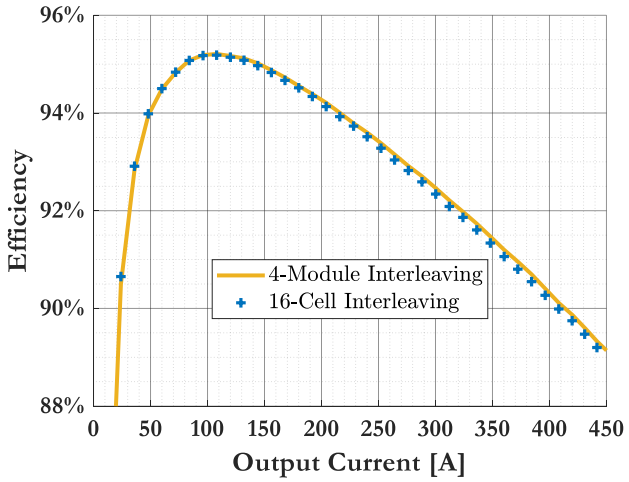


Fig. 27. Measured 48 V to 1 V efficiency of the VIB-PoL prototype with 4-module and 16-cell interleaving, f_{CP} = 92.59 kHz, f_{Buck} = 417 kHz. Gating losses are not included.

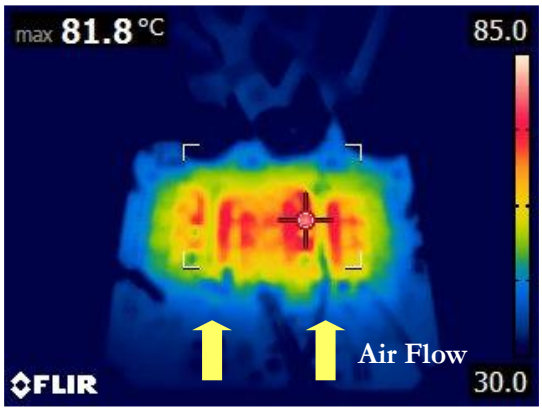


Fig. 28. Thermal image of the VIB-PoL prototype operating at 48 V-1 V/450 A, f_{CP} = 92.59 kHz, f_{Buck} = 417 kHz under 36 CFM air cooling from bottom. Heat is evenly distributed across the board.

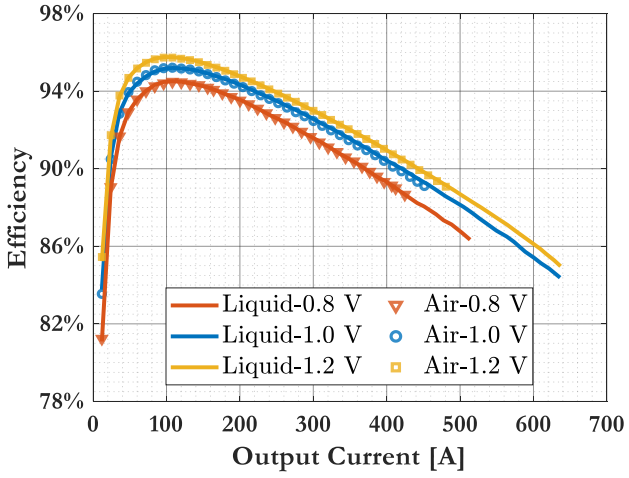


Fig. 29. Measured efficiency of the VIB-PoL prototype with liquid cooling (solid line) and with air cooling (marker only) at different output voltages. The VIB-PoL prototype is in 4-module interleaving mode, f_{CP} = 92.59 kHz and f_{Buck} = 417 kHz. Gating losses are not included.

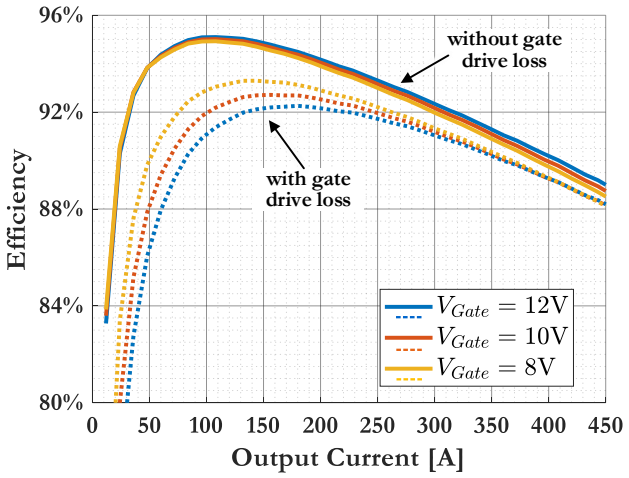


Fig. 30. Measures 48 V to 1 V efficiency with and without gate drive loss, V_{Gate} = 12 V, 10 V, 8 V, f_{CP} = 92.59 kHz, f_{Buck} = 417 kHz.

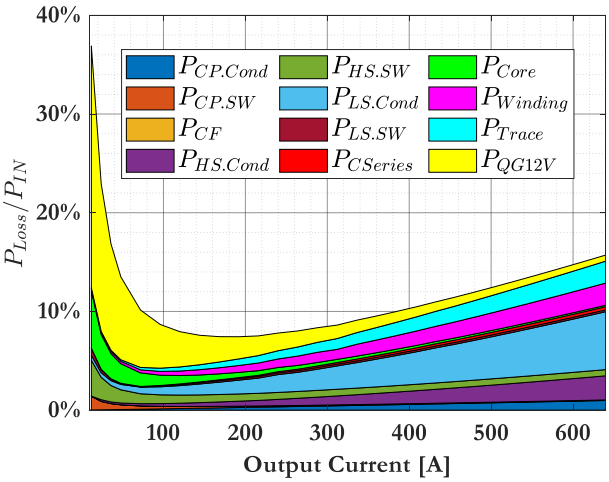


Fig. 31. Loss breakdown of the 48 V-1 V/417 kHz/92.59 kHz VIB-PoL prototype, including conduction loss of charge pump switches, high-side buck switches and low-side buck switches: $P_{CP.Cond}$, $P_{HS.Cond}$, $P_{LS.Cond}$; switching loss: $P_{CP.SW}$, $P_{HS.SW}$, $P_{LS.SW}$; ESR loss of flying capacitors and series-capacitors: P_{CF}, $P_{CSeries}$; Core loss and winding loss of coupled inductors: P_{Core}, $P_{Winding}$; PCB copper trace loss P_{Trace} and the total gate charge loss P_{QG12V} with gate drive voltage at 12 V.

power stage drops with lower gate voltage. The peak overall efficiency of the system is higher with a lower gate drive voltage. The system is more efficient with higher gate drive voltage when the output current is above 400 A.

VII. Loss Analysis, Comparison, and Discussion

Figure 31 shows a loss breakdown of the VIB-PoL prototype, including 1) losses from the charge pump: conduction loss (from SPICE simulations) and estimated switching loss of MOSFETs, ESR loss of the flying capacitors; 2) losses from the series-capacitor buck stage: estimated conduction loss and switching loss of the high-side MOSFETs and the low-side MOSFETs, ESR loss of the series-capacitors, core loss (from finite-element analysis) and winding loss of the coupled inductors; 3) conduction loss of the copper trace and the gate charge loss estimated by $Q_g V_{Gate} f$. The gate charge loss,

TABLE II
PERFORMANCE COMPARISON OF THE VIB-POL CONVERTER AND OTHER 48 V TO 1 V POINT-OF-LOAD VOLTAGE REGULATOR DESIGNS

Year	Note	@ Peak Efficiency		@ Full Load				Switching Frequency†	Including Gate Drive Loss & Size
		Output Current	Efficiency	Output Current	Efficiency	Box Power Density*	Current Area Density		
This Work	Liquid Cooled	108 A 144 A	95.2% 93.3%‡	640 A 640 A	84.4% 82.7%‡	463 W/in^3 330 W/in^3	0.311 A/mm^2 0.222 A/mm^2	417 kHz	No Yes
	Air Cooled	108 A 144 A	95.2% 93.3%‡	450 A 450 A	89.1% 88.1%‡	325 W/in^3 232 W/in^3	0.219 A/mm^2 0.156 A/mm^2	417 kHz	No Yes
2017	TI [41]	20 A	90.7%	50 A	87.7%	129 W/in^3	0.079 A/mm^2	600 kHz	Yes
2019	MP-MIH [42]	10 A	92.1%	40 A	80.4%	83.5 W/in^3	0.044 A/mm^2	300 kHz	No
2020	QSD-Buck [4]	15 A	94.5%	40 A	91.1%	30.9 W/in^3	0.024 A/mm^2	125 kHz	Eff.: No Density: Yes
2020	MLB-PoL [33]	15 A	91.5%	65 A	86.4%	198 W/in^3	0.122 A/mm^2	250 kHz	Yes
2020	Bel Power [43]	40 A	91.6%	70 A	90.5%	167 W/in^3	0.184 A/mm^2	242 kHz	Yes
2020	Sigma [2]	40 A	94.0%	80 A	92.5%	420 W/in^3	0.127 A/mm^2	600 kHz	Eff.: No Density: Yes
2020	TSAB [31]	30 A	91.5%	90 A	85.0%	36 W/in^3	0.023 A/mm^2	500 kHz	Eff.: No Density: Yes
2020	Vicor [16], [17]	120 A	90.1%	214 A	N/A	400 W/in^3	0.202 A/mm^2	1025 kHz	Yes
2020	24 V-FIB [7]	60 A	90.6%	150 A	86.2%	283 W/in^3	0.346 A/mm^2	417 kHz	No
2021	ADI [8]	30 A	90.8%	50 A	88.1%	88.5 W/in^3	0.064 A/mm^2	350 kHz	Yes
2021	On-Chip [6]	1.5 A	90.2%	8 A	76%	198 W/in^3	0.031A/mm^2	2500 kHz	Yes
2021	LEGO-PoL [44]	150 A	91.1%	450 A	85.7%	577 W/in^3	0.587 A/mm^2	1000 kHz	No

∗ The power density is calculated with the box volume (defined as the maximum Length×Width×Height) of the prototype.
† The switching frequency of the voltage regulation stage.
‡ Efficiency with 8-V gate voltage.

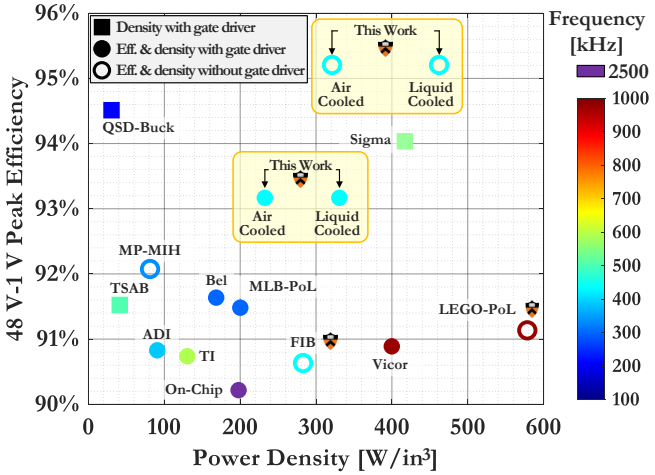


Fig. 32. Peak efficiency and power density of the designs presented in Table II. Data only including the gate driver size are marked by filled rectangle. Data with gate driver loss & size are marked by filled circles and data without gate driver loss & size are marked by hollow circles.

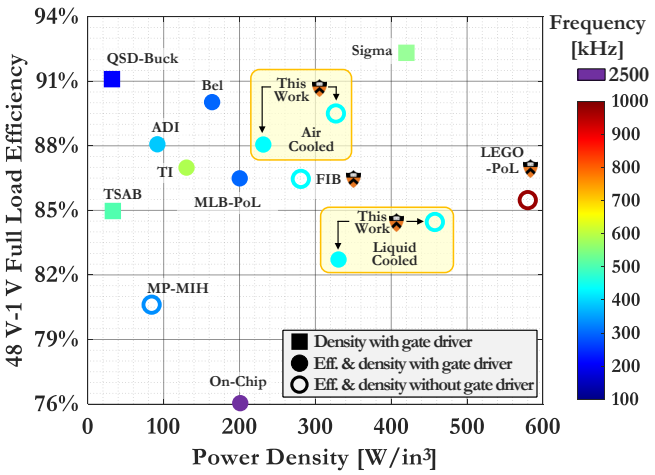


Fig. 33. Full load efficiency and power density of the designs presented in Table II. Data only including the gate driver size are marked by filled rectangle. Data with gate driver loss & size are marked by filled circles and data without gate driver loss & size are marked by hollow circles.

the core loss, and part of the switching loss contributed by C_{oss} of MOSFETs dominate the power loss at light load. The conduction loss increases quadratically with the current and they contribute most of the power loss at heavy load. The gate drive loss consumes almost 10% to 25% of the overall input power at light load with a 12 V gate voltage. Reducing the gate voltage can improve the overall system efficiency at light load. Phase-shedding technique is also applicable to the VIB-PoL system in light load.

Table II compares a few key metrics of the VIB-PoL converter with other state-of-the-art 48 V-to-1 V point-of-load voltage regulator designs. The peak efficiency and peak power

density of Table II are visualized in Fig. 32. The power density and the corresponding full load efficiency of Table II are visualized in Fig. 33. The VIB-PoL converter presented in this work achieves the highest peak efficiency: 95.2% without gate driver loss and 93.3% with gate driver loss, as well as high power density and current area density with both air cooling and liquid cooling.

VIII. Conclusions

This paper presents a 48 V to 1 V CPU voltage regulator with a 24 V virtual intermediate bus architecture. A charge pump stage and a series-capacitor buck regulation stage are directly linked at the intermediate bus without large decoupling capacitors under merged-two-stage operation. The switched-capacitor based design in both stages reduces the voltage conversion stress, improves the device utilization, and enables high efficiency. Coupled inductors are used to further reduce the ripple and improve the power density. A 48 V to 1 V, 640 A prototype with a peak power stage efficiency of 95.2% (93.3% including gate driver loss), a full load efficiency of 84.4% (83.1% including gate driver loss), a power density of 463 W/in^3, and a current area density of 0.311 A/mm^2 was tested to verify the effectiveness of the VIB-PoL architecture.

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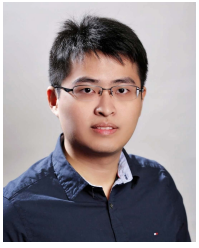

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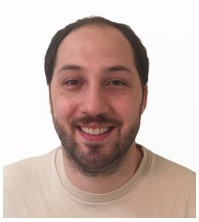

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