

# LEGO-PoL: A 48V-1.5V 300A Merged-Two-Stage Hybrid Converter for Ultra-High-Current Microprocessors

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**Abstract**—This paper presents a family of 48 V–1.5 V merged-two-stage hybrid-switched-capacitor converters with a *Linear Extendable Group Operated Point-of-Load* (LEGO-PoL) architecture for high current microprocessors. The proposed LEGO-PoL converter leverages the advantages of switched-capacitor (SC) circuits and multiphase buck circuits and can achieve soft charging, current sharing, and automatic voltage balancing. The SC circuits are connected in series to split the high input voltage into multiple stacked voltage domains, and the multiphase buck circuits are connected in parallel to split the high output current into multiple parallel current paths. The inductors of the multiphase buck converters are used as current sources to soft-charge and soft-switch the switched-capacitor circuits, and the switched-capacitor circuits are utilized to ensure current sharing among the multiphase buck circuits. The voltage balancing and current sharing mechanisms of the LEGO-PoL architecture are investigated in detail. A 450 W, 48 V–1.5 V, 300 A LEGO-PoL converter with a peak efficiency of 96%, a full load efficiency of 87.7%, and a power density of 577 W/in<sup>3</sup> was built and tested to verify the effectiveness of the LEGO-PoL architecture.

**Index Terms**—DC-DC power conversion, hybrid switched-capacitor circuit, linear extendable group operated (LEGO) architecture, point of load (PoL) converter

## I. INTRODUCTION

Power converters with high efficiency, high power density, and high bandwidth are needed to support future high performance microprocessors (CPUs, GPUs, and TPUs) [1]–[13]. One emerging trend in data center power delivery is to feed the servers with high voltage (e.g., 48 V) from the open compute racks. Delivering power at 48V reduces the conduction loss, improves the UPS deployment flexibility, and can leverage the existing semiconductor devices and circuit topologies of the 48 V telecom power ecosystems. Various topologies for high voltage conversion ratio high current PoL applications have been proposed, including hybrid-switched-capacitor-based designs [1]–[8], multi-phase-buck designs [9], [10], and transformer-based designs [11]–[13].

Among these solutions, two-stage “switched-capacitor & multiphase buck” designs are very attractive as they separate the challenges of achieving high conversion ratio and high bandwidth. Many recently proposed switched capacitor converters can achieve unique advantages in uniform device voltage stress and current stress, and can obtain soft charging and soft switching [1]–[10]. Resonant switched-capacitor circuits requires resonant inductors and many switches to achieve soft-charging, soft-switching and high conversion ratio. The

switched-capacitor stage and the following buck stage are usually decoupled, limiting the system efficiency and power density that can be achieved.

The recently proposed *Linear Extendable Group Operated Point-of-Load* (LEGO-PoL) architecture [5] fits particularly well to high-conversion-ratio high-output-current PoL applications. The LEGO-PoL architecture merges the operation of the switched capacitor stage and the multiphase buck stage and creates unique opportunities to improve the efficiency and power density. It eliminates the resonant inductors and the decoupling capacitors in hybrid-switched-capacitor circuits, and merges the operation of the switched-capacitor stage and the buck stage to create soft-charging and soft-switching opportunities. It offers automatic voltage balancing and current sharing, which are important for high-conversion-ratio, high-output-current applications. It leverages the high performance of low voltage DrMOS devices and multiphase buck control. This paper systematically investigates the soft-charging, current sharing, and voltage balancing mechanisms of the LEGO-PoL architecture, and shows enhanced experimental results with a 450 W, 48 V–1.5 V, 300 A LEGO-PoL prototype which achieves a peak efficiency of 96%, a full load efficiency of 87.7%, and a power density of 577 W/in<sup>3</sup>.

## II. PRINCIPLES OF THE LEGO-PO L ARCHITECTURE

Fig. 1 shows one submodule of the LEGO-PoL architecture including a 2:1 switched-capacitor unit and a single-phase buck unit. There is no dc-decoupling capacitor between the two units. Many 2:1 switched-capacitor units can be stacked in series on the input side. They usually operate at a lower switching frequency. Many buck units can be connected in parallel on the output side. They usually operate at a higher frequency. The inductors of the buck units charge and discharge the capacitors of the switched-capacitor unit with soft-charging. The capacitors ( $C_{F1}$  &  $C_{F2}$ ) of the switched-capacitor unit are used as the input capacitors of the buck unit.

Fig. 2 shows the topology of an example LEGO-PoL converter with three series-stacked 2:1 switched-capacitor units and three parallel connected 4-phase buck units. The three switched-capacitor units convert 48 V to 8 V ( $3 \times 2:1=6:1$ ), and the three 4-phase buck units convert 8 V to 1.5 V and share 300 A. The 8 V bus virtually exists and there is no decoupling capacitor between the switched-capacitor unit and 4-phase buck unit. Each of 4-phase buck units uses capacitors

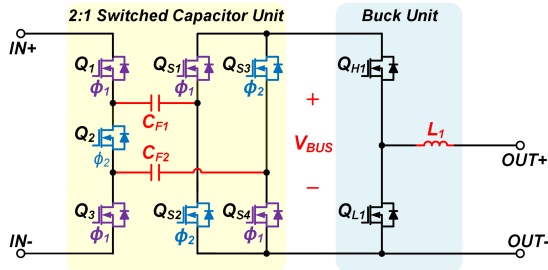


Fig. 1. One submodule of the LEGO-PoL architecture including a 2:1 switched-capacitor unit and a buck unit. Many 2:1 switched-capacitor units can be connected in series to split the input voltage; many buck units can be connected in parallel to share the output current. There is no de-decoupling capacitor between the two units.

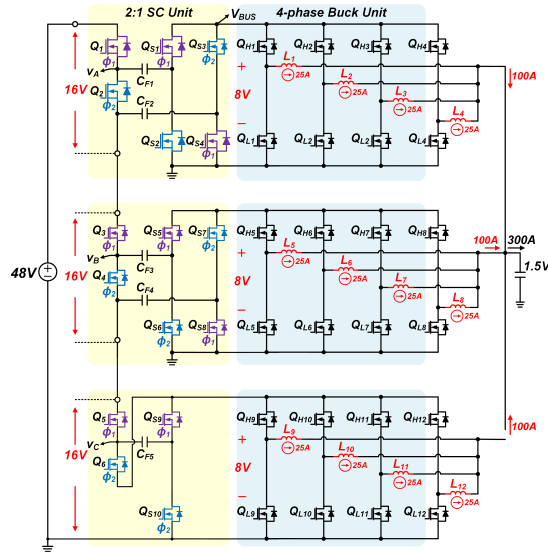


Fig. 2. A 48 V-1.5 V LEGO-PoL design with three stacked submodules. The input ports of the submodules are connected in series, and the output ports of the submodules are connected in parallel. The number of submodules can be *Linearly Extended* and they are *Group Operated*.

of its switched-capacitor stage as the input capacitor, and the inputs of the multiple 4-phase buck units are separated. The switched-capacitor units operate at a lower frequency (e.g., 100 kHz), and the multi-phase buck units operate at a higher frequency (e.g., 1 MHz). The dual-frequency operation enables high converter bandwidth for the microprocessors while offering high efficiency and high power density for the power conversion. As illustrated in Fig. 3, the operations of the two stages are highly integrated in the two operation states (the buck units are modeled as current sources). The multi-phase buck units function as current sources to soft-charge the capacitors in the switched-capacitor units – the capacitors are never connected in parallel with each other. The capacitors in the switched-capacitor units are used as the decoupling capacitors for the buck units.

The LEGO-PoL architecture can be *Linearly Extended* to cover a wide range of input voltage and output current range. These building blocks are *Group Operated* with synchronized

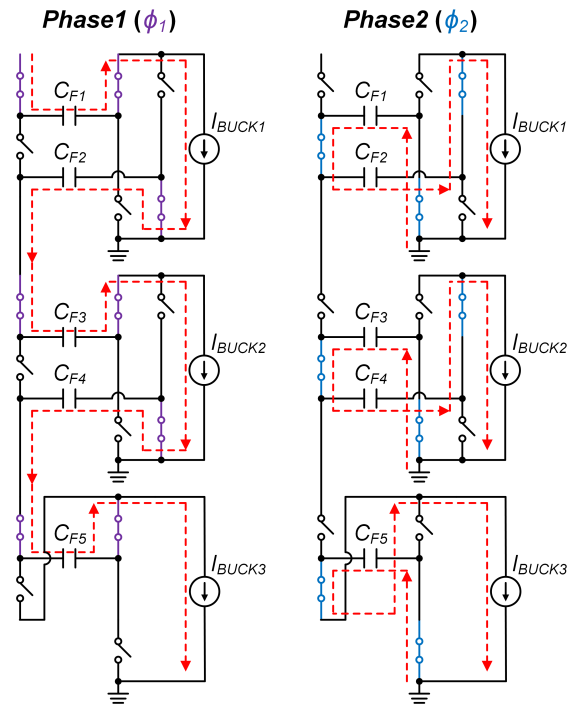


Fig. 3. Current transfer mechanism of LEGO-PoL. The capacitors in the switched-capacitor units are always “soft” charged and discharged by a current source (the buck inductor).

control signals. For example, in Fig. 2, three 16 V, 100 A submodules are connected with their input in series to block the high input voltage (48 V), and with their output in parallel to carry the high output current (300 A). The number of the switched-capacitor units can be linearly extended to cover a wider input voltage range; the number of the parallel units can be linearly extended (by adding more series and parallel units) to cover higher output current range.

Fig. 4 compares the merged-two-stage architecture against a few other existing single-stage and two-stage hybrid switched-capacitor designs. Table I lists the key advantages and disadvantages of each design. The merged-two-stage architectures decoupled the challenge of performing voltage conversion and high control bandwidth by operating at two different frequencies - the switched-capacitor units operate at a lower frequency (kHz range), and the multi-phase buck units operate at a higher frequency (MHz range). The decoupled operation of the merged-two-stage design offers unique zero-current-switching (ZCS) and soft-charging opportunities for the switched-capacitor units. The merged-two-stage architecture can also support a large number of interleaved current phases (e.g., 32 phases). It can leverage the state-of-the-art control techniques that have been developed for standard voltage regulation modules (VRMs). The architecture also decouples the high voltage stress on the input side and the high current stress on the output side by leveraging the series-input parallel-output configuration.

A two-stage architecture usually requires bulky buffering capacitors and many resonant inductors if resonant switched-

TABLE I  
COMPARISONS BETWEEN A FEW HYBRID SWITCHED-CAPACITOR PoL TOPOLOGIES

Topology	Single Stage Series Capacitor Multiphase Buck	Single Stage Switched Capacitor Multiphase Buck	Two-Stage Switched Tank & Multiphase Buck	Merged-Two-Stage Switched Tank & Multiphase Buck
Frequency	Single Frequency	Single Frequency	Dual Frequency	Dual Frequency
Soft Charging	Yes	Conditioned	Yes	Yes
Magnetics	Buck-Only	Buck-Only	Resonant & Buck	Buck-Only
Charging Current	Narrow Pulse	Narrow Pulse	Sinusoidal Wave	Square Wave
ZCS	No	No	Yes	Yes
Extendability	Limited Phase	Limited Phase	Unlimited Phase	Unlimited Phase
Bandwidth	Limited	Limited	High	High
Reference	[9], [10]	[3], [4]	[1], [2]	This work (LEGO-PoL)

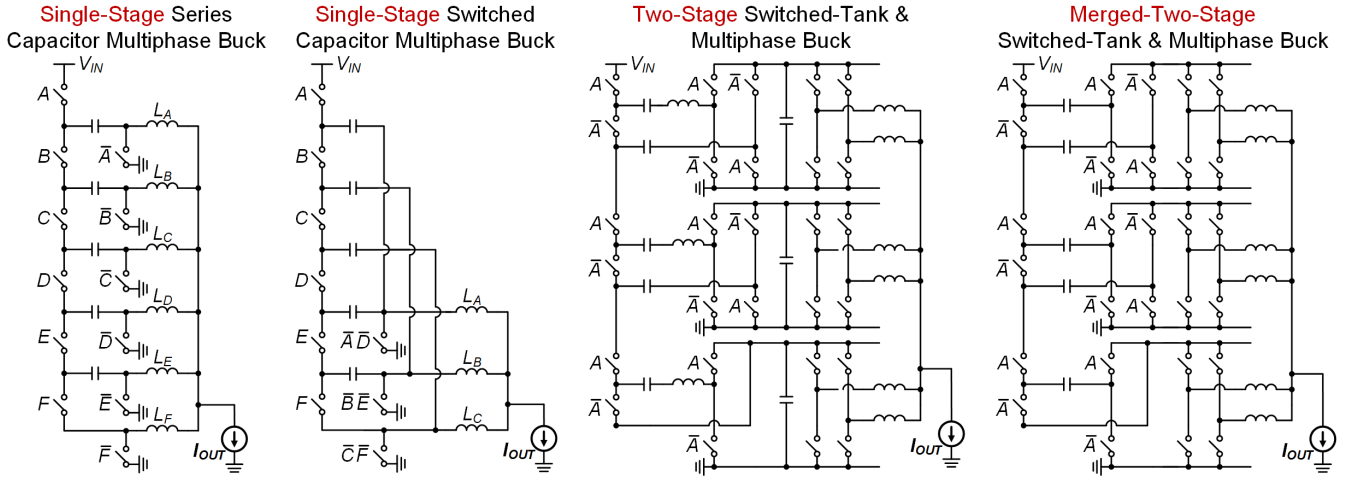


Fig. 4. A few hybrid switched-capacitor PoL topologies: a) Single-stage series capacitor multiphase buck, b) Single-stage switched-capacitor multiphase buck, c) Two-stage switched-tank & multiphase buck, and d) Merged-two-stage switched-tank & multiphase buck.

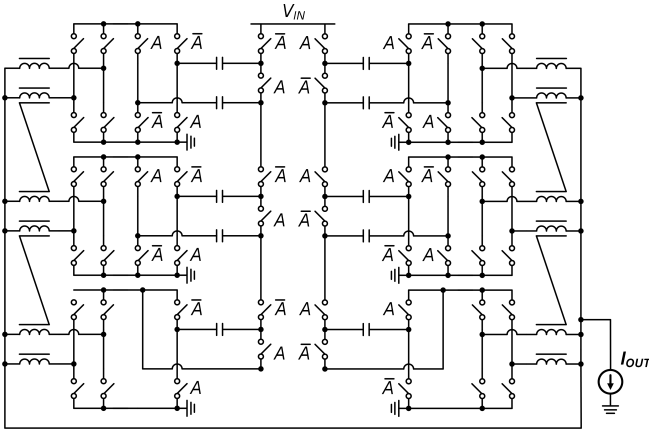


Fig. 5. Extended embodiment of the LEGO-PoL converter with two interleaved input stacks and many coupled output inductors.

capacitor topologies are adopted. Single-stage architectures are usually smaller and more efficiency, but they face the challenge in control. The topology in Fig. 4(a) and Fig. 4(b) need to operate in “split-phase” and/or with capacitance matching to achieve soft charging. The merged-two-stage architecture can offer comparable efficiency and power density as single-stage architectures, and can achieve comparable control performance as a two-stage solution. They have the capability of supporting

coupled inductors and “merged-phase” operation during fast transient [14]–[16]. Advanced voltage-mode or current-mode strategies can be directly applied. Fig. 5 shows an extended embodiment of the LEGO-PoL architecture with 1) interleaved input switches; and 2) cross-coupled multi-phase inductors. This architecture can completely eliminate the input current ripple (50% duty ratio), and can achieve very fast transient response (as a multiphase buck with coupled inductors).

### III. OPERATION MECHANISMS

The LEGO-PoL architecture decouples the voltage stress, current stress, and the dynamic requirements in a high current PoL converter and optimally addresses these design challenges. In this section, we investigate the soft charging, current sharing, and voltage balancing mechanisms in detail.

#### A. Soft Charging

As illustrated in Fig. 3, by combining a 2:1 switched-capacitor unit and a multi-phase buck unit and eliminating the decoupling capacitor between two units, the capacitors of the switched-capacitor units are always charged and discharged by the buck inductors, enabling full soft charging operation. Since the capacitors in the switched-capacitor stage are reused as the input capacitors for the multiphase buck stage, the soft-charging current loop should be extremely compact.

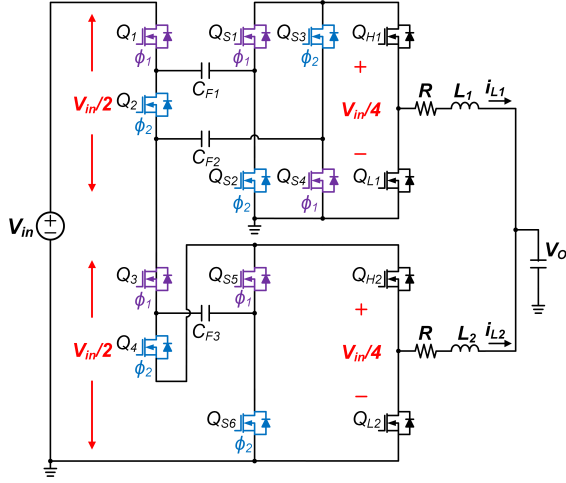


Fig. 6. Topology of a 2-stack LEGO-PoL converter with 36 V input voltage and 1.5 V output voltage for investigating the current sharing mechanism.

### B. Automatic Current Sharing and Voltage Balancing

The automatic current sharing and voltage balancing mechanism of the LEGO-PoL architecture can be explained by analyzing the current flow in the two switching phases in Fig. 3. In each switching cycle, capacitor  $C_{F1}$ ,  $C_{F3}$ , and  $C_{F5}$  are charged by one current source in  $\phi_1$ , and discharged by another current source in  $\phi_2$ , similar for  $C_{F2}$  and  $C_{F4}$ . Since the switched-capacitor converter operates with 50% duty ratio, the two current sources have to be equal, leading to current sharing between two adjacent modules, and sequentially current sharing to all modules. For example,  $C_{F2}$  is discharged by  $I_{BUCK2}$  in  $\phi_1$ , and charged by  $I_{BUCK1}$  in  $\phi_2$ .  $C_{F3}$  is charged by  $I_{BUCK2}$  in  $\phi_1$ , and discharged by  $I_{BUCK2}$  in  $\phi_2$ . To maintain the charge balance in  $C_{F2}$  and  $C_{F3}$ ,  $I_{BUCK1}$  has to be equal to  $I_{BUCK2}$  in steady state operation.

In order to illustrate the current sharing mechanism quantitatively, we perform a large signal average analysis on a  $n = 2$  design in Fig. 6. Assume each buck converter connected to the switched-capacitor stage is a single phase buck with inductance  $L$ , and  $L$  is connected with a series resistance  $R$  (representing the resistance of the buck converter including conduction loss and switching loss); Assume the duty ratio of the buck converter, i.e., the duty ratio of high side switches, is  $D$ , the large-signal average current of inductor  $L_x$  is  $i_x$ , the large-signal average voltage of capacitor  $C_{Fx}$  is  $v_x$ .

The large-signal average model equations includes:

$$\begin{aligned} L_1 \frac{di_{L1}}{dt} &= \langle v_{L1} \rangle = \frac{1}{2}(V_{in} - v_2)D - v_o - i_{L1}R, \\ L_2 \frac{di_{L2}}{dt} &= \langle v_{L2} \rangle = \frac{1}{2}v_2D - v_o - i_{L2}R, \\ C_{F2} \frac{dv_2}{dt} &= \langle i_{CF2} \rangle = \frac{1}{2}(Di_{L1} - Di_{L2}). \end{aligned} \quad (1)$$

$$\frac{d^2(i_{L1} - i_{L2})}{dt^2} + \frac{R}{L} \frac{d(i_{L1} - i_{L2})}{dt} + \frac{D^2}{2LC_{F2}}(i_{L1} - i_{L2}) = 0. \quad (2)$$

Unlike a traditional buck converter, the charge balance

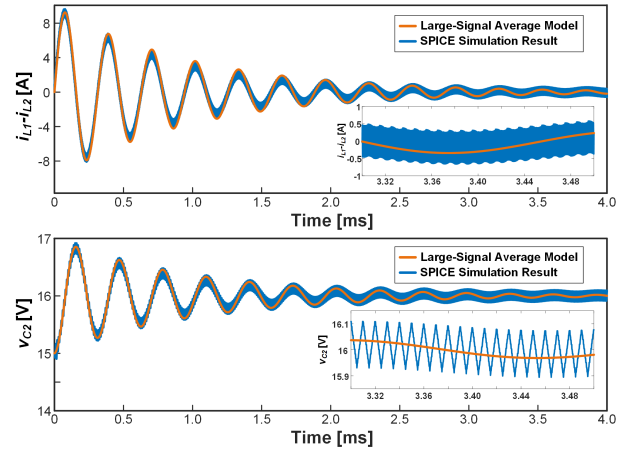


Fig. 7. Large-signal average model and SPICE simulated transient waveforms of the automatic current sharing dynamics. The model was derived with  $V_{in}=32$  V,  $D=0.2$ ,  $L_x=1$   $\mu$ H,  $C_{Fx}=45$   $\mu$ F, and  $R=2$  m $\Omega$ .

requirement of capacitor  $C_{F2}$  leads to the automatic current sharing mechanism between  $L_1$  and  $L_2$ . Assuming that  $L_1=L_2=L$ , a second-order differential equation with explicit solutions (2) describes the large-signal dynamics of the current difference as a function of the circuit parameters and initial conditions. The natural frequency  $\omega_n$  of this second order oscillation system is  $\frac{D}{\sqrt{2LC_{F2}}}$ . The damping ratio  $\zeta$  is  $\frac{R}{2D} \sqrt{\frac{2C_{F2}}{L}}$ . The decay rate  $\alpha$  is  $\frac{R}{2L}$ , the quality factor  $Q$  is  $\frac{D}{R} \sqrt{\frac{L}{2C_{F2}}}$ . The current difference will respond to perturbations like a second-order system, and gradually decay to zero in periodic steady state. The current sharing mechanism of the LEGO-PoL converter is very similar to that of series-capacitor buck converter [10]. Note  $C_{F1}$  and  $C_{F3}$  have no impact on the current sharing dynamics.

As illustrated in Fig. 7, the large-signal average modeling results match well with the SPICE simulation results. In periodic steady state, the large signal current  $i_{L1}=i_{L2}$ , and  $\frac{di_{L1}}{dt} = \frac{di_{L2}}{dt} = 0$ , as a result, the average voltage of  $C_{F2}$ ,  $v_2$  equals  $\frac{1}{2}V_{in}$ . This mechanism holds the large-signal average of  $v_2$  at  $\frac{1}{2}V_{in}$ . Since  $C_2 \frac{dv_2}{dt} = \frac{D}{2}(i_{L1} - i_{L2})$ , the transient dynamics of the capacitor voltage follows a similar second-order transient dynamics (similar damping ratio and  $Q$ ) as  $i_{L1} - i_{L2}$  and gradually damps to  $\frac{1}{2}V_{in}$  following the same oscillation.  $V_2$  will be automatically maintained at 16 V in this example implementation.

A small buffer capacitor (in the nF scale) is placed between the switched-capacitor units and buck units to filter the high frequency current and maintain the voltage of  $C_{F1}$  and  $C_{F3}$  at 9 V and 27 V while not disturbing soft-charging.

Similar analysis can be extended to higher order designs. Assuming  $L_1=L_2=L_3=L$  and  $C_{F2}=C_{F4}=C$ , the large-signal average model for a three submodule LEGO-PoL system is:

$$\ddot{\mathbf{X}} + \frac{R}{L}\dot{\mathbf{X}} + \frac{D^2}{4LC}\mathbf{M}\mathbf{X} = 0,$$

$$\ddot{\mathbf{X}} = \begin{bmatrix} \frac{d^2 i_{L1}}{dt^2} \\ \frac{d^2 i_{L2}}{dt^2} \\ \frac{d^2 i_{L3}}{dt^2} \end{bmatrix}, \quad \dot{\mathbf{X}} = \begin{bmatrix} \frac{di_{L1}}{dt} \\ \frac{di_{L2}}{dt} \\ \frac{di_{L3}}{dt} \end{bmatrix}, \quad \mathbf{X} = \begin{bmatrix} i_{L1} \\ i_{L2} \\ i_{L3} \end{bmatrix},$$

$$\mathbf{M} = \begin{bmatrix} 1 & -1 & 0 \\ -1 & 2 & -1 \\ 0 & -1 & 1 \end{bmatrix},$$

$$\mathbf{Q} = \begin{bmatrix} -0.577 & -0.707 & 0.408 \\ -0.577 & 0 & -0.816 \\ -0.577 & 0.707 & 0.408 \end{bmatrix}, \quad \mathbf{A} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 3 \end{bmatrix}.$$

Note  $\mathbf{M}$  is a real symmetric matrix.  $\mathbf{M}$  can be diagonalized as  $\mathbf{M}=\mathbf{Q}\mathbf{A}\mathbf{Q}^{-1}$  where  $\mathbf{Q}$  is a matrix composed of eigenvectors ( $e_1, e_2$ , and  $e_3$ ), and  $\mathbf{A}$  is a diagonal matrix composed of eigenvalues ( $\lambda_1, \lambda_2$ , and  $\lambda_3$ ) of  $\mathbf{M}$  respectively. (3) can be rewritten as (4) by denoting  $\mathbf{Y}=\mathbf{Q}^{-1}\mathbf{X}$ .

$$\ddot{\mathbf{Y}} + \frac{R}{L}\dot{\mathbf{Y}} + \frac{D^2}{4LC}\mathbf{A}\mathbf{Y},$$

$$\frac{d^2 y_1}{dt^2} = \frac{R}{L} \frac{dy_1}{dt} + \frac{D^2}{4LC}(\lambda_1 y_1) = 0,$$

$$\frac{d^2 y_2}{dt^2} = \frac{R}{L} \frac{dy_2}{dt} + \frac{D^2}{4LC}(\lambda_2 y_2) = 0,$$

$$\frac{d^2 y_3}{dt^2} = \frac{R}{L} \frac{dy_3}{dt} + \frac{D^2}{4LC}(\lambda_3 y_3) = 0.$$

Since  $i_{L1} - i_{L3}$  is the same with  $y_2$ , the second-order differential equation of  $(i_{L1} - i_{L3})$  is:

$$\frac{d^2(i_{L1} - i_{L3})}{dt^2} + \frac{R}{L} \frac{d(i_{L1} - i_{L3})}{dt} + \frac{D^2}{4LC}(i_{L1} - i_{L3}) = 0. \quad (5)$$

This second-order differential equation describes the large-signal dynamics of the current difference in the three submodule design. The current difference gradually damps to zero in periodic steady state. For this reason, the average voltages of  $C_{F2}$  and  $C_{F4}$ ,  $v_2$  and  $v_4$ , reach  $\frac{2V_{in}}{3}$  and  $\frac{V_{in}}{3}$  respectively. As illustrated in Fig. 8, this large-signal average model also matches well with SPICE simulation results. The capacitance  $C_{F1}$ ,  $C_{F3}$ , and  $C_{F5}$  have no impact on the current sharing and voltage balancing. A generalized large signal average model of the LEGO-PoL architecture with arbitrary  $N$  submodules is provided in the Appendix. As proved in the Appendix, automatic current sharing and automatic voltage balancing are guaranteed in a LEGO-PoL architecture with  $N$  submodules.

#### IV. DESIGN CONSIDERATIONS

##### A. Switches of the Switched-Capacitor Stage

The series stacked 2:1 switched-capacitor units split the input voltage into small voltage domains. As a result, the LEGO-PoL converter can use low voltage rating devices with low on-resistance. The voltage ratings of the active switches are

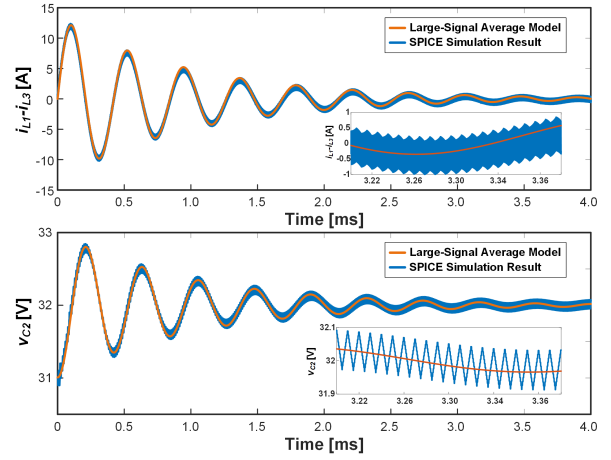


Fig. 8. Large-signal average model and SPICE simulated transient response of the automatic current sharing dynamics for  $n=3$  design. The model was derived with  $V_{in}=48$  V,  $D=0.2$ ,  $L_x=1$   $\mu$ H,  $C_{F_x}=45$   $\mu$ F, and  $R=2$  m $\Omega$ .

either  $V_{BUS}$  or  $2V_{BUS}$ . Unlike a traditional two-stage hybrid-switched-capacitor designs, the voltages across all switches are clamped by the capacitors under all worst case situations. The merged two-stage operation enables switches to operate at lower switching frequency with zero-current-switching (ZCS). For this reason, the switches in the switched-capacitor stage have reduced switching loss compared to other switched-capacitor implementations.

##### B. Capacitors of the Switched-Capacitor Stage

In many hybrid-switched-capacitor designs, the capacitors need to be carefully selected because the capacitance value determines the soft charging, soft-switching and resonant operation. The LEGO-PoL converter eliminates the resonant inductors in traditional resonant-switched-capacitor designs and achieves soft charging operation by using the buck inductors as current sources. Smaller capacitance values with larger voltage ripple are allowed. The capacitance value does not need to be precisely controlled. This allows a variety of capacitors to be used in a LEGO-PoL design. Class-II (e.g., X5R, X5S, X6S, X7R, etc.) MLCC capacitors can be freely considered with high tolerance to dc voltage bias, temperature variation, and capacitance degradation.

##### C. Design of the Multiphase Buck Stage

The buck stage of the LEGO-PoL converter can follow the design considerations of the state-of-the-art standard VRMs using multiphase buck converters. The multiphase buck converters can be interleaved with their inductors coupled with each other. Advanced control techniques are directly applicable. Current sharing is guaranteed across the multiphase buck units belonging to different submodules. For example, in Fig. 2, the LEGO-PoL controller only needs to balance the current of each four-phase buck unit in a 12-phase interleaved operation. In a traditional 12-phase buck converter, the controller needs to balance the current of all 12 phases.



TABLE II  
COMPONENTS LIST OF THE 48 V-1.5 V, 300 A LEGO-PO L CONVERTER

$Q_1$ & $Q_6$	BSZ013N2LS (25V, 1.3m $\Omega$ )
$Q_2$ - $Q_5$	BSZ0501NSI (30V, 2.0m $\Omega$ )
$Q_{S1}$ - $Q_{S10}$	BSZ013N2LS (25V, 1.3m $\Omega$ )
$C_{F1}$ - $C_{F5}$	45 $\mu$ F, 1210, X7R, Murata
$Q_H$ & $Q_L$	SiC632 (DrMOS, 24V, 50A)
$L_1$ - $L_{12}$	1.0 $\mu$ H (HC1-1R0-R, 1.23m $\Omega$ )
Digital Controller	TMS320F28069

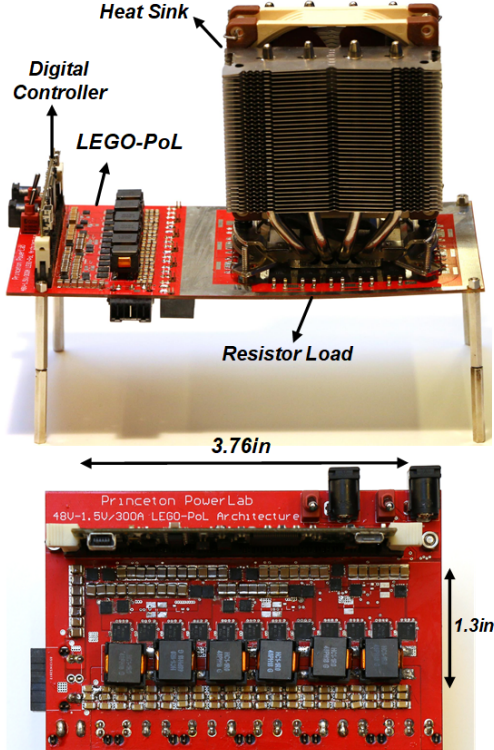


Fig. 9. Picture of the 48 V-1.5 V/300 A LEGO PoL prototype with three series stacked submodules and twelve interleaved buck phases.

#### D. PCB Layout Principles

Eliminating the decoupling capacitor between two stages creates the soft-charging and soft switching opportunities, but brings challenges in printed circuit board layout and design. The capacitors of the switched-capacitor units are reused as the input capacitors of the buck units. As a result, the high frequency current loop between the switched-capacitor units and the buck units should be as small as possible.

### V. EXPERIMENTAL RESULTS

To verify the effectiveness of the LEGO-PoL architecture, a 40 V-60 V input (48 V nominal) and 1.5 V, 300 A output is built and tested. Fig. 9 shows a picture of the prototype. The circuit topology is shown in Fig. 2. Three 2:1 switched-capacitor stages were stacked in series on the input side (48

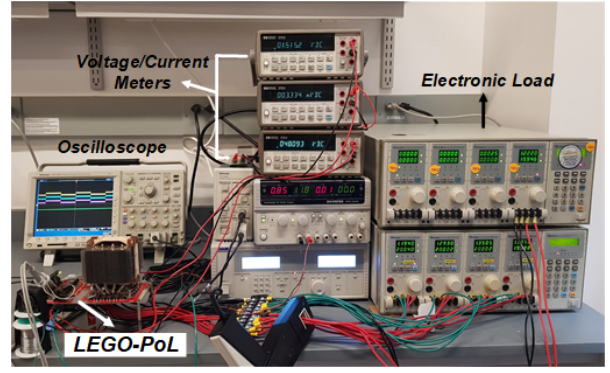


Fig. 10. Picture of the experimental platform including the 48 V/1.5 V 300 A prototype, a few voltage/current meters and a few electronic loads.

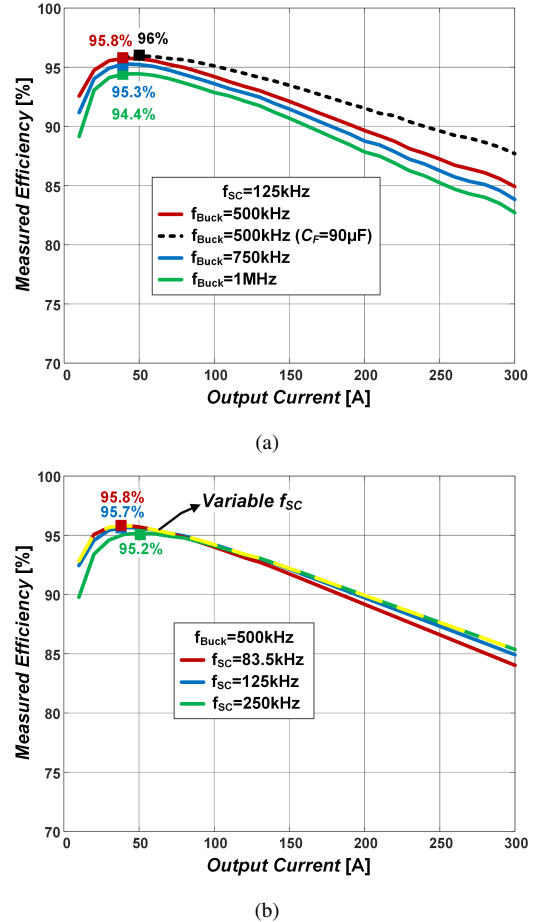


Fig. 11. Measured efficiency of the 48 V-1.5 V 300 A LEGO-PoL system at different operating frequencies: (a) Fix the switched-capacitor frequency at 125 kHz, and sweep the buck frequency; (b) Fix the buck frequency at 500 kHz, and sweep the switched-capacitor frequency.

V), and three 4-phase buck units were connected in parallel on the output side (1.5 V, 300 A). Table II lists the bill-of-material (BOM) of this design. The switches in the switched-capacitor units are implemented as standard MOSFETs. The switches in the multi-phase buck units are implemented as low voltage DrMOS.  $C_{F1}$ - $C_{F5}$  are 45  $\mu$ F. In a traditional two-stage design with similar performance, the capacitor size

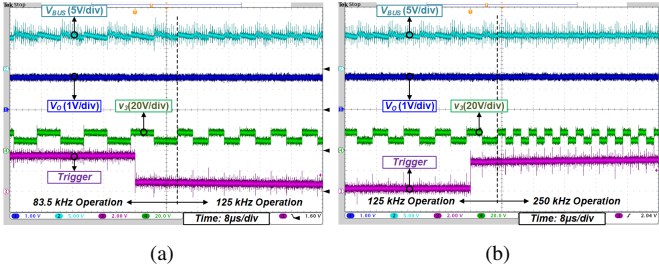


Fig. 12. Measured waveforms during a step change of the switched-capacitor frequency: (a) From 83.5 kHz to 125 kHz; (b) From 125 kHz to 250 kHz. The buck frequency was fixed at 500 kHz.

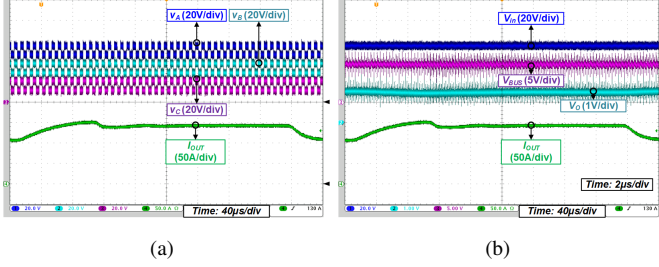


Fig. 13. Measured waveforms during a load step transient (from 100 A to 150 A). (a) Voltages of the switch node in the switched-capacitor units ( $v_A$ ,  $v_B$ ,  $v_C$ ); (b) Input voltage ( $V_{in}$ ), bus voltage ( $V_{BUS}$ ), and output voltage ( $V_O$ ).

would be 150  $\mu$ F. 500 nF 0603 size capacitors are used as input capacitors of the DrMOS. The buck inductor is 1  $\mu$ H. The power density of the prototype (considering the power stage) is 577 W/in<sup>3</sup>. Fig. 10 shows a picture of the experimental platform. We connected two Chroma 63103A in parallel as the electronic load. Agilent 34401 and 34330A current shunt were used for measuring efficiency. A Tektronix current probe (TCP404XL & TCPA400) was used to measure the transient of the current waveform.

Fig. 11 shows the measured efficiency of the 48 V–1.5 V 300 A LEGO-PoL system. The buck stage and the switched capacitor stage are operating at different frequencies. The peak efficiency of the 48 V–1.5 V system is 95.75% at 40 A, and 85% at 300 A with  $f_{Buck}$ =500 kHz, and  $f_{SC}$ =125 kHz. If  $C_F$  was increased to 90  $\mu$ F, the system peak efficiency and full load efficiency were increased to 96% and 87.7%, respectively. In a traditional hybrid-switched-capacitor design, the switching frequency usually needs to be fixed to maintain resonant operation and maintain soft switching. By modulating the switching frequency, the LEGO-PoL converter can achieve higher performance across a wide operation range. The power density of the prototype is 577 W/in<sup>3</sup> (power stage only). Fig. 12 shows the transient waveforms when the switched-capacitor operating frequency changes. As the switching frequency increases, the ripples in the bus voltage are reduced. The average value of bus voltage and output voltage are well maintained, and the capacitor voltages are well balanced.

Fig. 13 shows the transient response of the prototype when the load steps between 100 A and 150 A. The voltages of the switch node in the switched-capacitor units ( $v_A$ ,  $v_B$ , and  $v_C$ ) maintains the same during transient, indicating automatic

current sharing and voltage balancing. The intermediate bus voltage ( $V_{BUS}$ ) and output voltage ( $V_O$ ) are also well regulated during the load step change.

## VI. CONCLUSIONS

This paper presents a family of LEGO-PoL converters with merged-two-stage operation for very high current microprocessors. By merging the operation of the switched-capacitor units and the multi-phase buck units, a LEGO-PoL converter can achieve soft charging and ZCS operation without resonant inductors. The merged-two-stage operation also enables high control bandwidth for voltage regulation while offering high efficiency and high power density. The LEGO-PoL system can be linearly extended by adding more switched-capacitor or multiphase buck building blocks with automatic voltage balancing and current sharing. A 48 V–1.5 V 300 A CPU power supply has been built and tested to verify the effectiveness of the LEGO-PoL architecture. The peak efficiency of the prototype is 96%. The full load efficiency of the system is 87.7%. The power density of the prototype is 577 W/in<sup>3</sup>.

## ACKNOWLEDGMENT

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## APPENDIX

This appendix investigates the current sharing and voltage balancing mechanisms of the LEGO-PoL architecture with  $N$  submodules. Assuming that  $L_1 = L_2 = \dots = L_N = L$ , and  $C_{F2} = C_{F4} = \dots = C_{F(2(N-1))} = C$ , the large-signal average model of the system is:

$$\ddot{\mathbf{X}} + \frac{R}{L}\dot{\mathbf{X}} + \frac{D^2}{4LC}\mathbf{M}\mathbf{X} = 0,$$

$$\ddot{\mathbf{X}} = \begin{bmatrix} \frac{d^2 i_{L1}}{dt^2} \\ \frac{d^2 i_{L2}}{dt^2} \\ \vdots \\ \frac{d^2 i_{LN}}{dt^2} \end{bmatrix}, \quad \dot{\mathbf{X}} = \begin{bmatrix} \frac{di_{L1}}{dt} \\ \frac{di_{L2}}{dt} \\ \vdots \\ \frac{di_{LN}}{dt} \end{bmatrix}, \quad \mathbf{X} = \begin{bmatrix} i_{L1} \\ i_{L2} \\ \vdots \\ i_{LN} \end{bmatrix}, \quad (6)$$

$$\mathbf{M} = \begin{bmatrix} 1 & -1 & 0 & 0 & \dots & 0 \\ -1 & 2 & -1 & 0 & \dots & 0 \\ 0 & -1 & 2 & -1 & \dots & 0 \\ \vdots & \vdots & \vdots & \ddots & \dots & \vdots \\ 0 & 0 & \dots & -1 & 2 & -1 \\ 0 & 0 & \dots & 0 & -1 & 1 \end{bmatrix}.$$

$$\mathbf{x}^T \cdot \mathbf{M} \cdot \mathbf{x} = \sum_{k=1}^{N-1} (x_{k+1} - x_k)^2 \geq 0 \quad (7)$$

$\mathbf{M}$  is a  $N \times N$  real symmetric matrix, so it can be diagonalized as  $\mathbf{M} = \mathbf{Q}\mathbf{\Lambda}\mathbf{Q}^{-1}$ , where  $\mathbf{Q} = [e_1, e_2, \dots, e_N]$  and  $\mathbf{\Lambda}$  is the diagonal matrix consisting of eigenvalues ( $\lambda_1, \lambda_2, \dots, \lambda_N$ ).

For any non-zero  $\mathbf{x}=[x_1, x_2, \dots, x_N]^T$ ,  $\mathbf{M}$  satisfies (7), so  $\mathbf{M}$  is positive semidefinite, i.e.  $\lambda_k \geq 0$  ( $k = 1, 2, \dots, N$ ). The rank of  $\mathbf{M}$  is  $N - 1$ , so there exists and only exists one zero eigenvalue. Assuming  $\lambda_1 = 0$ , and the corresponding  $\mathbf{e}_1$  can be found as  $[1, 1, \dots, 1]^T$ . Denoting  $\mathbf{Y}=\mathbf{Q}^{-1}\mathbf{X}$ , then (6) can be rewritten as (8) with explicit solutions:

$$\begin{cases} \frac{d^2 y_1}{dt^2} + \frac{R}{L} \frac{dy_1}{dt} = 0, & k = 1, \\ \frac{d^2 y_k}{dt^2} + \frac{R}{L} \frac{dy_k}{dt} + \left(\frac{D^2}{4LC} \lambda_k\right) y_k = 0, & k = \{2, 3, \dots, N\} \end{cases} \quad (8)$$

The general solutions for (8) are:

$$\begin{cases} y_1(t) = K_{11}e^{-\alpha t} + K_{12}, \\ y_{k(k \geq 2)}(t) = K_{k1}e^{-\alpha + \frac{\sqrt{\alpha^2 - 4\beta_k^2}}{2}t} + K_{k2}e^{-\alpha - \frac{\sqrt{\alpha^2 - 4\beta_k^2}}{2}t}, \end{cases} \quad (9)$$

where  $K_{k1}$  and  $K_{k2}$  are constant coefficients,  $\alpha = \frac{R}{L}$ , and  $\beta_k = \frac{D^2 \lambda_k}{4LC}$ . Since  $\alpha$  is larger than zero,  $y_1(t)$  damps to  $K_{12}$ , and  $y_{k(k \geq 2)}(t)$  damps to zero as time goes to infinity. When there are repeated roots for the characteristic equation,  $y_{k(k \geq 2)}(t)$  have similar form as (9) and also damp to zero as time goes to infinity. Therefore, in periodic steady state, the large signal inductor currents of the LEGO-PoL architecture with  $N$  submodules settle to the same constant value  $K_{12}$ :

$$\begin{bmatrix} i_{L1} \\ i_{L2} \\ \vdots \\ i_{LN} \end{bmatrix} = \mathbf{Q}^{-1}\mathbf{Y} = [\mathbf{e}_1, \mathbf{e}_2, \dots, \mathbf{e}_N] \begin{bmatrix} K_{12} \\ 0 \\ \vdots \\ 0 \end{bmatrix} = \begin{bmatrix} K_{12} \\ K_{12} \\ \vdots \\ K_{12} \end{bmatrix}. \quad (10)$$

Similarly, the average capacitor voltages of  $V_{CF2}, V_{CF4}, \dots, V_{CF(2(N-1))}$  damp to a balanced voltage:

$$\begin{bmatrix} V_{CF2} \\ V_{CF4} \\ \vdots \\ V_{CF(2(N-1))} \end{bmatrix} = \frac{V_{in}}{N} \begin{bmatrix} N-1 \\ N-2 \\ \vdots \\ 1 \end{bmatrix}. \quad (11)$$

Fig. 14 shows the SPICE verification of the dynamic model of a  $n = 7$  design. The charge balancing mechanism of the capacitors maintains the current sharing and voltage balancing for the LEGO-PoL architecture with a large number of modular building blocks.

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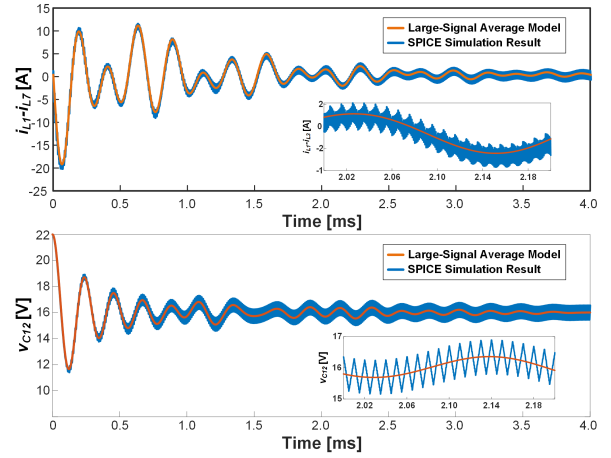


Fig. 14. SPICE verification of the dynamic model for a  $n = 7$  design. The model was derived with  $V_{in}=112$  V,  $D=0.2$ ,  $L_x=1$   $\mu$ H,  $C_{Fx}=45$   $\mu$ F, and  $R=2$  m $\Omega$ . The deviation of the capacitor voltages  $V_{CF2}, V_{CF4}, \dots, V_{CF12}$  from balanced values are  $-1V, +2V, -3V, \dots, +6V$ . The derived model matches very well with simulation results.

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