A "Reverse-Feeding" Hold-up Time Strategy for Two-Stage Grid-Interface PFC with a Rectifier-Coupled Boost Inductor

Jaeil Baek†, Gun-Woo Moon‡, Minjie Chen†
†*Princeton University, Princeton, NJ, United States*
‡*KAIST, Daejeon, Republic of Korea*
Email: †{*jaeil.baek, minjie*}*@princeton.edu;* ‡*gwmoon@kaist.ac.kr*

***Abstract*—This paper presents a "reverse-feeding" hold-up time strategy to improve the performance of two-stage grid-interface power factor correction (PFC) circuit with a rectifier-coupled boost inductor. During the hold-up time, instead of delivering the energy only through the dc-dc converter (e.g., a LLC converter, or a phase-shift full-bridge (PSFB) converter), the energy stored in the energy-buffer capacitor is also transferred through an extra-winding on the boost inductor to the secondary side. This additional energy transfer path regulates the output voltage during the hold-up time and offers extra flexibility to optimize the system performance during normal operation and hold-up time. With this configuration, the dc-dc converter can be designed as a almost fixed ratio dc transformer. The "reverse-feeding" strategy can extend the HUT by 25%, reduce the energy-buffer capacitor size by 25%, improve the system peak efficiency (96.5%) and enhance the power density. The effectiveness of the proposed method is verified by a PFC prototype with 100V-240V_{rms} ac input and 800W, 12V/66.7A dc output.**

***Index Terms*—High efficiency, high power density, hold-up time (HUT), phase-shift-full-bridge converter, power factor correction (PFC) converter**

I. Introduction

Grid-interface ac-dc power supplies typically consist of a power factor correction (PFC) stage and a dc-dc stage, as illustrated in Fig. 1(a). They need to meet the grid-interface and efficiency requirements [1]–[3]. The PFC stage is usually implemented as a boost converter [4]–[6]. The dc-dc stage is usually implemented as a LLC converter or phase-shift-full-bridge converter which can offer high performance across wide operation range [7]–[14]. Ac-dc converters also need to meet the hold-up time (HUT) requirement [11]–[15] to avoid abrupt shut-down and maintain the operation of equipment for a few milliseconds (a few line cycles) if ac line is lost. Fig. 1(b) illustrates the operation principles and key waveforms of typical grid-interface ac-dc power supply. In normal operation when ac line is ON and high efficiency is required, the boost PFC converter provides constant bus voltage (V_{B-Reg}) and the dc-dc converter regulates the output voltage (V_O). In conventional designs, the boost PFC does not operate during the hold-up time (HUT) when the ac line is OFF. The dc-dc converter keeps functioning to transfer the energy stored in the energy-buffer capacitor (C_B) to the output port. Thus, the HUT is determined by the energy-buffer capacitor and the regulation range of the dc-dc converter.

There are two ways to extend the HUT. One way is to increase the size of the energy-buffer capacitor. By decreasing

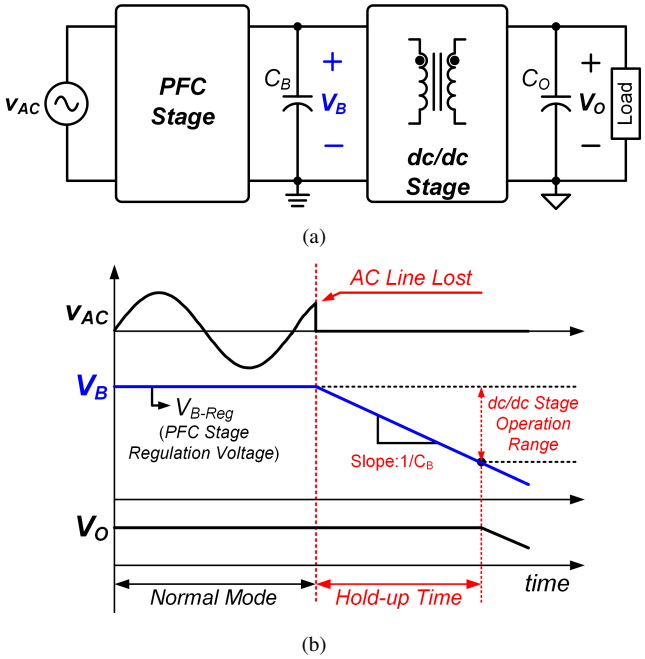


Fig. 1. Typical grid-interface ac-dc power supply. (a) Block diagram. (b) Operation modes and key waveforms.

the slope of bus voltage drop, the dc-dc converter can be designed with narrower input voltage range which usually results in higher efficiency. However, since the size of capacitor increases as its capacitance increases, this approach reduces the system power density. The other way is to extend the operation range of the dc-dc converter [11]–[14]. Wider operation range of the dc-dc converter allows the utilization of smaller energy-buffer capacitor. There is a strong design tradeoff between the operation range of the dc-dc converter and the size of the energy-buffer capacitor. Usually, the operation range is restricted to 80% to 90% of V_{B-Reg} [15]. For example, if the dc-dc converter is designed for wide-operation range, its transformer turns-ratio is usually low, so that it can cover the HUT with small energy-buffer capacitor. However, in normal operation, the effective duty ratio of the dc-dc is small, the efficiency may drop due to the significant circulating current, magnetic core loss, and other losses.

To break the above mentioned tradeoff boundaries, many hold-up time extension strategies have been proposed. Most

methods usually only focus on the dc-dc converter [11]–[14]. In [11], [12], the transformer turns ratio can be adjusted by including more semiconductor devices. In normal operation, higher transformer turns ratio enabled higher efficiency. During the HUT, lower transformer turns-ratio is used. In [13], the duty ratio loss is controlled by additional semiconductor devices. By nearly eliminating duty-cycle loss during the HUT, the operation range of the dc-dc converter is extended. In [14], a hybrid PWM-PFM control strategy is used with additional inductors and capacitors. By adopting PFM control during the HUT, it can extend its operation range and regulate the output voltage without abrupt voltage gain variation.

In [15], an additional boost converter is added between two split buffer capacitors. In normal operation, the boost converter is turned off and the two buffer capacitors function together. During the HUT, the two split capacitors are used as the input capacitor and the output capacitor of the boost converter to extract more energy from the buffer capacitor. Thus, it can extend the HUT and offer high efficiency and good voltage regulation performance in HUT transient operation. However, one additional diode is needed between two split buffer capacitors, introducing additional conduction loss during the normal operation. Moreover, the hard switching operation of the additional boost converter brings additional thermal constraints.

This paper proposes a "reverse-feeding" strategy for two-stage ac-dc PFC converters to achieve both high efficiency in normal operation and extended HUT. In the "reverse-feeding" strategy, an additional winding is added on the boost inductor to create an additional energy transfer path from the energy-buffer capacitor to the rectifier. Both the dc-dc converter and the boost converter can be used to regulate the output voltage during the HUT. Thus, the dc-dc converter does not need to be designed for the full operation range and can be optimized to achieve higher efficiency during normal operation. The boost converter with a rectifier-coupled boost inductor can be designed to extend the HUT and optimize the peak system efficiency. Moreover, the boost converter does not require additional heat sink due to its soft switching operation.

II. "Reverse-Feeding" HUT Strategy

A. Key Concepts

In a conventional two-stage PFC design, the boost converter is usually deactivated during the HUT (Fig. 2(a)). The dc-dc converter solely regulates the output voltage. As illustrated in Fig. 2(b), by adding one additional winding on the boost inductor, the boost converter can create an additional energy transfer path from the energy-buffer capacitor to the output. This energy transfer path creates additional design flexibility for the dc-dc converter. The topology in Fig. 2(b) comprises a half-bridge (HB) structure composed of two boost switches (Q_S and Q_B), one boost inductor (L_B), and a series connected capacitor (C_{in}). By coupling the boost inductor to the rectifier side with an additional winding (N_B), the boost converter of the PFC can be used as a half-bridge converter (forward, flyback, resonant, or dual-active bridge converter) during the

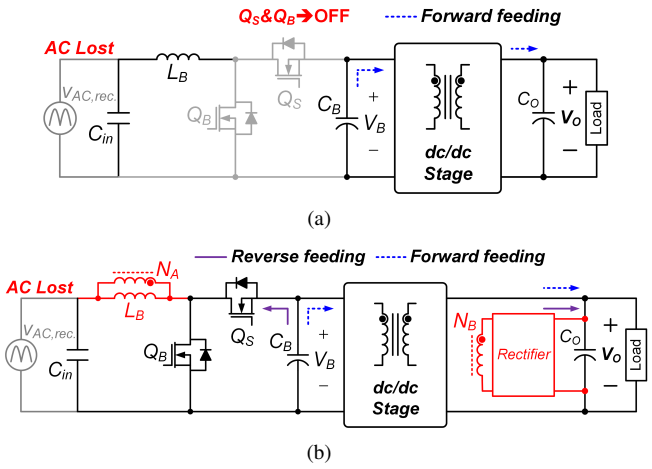


Fig. 2. Power flow of the ac-dc PFC circuit. (a) Power flow in a conventional two-stage PFC. (b) Power flow in the PFC with "reverse-feeding".

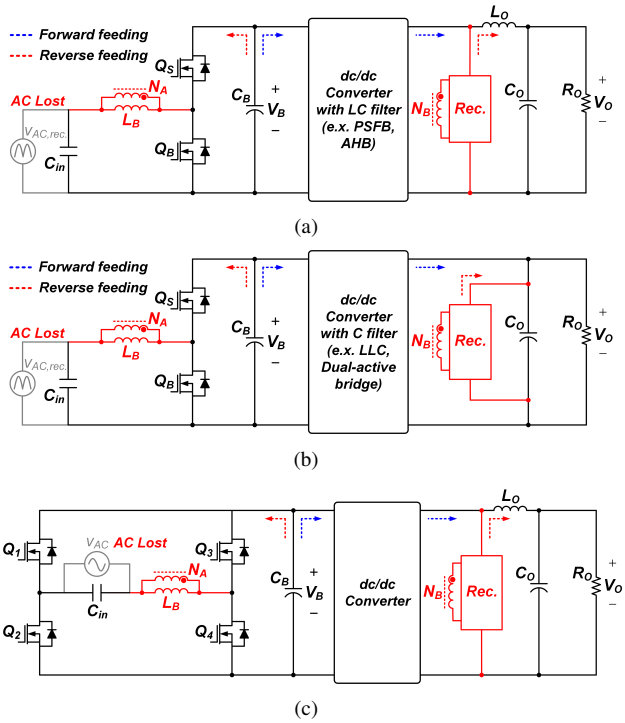
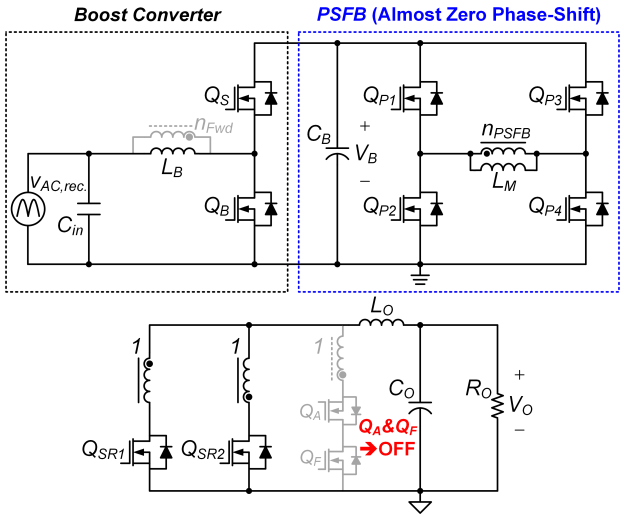


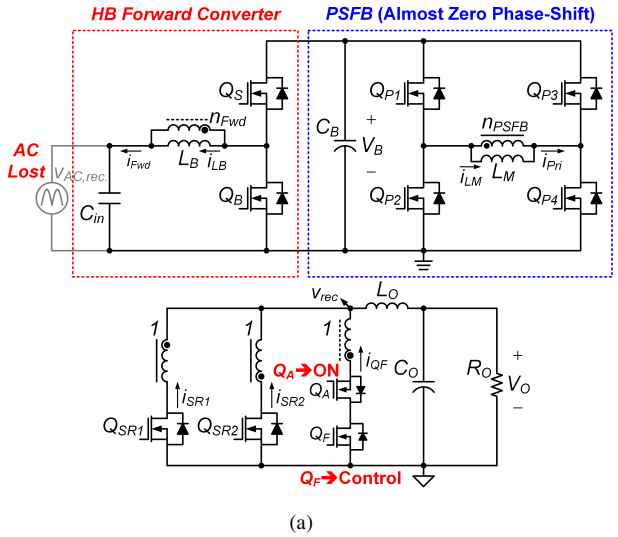
Fig. 3. Embodiments of the reverse-feeding HUT strategy. (a) Converter with a LC filter. (b) Converter with C filter. (c) Bridgeless boost converter. Blue and purple arrows indicate forward feeding and reverse feeding, respectively.

HUT to reduce the design challenge of the dc-dc converter. The dc-dc converter only needs to operate within a narrow input voltage range, leading to higher peak energy efficiency in normal operation. The half-bridge converter can extend the HUT, which can be converted to reduced energy-buffer capacitor size leading to higher system power density.

B. Embodiments of the Reverse-Feeding HUT Strategy

The proposed reverse-feeding HUT strategy can be implemented with a variety of topologies, as illustrated in Fig. 3. For converters with a LC filter structure (such as a PSFB





(a)

Fig. 4. Operation principles of the PFC in normal mode with AC-line ON.

converter or asymmetric half-bridge (AHB) converter), the additional rectifier can be connected to L filter and share the LC filter. Various types of rectifiers (such as a single ended, double ended, voltage multiplier, zeta, buck, boost) can be applied to the reverse-feeding strategy. For converters with a C filter (such as a LLC resonant converter or dual-active bridge converter), the additional rectifier can be connected to the output directly [16]. As illustrated in Fig. 3(c), the reverse-feeding strategy enables the bridgeless boost converter to be used as a full bridge converter during the HUT.

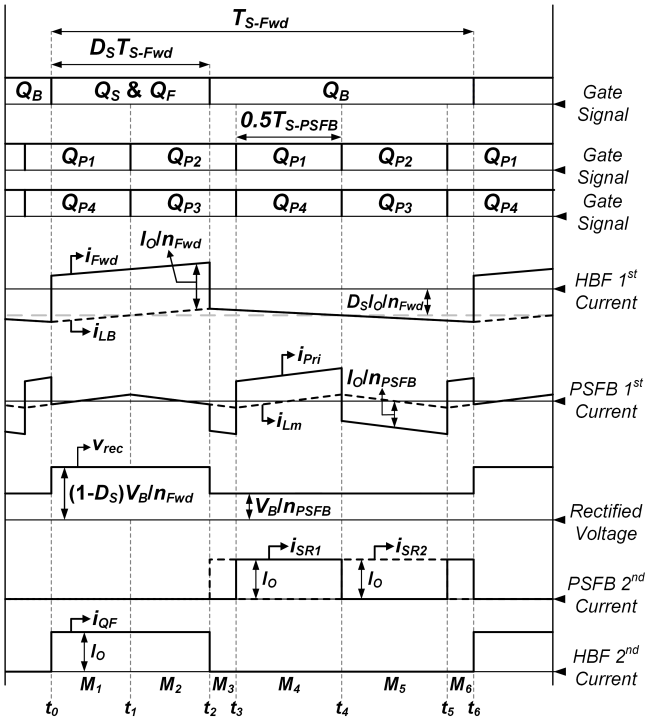
III. "Reverse-Feeding" Design Example

In this paper, the reverse-feeding HUT strategy is applied to a 100V-240V_{rms} ac input and 800W, 12V/66.7A dc output two-stage PFC design with a boost converter and a phase-shift-full-bridge (PSFB) converter. By adding an extra winding and a single-ended rectifier, the boost converter operate as a half-bridge (HB) forward converter during the HUT.

A. Operation Principles

1) Normal Operation: In normal operation, the PFC with reverse-feeding operates as a regular two-stage PFC with the additional rectifier side switches (Q_F and Q_A) kept OFF , as illustrated in Fig. 4. The boost PFC converter regulates the intermediate bus voltage (V_B), i.e., the input voltage of the dc-dc converter (using a PSFB converter as an example). The PSFB converter regulates the output voltage (V_O). A PSFB converter operating with almost zero phase-shift, i.e., 50% effective duty ratio (D_{eff}), can achieve higher efficiency than a PSFB converter designed for wide input voltage range. The operation principles of the PFC in the normal operation is exactly the same as in a traditional two-stage PFC converter except for the voltage stress of Q_F and Q_A:

$$V_{QF} = \frac{V_B}{n_{Fwd}} + \frac{V_B}{n_{PSFB}}, \tag{1}$$



(b)

Fig. 5. Operation principles of the PFC during HUT. (a) Operational schematic diagram. (b) Operational waveforms.

$$V_{QA} = \frac{V_B}{n_{Fwd}} + \frac{\sqrt{2}v_{AC-max}}{n_{PSFB}}, \tag{2}$$

where n_{Fwd} is the transformer turns-ratio of the boost inductor, n_{PSFB} is the transformer turns-ratio of the PSFB transformer, and v_{AC-max} is the maximum ac line voltage.

2) HUT Operation: Several assumptions are made to simplify the analysis: 1) the input capacitor (C_{in}) is large enough to be considered as a constant voltage source, i.e., $D_S V_B$; 2) the dead times between Q_S and Q_B, Q_{P1} and Q_{P2}, and Q_{P3} and Q_{P4} are small enough to be ignored; 3) the output

inductor (L_O) is large enough to be considered as a constant current source, i.e., (I_O); 4) all parasitic components except for those specified in Fig. 5(a) are ignored; 5) n_{Fwd} is lower than n_{PSFB}; and 6) the synchronous rectifier switches (Q_{SR1}, Q_{SR2}, and Q_F) function as ideal diodes. Fig. 5 shows the operational principles of the proposed topology during the HUT. Q_A is kept ON and one switching frequency is divided into six modes and each mode is explained as follows:

Mode 1 (M_1) **[t_0-t_1]:** At time t_0, Q_S and Q_F are turned on. Since n_{Fwd} is lower than n_{PSFB}, the power is transferred to the output through the boost converter and the coupled inductor (function as a half-bridge forward converter). The current flowing through the primary side of the PSFB converter is small magnetizing current (i_{LM}). Therefore, i_{Fwd}, i_{LB}, and v_{Rec} can be expressed as follows:

$$i_{Fwd}(t) = i_{LB}(t) + \frac{I_O}{n_{Fwd}}(t - t_0), \tag{3}$$

$$i_{LB}(t) = i_{LB}(t_0) + \frac{(1 - D_S)V_B}{L_B}(t - t_0), \tag{4}$$

$$v_{Rec}(t) = \frac{(1 - D_S)V_B}{n_{Fwd}}, \tag{5}$$

where D_S is the duty ratio of the switches Q_S and Q_F.

Mode 2 (M_2) **[t_1-t_2]:** At time t_1, Q_{P1} and Q_{P4} are turned off, and Q_{P2} and Q_{P3} are turned on. The magnetizing current (i_{Lm}) of the PSFB converter is reset and the power is still transferred by the HB forward converter.

Mode 3 (M_3) **[t_2-t_3]:** At time t_2, Q_S and Q_F are turned off. The HB forward converter operates in free-wheeling and the PSFB converter delivers power to the output through Q_{P2}, Q_{P3}, and Q_{SR2}. i_{Fwd}, i_{LB}, i_{Pri}, i_{Lm}, and v_{Rec} are:

$$i_{Fwd}(t) = i_{LB}(t), \tag{6}$$

$$i_{LB}(t) = i_{LB}(t_2) - \frac{D_S V_B}{L_B}(t - t_2), \tag{7}$$

$$i_{Pri}(t) = i_{LM}(t_2) - \frac{I_O}{n_{PSFB}}(t - t_2), \tag{8}$$

$$i_{LM}(t) = i_{LM}(t_2) - \frac{V_B}{L_M}(t - t_2), \tag{9}$$

$$v_{Rec}(t) = \frac{V_B}{n_{PSFB}}, \tag{10}$$

Mode 4 (M_4) **[t_3-t_4]:** At time t_3, Q_{P2} and Q_{P3} are turned off, and Q_{P1} and Q_{P4} are turned on. Since the HB forward converter is still in the free-wheeling state, the PSFB converter delivers energy to the output through Q_{P1}, Q_{P4}, and Q_{SR1}. i_{Pri}, i_{Lm}, and v_{Rec} are:

$$i_{Pri}(t) = i_{LM}(t_3) + \frac{I_O}{n_{PSFB}}(t - t_3), \tag{11}$$

$$i_{LM}(t) = i_{LM}(t_3) + \frac{V_B}{L_M}(t - t_3), \tag{12}$$

$$v_{Rec}(t) = \frac{V_B}{n_{PSFB}}, \tag{13}$$

Mode 5 (M_5) **[t_4-t_5]:** At time t_4, Q_{P1} and Q_{P4} are turned off, and Q_{P2} and Q_{P3} are turned on. In this operation, the HB forward converter and the PSFB converter operate as described in Mode 3 ($M3$).

Mode 6 (M_6) **[t_5-t_6]:** At time t_5, Q_{P2} and Q_{P3} are turned off and Q_{P1} and Q_{P4} are turned on. In this operation, the HB forward converter and the PSFB converter operate like in Mode 4 ($M4$). At time t_6, when Q_B is turned off, the power is starting to be transferred by the HB forward converter.

This operation mechanism is just one example implementation of the "reverse-feeding" concept. The operation frequency of the PSFB converter and the HB forward converter can be freely adjusted and jointly optimized. More sophisticated power delivery strategies can be added. Similar concepts can be applied to other dc-dc topologies (e.g., LLC, dual-active bridge, and series resonant).

B. Advantages of the Reverse-Feeding Strategies

1) Voltage Conversion Ratio: In the normal operation, the PFC with reverse-feeding strategy has the same voltage conversion ratio and function with the PFC with conventional designs. During the HUT, the output voltage is only regulated by the PSFB converter in conventional designs. The voltage conversion ratio (M_{Conv}) is:

$$\frac{V_O \times n_{PSFB}}{V_B} = M_{Conv} = 2D_{eff},\ D_{eff} \leq 0.5. \tag{14}$$

where D_{eff} is the effective duty-ratio of the PSFB converter.

Meanwhile, in the PFC with the proposed strategy, both the HB forward converter and the PSFB converter regulate the output voltage during the HUT. Thus, the voltage conversion ratio (M_{Pro}) is the weighted average of the voltage gains of the two converters. From (5), (10), and (13), M_{Pro} can be expressed as follows:

$$M_{Pro} = \begin{bmatrix} 2D_{eff},\ D_{eff} \leq 0.5 \\ (1 - D_S)(1 + \alpha D_S),\ D_{eff} = 0.5 \end{bmatrix}, \tag{15}$$

where α is n_{PSFB}/n_{Fwd}.

Fig. 6 shows the voltage conversion ratio of the conventional PSFB converter and the reverse-feeding strategy during the HUT. When D_{eff} is smaller than 0.5, since the PFC with reverse-feeding operates like a conventional PSFB converter, its voltage conversion ratio is the same as the conventional one. When D_{eff} is 0.5, the conventional PSFB converter reaches its maximum voltage conversion ratio. On the other hand, in the reverse-feeding strategy, the HB forward converter can offer additional voltage gain, and larger α leads to much higher voltage conversion ratio than the conventional one. For this reason, the reverse-feeding strategy enables the PSFB to be designed with higher transformer turns-ratio than the conventional PSFB converter. The higher effective voltage conversion ratio enabled by the reverse-feeding strategy also enables larger voltage drop in the energy-buffer capacitor, thus extending the HUT and improving the power density of the converter (by using smaller energy-buffer capacitors).

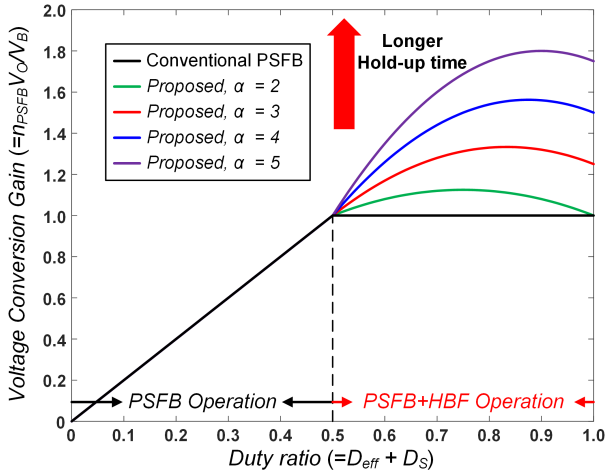


Fig. 6. Comparison of voltage conversion ratio between the conventional PSFB converter and the PFC with reverse-feeding. Due to additional voltage gain of the HB forward converter (HBF), the PFC with the proposed strategy can achieve higher voltage conversion ratio than a conventional design, and thus extend the HUT and reduce the buffer capacitor size.

2) Boost PFC converter: The boost PFC converter with the reverse-feeding strategy operates like a conventional boost PFC converter in normal mode. Thus, it has the same characteristics, such as voltage gain, voltage stress, and current stress, as the conventional one. For this reason, the boost PFC converter can be designed following the conventional method [17], [18] except for the rectifier-coupled boost inductor. Table I shows the designed parameters of boost PFC converter in the conventional and proposed strategies. For Q_S, both converters use a GaN FET in TO-220 package. The input filter capacitor (C_{in}) is selected as 1μF to meet the electromagnetic interference (EMI) requirements. The buffer capacitor (C_B) of the boost PFC converter is selected as 810μF to support 30ms HUT. Thus, if the bus voltage is regulated as 400V in the normal operation, the minimum bus voltage (V_{Min}) during HUT is 315V. The winding area of the rectifier-coupled boost inductor should increase as much as a winding area for an additional winding (N_B). To use the same magnetic core, the rectifier-coupled boost inductor applies slightly thinner wire than the conventional one to N_A, which results in slightly larger conduction loss compared to the conventional one.

3) PSFB converter: In the conventional design, since the PSFB converter should solely regulate the output voltage during the HUT, the conventional PSFB converter should be designed with 315V-400V input voltage range. On the other hand, during the HUT, the HB forward converter can provide additional high voltage gain. Therefore, the PSFB converter in the reverse-feeding strategy can be better optimized in normal operation range. The normal operation range just includes the ripple voltage of V_B (ΔV_B) so the minimum input voltage of the PSFB converter is V_B-0.5ΔV_B in normal mode. ΔV_B can be expressed as follows:

$$\Delta V_B = \frac{P_O}{2\pi f_{Line} C_B V_{B-Reg}}, \tag{16}$$

where P_O is the output power, f_{Line} is the ac line frequency, and V_{B-Reg} is the regulated PFC output voltage.

In this paper, considering ΔV_B and some design margin, we assumed that the PSFB converter in the proposed strategy is designed with 380V-400V input voltage range. Similar concept is applicable to other two-stage PFC designs with different design constraints. Table II compares the designed parameters of the PSFB converter in the conventional and proposed strategies. From (14) and (15), by reducing the input voltage range of the PSFB converter, the reverse-feeding strategy enables the PSFB converter to have higher transformer turns-ratio than the conventional one, which results in the following advantages while it functioning as a dc transformer:

- **Reduced primary side conduction loss.** The primary side current (i_{Pri}) reflected from the secondary side has the same forms in (8) and (11). Therefore, the increased transformer turns-ratio (n_{PSFB}) can reduce the primary side current, reducing the conduction losses on the primary side. In principle, a higher turns-ratio transformer operating with higher duty ratio offers higher performance than a lower turns-ratio transformer operating with lower duty ratio.
- **Reduced output inductor core loss.** The delta flux density of the output inductor core (ΔB_{Lo}) is:

$$\Delta B_{Lo} = \frac{V_O(1 - D_{eff})}{A_e N_{Lo} f_S}, \tag{17}$$

  where A_e is the effective cross section area of the core, N_{Lo} is the number of output inductor turns, and f_S is the switching frequency. Assuming that the PSFB converter in a reverse-feeding design and in a conventional design use minimized N_{Lo} and maximized wire thickness to carry high output current, the core loss difference is only determined by D_{eff}. Due to the increased transformer turns-ratio, the PSFB converter with the reverse-feeding strategy operates with much larger effective duty ratio in the normal operation compared to a conventional design. Therefore, the increased transformer turns-ratio can reduce the output inductor core loss (or reduce the inductor size).
- **Reduced snubber loss.** The PSFB converter usually adopts a RCD clamped snubber circuit to clamp the secondary voltage stress. Since higher transformer turns-ratio reduces voltage stress of the secondary switch (=2V_B/n_{PSFB}), the snubber loss in a conventional PSFB converter is reduced.
- **Better device rating.** Since the PSFB converter operates in a narrower operation range, the switch voltage ratings and current ratings can be better optimized.

In summary, the "reverse-feeding" strategy uses the boost PFC converter to process energy during the HUT to create additional design flexibility for the dc-dc converter, and allows the ac-dc system to be better optimized for higher efficiency and power density. In a specific "boost+PSFB" two stage design, the "reverse-feeding" strategy reduces the primary conduction loss, output inductor core loss, and snubber loss in the normal operation when high efficiency is required.

C. Design Considerations of HB Forward Converter

The HB forward converter reuses the components of the boost PFC converter. Thus, the HB forward converter should be designed using the optimally designed parameters of the boost PFC converter shown in Table I to achieve high performance in normal operation. As a result, design parameters of the HB forward converter are only the additional winding (N_B) and the switching frequency (f_{S-Fwd}) during HUT. Those parameters should be designed under following criteria to achieve high normal operation efficiency and extended HUT: (1) Minimized impact on the boost PFC converter; (2) Maximizing the HUT.

1) Voltage Stress of the Rectifier Switches: As illustrated in Fig. 6, the HB forward converter can offer higher additional voltage gain as n_{Fwd} decreases, which can extend the HUT. However, since n_{Fwd} is related to the voltage stress of the secondary semiconductor devices, the additional voltage stress on the rectifier side should be considered. The switch stress on the rectifier side during the HUT is:

$$V_{QSR1} = V_{QSR2} = \frac{(1-D_S)V_B}{n_{Fwd}} + \frac{V_B}{n_{PSFB}}, \quad (18)$$

$$V_{QF} = \frac{D_S V_B}{n_{Fwd}} + \frac{V_B}{n_{PSFB}}, \quad (19)$$

Q_A is kept ON during HUT and does not block voltage. The voltage stress of rectifier switches are determined by the maximum voltage stress during normal and HUT operations.

2) Current Stress on the Primary Side: In order to reuse the switches designed for the boost PFC converter, the HB forward converter should have lower maximum current stress than the boost PFC converter. The peak current stress of Q_S and Q_B of the HB forward converter are:

$$i_{QB-peak} = \frac{D_S I_O}{n_{Fwd}} + \frac{D_S(1-D_S)V_B}{2L_B f_{S-Fwd}}, \quad (20)$$

$$i_{QS-peak} = \frac{i_{Lo} - D_S I_O}{n_{Fwd}} + \frac{D_S(1-D_S)V_B}{2L_B f_{S-Fwd}}, \quad (21)$$

3) Rectifier-coupled Boost Inductor: In normal operation, the rectifier-coupled boost inductor operates as a traditional boost inductor. Thus, it should be designed considering large offset current under the minimum ac input condition, i.e., $\sqrt{2}P_O/v_{AC-min}$. During the HUT, the rectifier-coupled boost inductor operates as a transformer for the HB forward converter and the offset current of the HB forward converter is $(D_S I_O)/n_{For}$, which is much smaller than $\sqrt{2}P_O/v_{AC-min}$. Thus, the rectifier-coupled boost inductor does not require additional core section area compared to conventional boost inductor. However, due to the additional winding, the window area should slightly increase, or thinner windings (N_A) should be used. In general, since the boost converter only operate for a very short amount of time (a few line cycles), the current density of N_B can be much higher than what is usually required for a forward converter. Therefore, the additional windings can be implemented with very thin wires and the additional winding area is negligible.

4) CCM (Continuous Current Mode) Operation: The HB foward converter can be designed to operate in CCM (continuous current mode) to simplify the control strategy and avoid abrupt voltage gain change between CCM operation and DCM (discontinuous current mode) operation during the HUT. To maintain CCM operation during the HUT, the ripple current of the output inductor (Δi_{Lo}) should meet the following criteria:

$$\Delta i_{Lo} = \frac{n_{PSFB} V_O D_S}{2(1+\alpha D_S) L_O f_{S-Fwd}} \leq I_O, \quad (22)$$

In summary, BSC03N08NS (80V) is selected for Q_F and Q_A, f_{S-Fwd} is 40kHz, and n_{Fwd} and N_B are designed as shown in Table I.

TABLE I
DESIGNED PARAMETERS OF THE BOOST PFC CONVERTER

List	Conventional	Reverse-Feeding
Q_B	IPZ60R099P6	
Q_S	TPH3212PS	
C_{in}	1μF	
C_B	810μF	
V_B	315V-400V (V_{B-reg}=400V)	
L_B	AMP27P40×2 511μH N_A=72T (1.2Φ) -	AMP27P40×2 511μH N_A=72T (1.1Φ) N_B=8T (0.05Φ×320)

TABLE II
DESIGNED PARAMETERS OF THE PSFB CONVERTER

List	Conventional	Reverse-Feeding
Q_{P1} & Q_{P2}	TK25V60X	
Q_{P3} & Q_{P4}	TK12V60W	
Q_{SR1} & Q_{SR2}	BSC016N06NS (2EA)	
L_O	APM27P90, 2.0μH, 4turns (1.5Φ×6)	
Transformer	EE3531 L_M=1.8mH n_{PSFB}=23 (N_P:N_S:N_S=23:1:1)	EE3531 L_M=1.8mH n_{PSFB}=28 (N_P:N_S:N_S=28:1:1)
R_{snb}	2.1kΩ	7.5kΩ

IV. EXPERIMENTAL RESULTS

To verify the effectiveness of the "reverse-feeding" strategy, an 800W server power supply with 100-240V_{rms} ac input and 12V/66.7A output was built and tested. We also implemented a conventional two-stage PFC design as a comparison with similar operation range and optimization procedure. Table I and Table II summarize the details of the two prototypes. The switching frequencies of the boost PFC converter and PSFB converter in both strategies are 55kHz and 75kHz, respectively.

Fig. 7. Comparison between a conventional boost inductor and a rectifier-coupled boost inductor. The winding areas of the two designs are almost the same with identical magnetic cores.

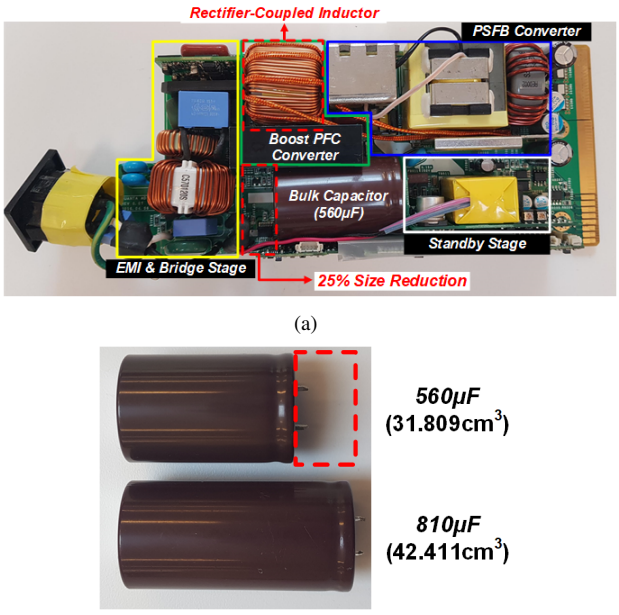


Fig. 8. Picture of the 800W, 12V/66.7A prototype with rectifier-coupled boost inductor and additional secondary switches. (a) Ac-dc server power supply. (b) Comparison of capacitor size between 560μF and 810μF (25% size reduction).

Fig. 7 shows the comparison between conventional boost inductor and rectifier-coupled boost inductor. Fig. 8 shows pictures of the prototype. When the proposed topology was used with the same capacitance of the conventional prototype, it extended the HUT. When the proposed topology was designed with the same HUT of the conventional one, it reduced the size of a energy-buffer capacitor (25% reduction) and can achieve higher power density.

Fig. 9 shows measured waveforms of the two prototypes in normal operation. As discussed in Part III-B, the reverse-feeding strategy enabled the PSFB converter to have much smaller circulating current and primary current than the conventional one because of high transformer turns-ratio in narrow operation range. Moreover, it has shorter free-wheeling period. The voltage stress on the secondary side switches are reduced.

Fig. 10 shows the measured efficiency and estimated loss

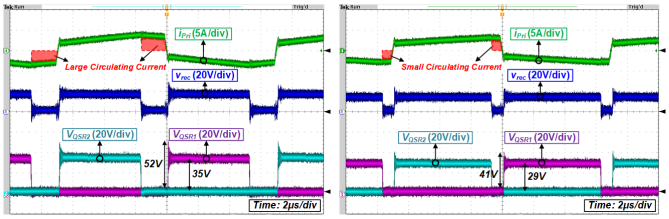
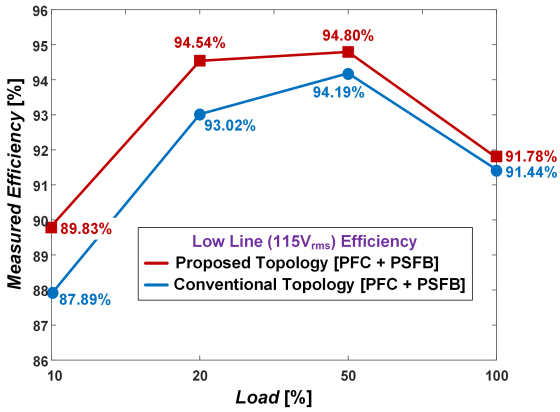
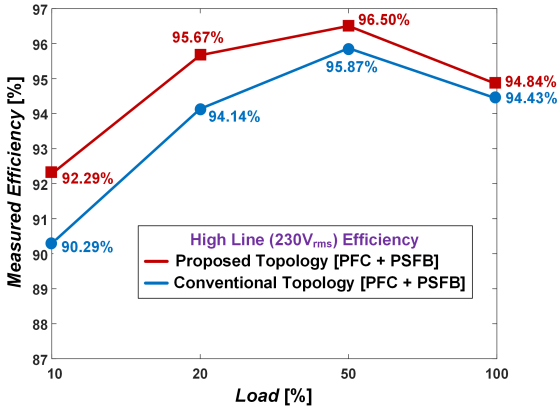


Fig. 9. Measured waveforms at V_B=400V and full load condition. (a) Conventional PSFB converter. (b) PSFB converter with reverse-feeding.





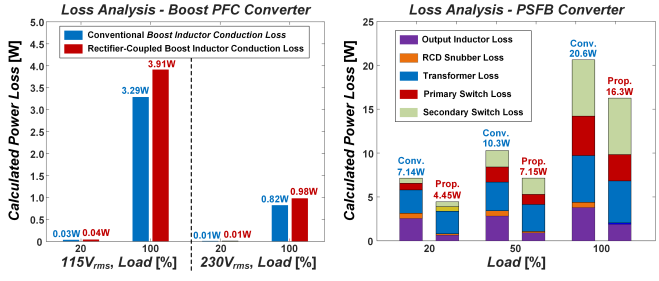


Fig. 10. Measured system (boost PFC + PSFB converter) efficiency. (a) 115V_{rms} (Low line). (b) 230V_{rms} (High line). (c) Loss analysis.

breakdown of two prototypes in 115V_{rms} and 230V_{rms}. Due

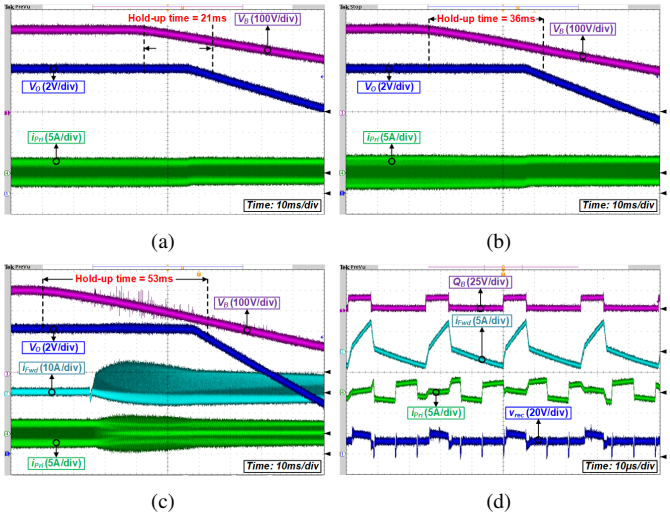


Fig. 11. Measured waveforms during HUT (full load condition). (a) Conventional PSFB converter with n_{PSFB}=28. (b) Conventional PSFB converter with n_{PSFB}=23. (c) Proposed topology. (d) Proposed topology at V_B=250V.

to the additional winding (N_B), the conduction loss in the rectifier-boost inductor is slightly increased in normal operation. This is because the winding of N_A can be designed with slightly thinner wires. However, benefiting from the additional design flexibility and system optimization, the prototype with the reverse-feeding strategy achieves higher efficiency than the conventional one over the entire load condition. As illustrated in Fig. 10(c), it achieves 96.5% peak efficiency by improving the PSFB converter efficiency through the reduced primary conduction loss, output inductor core loss, and snubber loss.

Fig. 11 shows the measured waveforms during the HUT. Conventional PSFB converter has trade-off relationship between high efficiency and long HUT as shown in Fig. 11(a) and Fig. 11(b). On the other hand, since the HB forward converter provides additional voltage gain, the reverse-feeding strategy obtained much longer HUT compared to the conventional PSFB converter, while achieving high efficiency in the normal mode. From Figs. 11(c) and (d), the proposed strategy well regulates V_O at V_B=250V using both the PSFB converter and HB forward converter. When the prototype with the reverse-feeding strategy is designed to achieve the same HUT as a conventional PSFB converter with n_{PSFB}=23, the buffer capacitor can be reduced by 25% as shown in Fig. 8.

V. Conclusions

This paper presents a "reverse-feeding" HUT strategy to achieve high efficiency and extend the HUT in grid-interface PFC. By coupling the boost inductor to the rectifier stage, the boost stage of the PFC can be reused as a HB converter during the HUT. This enables the dc/dc stage (e.g. PSFB converter) to be optimized for narrower operation range and achieve higher efficiency in normal operation. During the HUT, both the boost stage and the dc/dc stage are used to transfer power from the energy-buffer capacitor to the output. The effectiveness of the "reverse-feeding" strategy was verified by two PFC prototypes with the same boost converter and the PSFB converter. The PFC with reverse-feeding can achieve higher peak efficiency (96.5%) with extended HUT (about 1.5 times), or can reduce the buffer capacitor size by 25%. The "reverse-feeding" strategy can be similarly implemented in a variety of other two-stage grid-interface PFC topologies.

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