A "Reverse-Feeding" Hold-up Time Strategy for Two-Stage Grid-Interface PFC with a Rectifier-Coupled Boost Inductor

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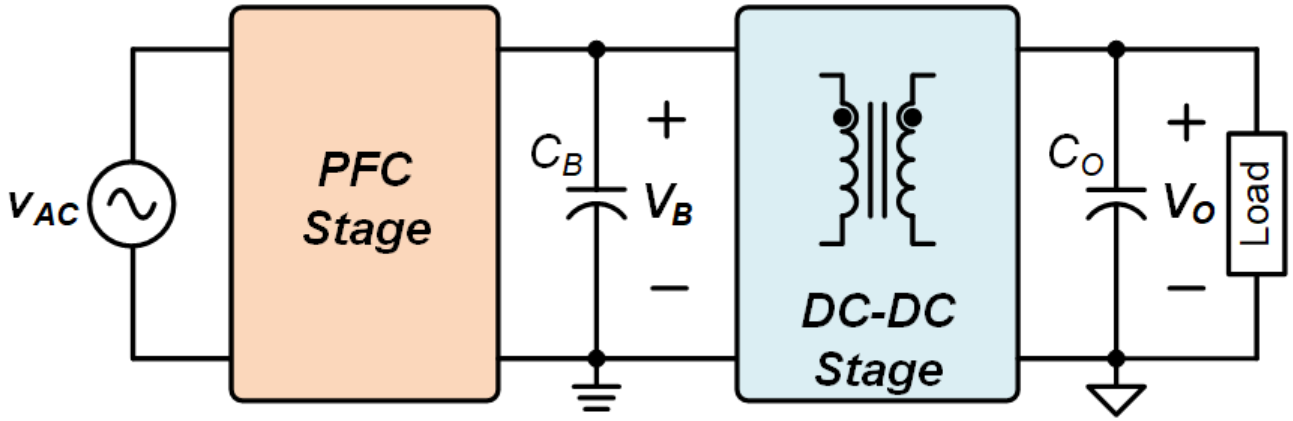
Note: This work was started at KAIST and completed at Princeton University

Two-stage grid-interface PFC architecture

Needed in a wide range of applications

- Data-center / Transportation / Industrial applications



[*Two-stage grid-interface PFC*]

- PFC stage

  ➔ High power quality, V_B regulation

- DC/DC stage

  ➔ Isolation, V_O regulation

Design targets

- High efficiency / high power density
- High power quality
- Hold-up time requirement

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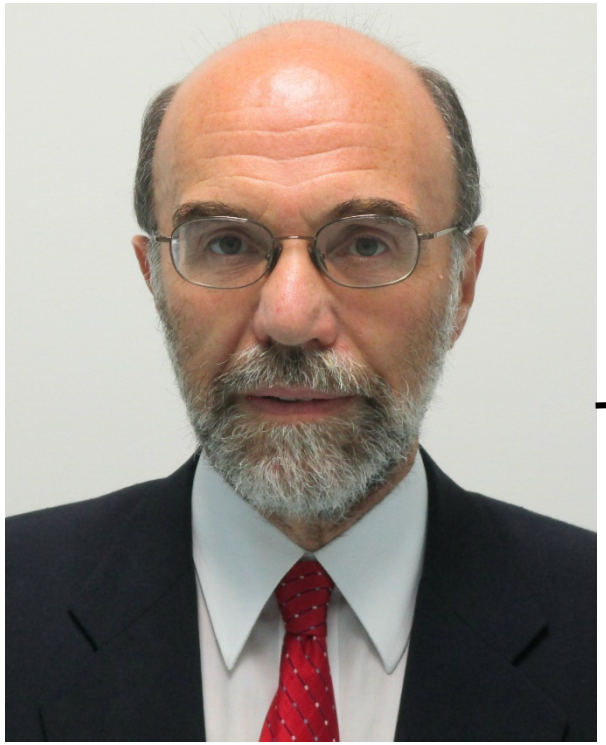
Dr. Jovanovic's contribution to PFC applications

IEEE ENERGY CONVERSION CONGRESS & EXPO

A wide range of contribution to power electronics field



Single-phase PFC

- **Topology solutions**
  1. Soft-switching snubber circuit [1]
  2. Coupled-inductor design [2]
  3. Comprehensive overview of PFC circuits [3],[4]
  - ⋮
- **Control techniques (Analog & Digital)**
  1. DCM/CCM boundary control [5]
  2. DCM interleaving control [6]
  3. PLL-based interleaving control [7]
  - ⋮
- **Hold-up time extension technique [8]**

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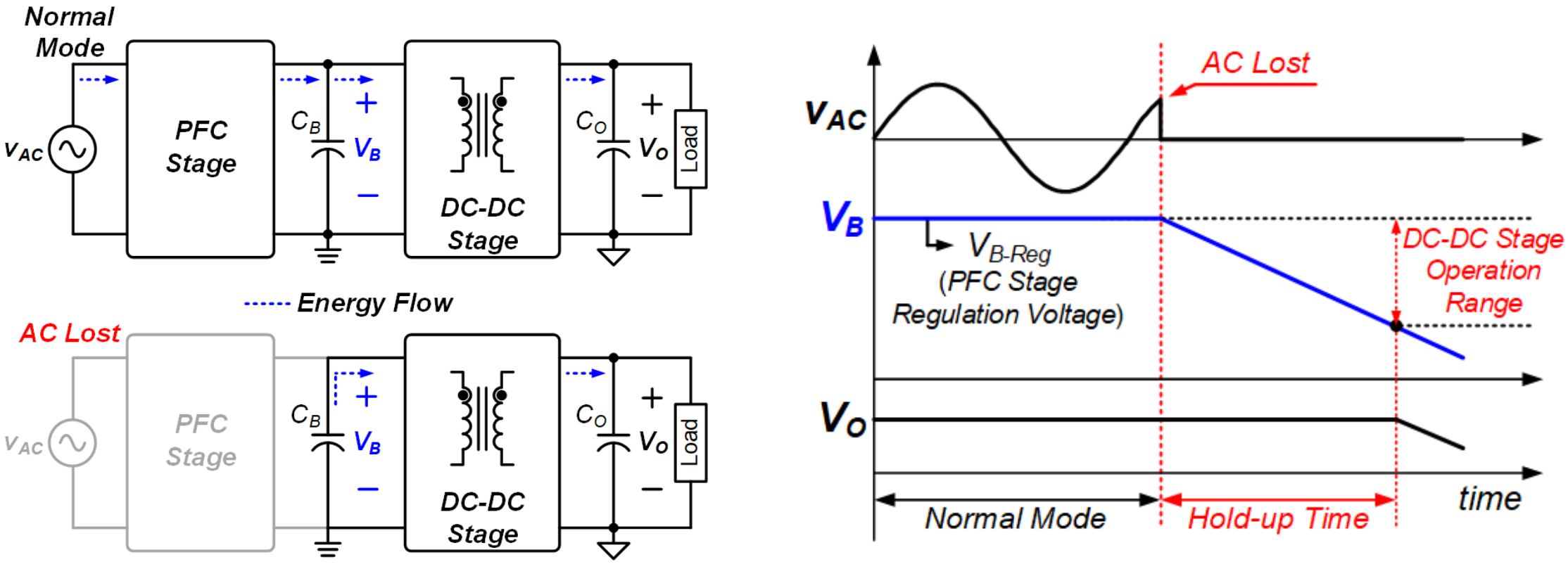
Hold-up time requirement in PFC

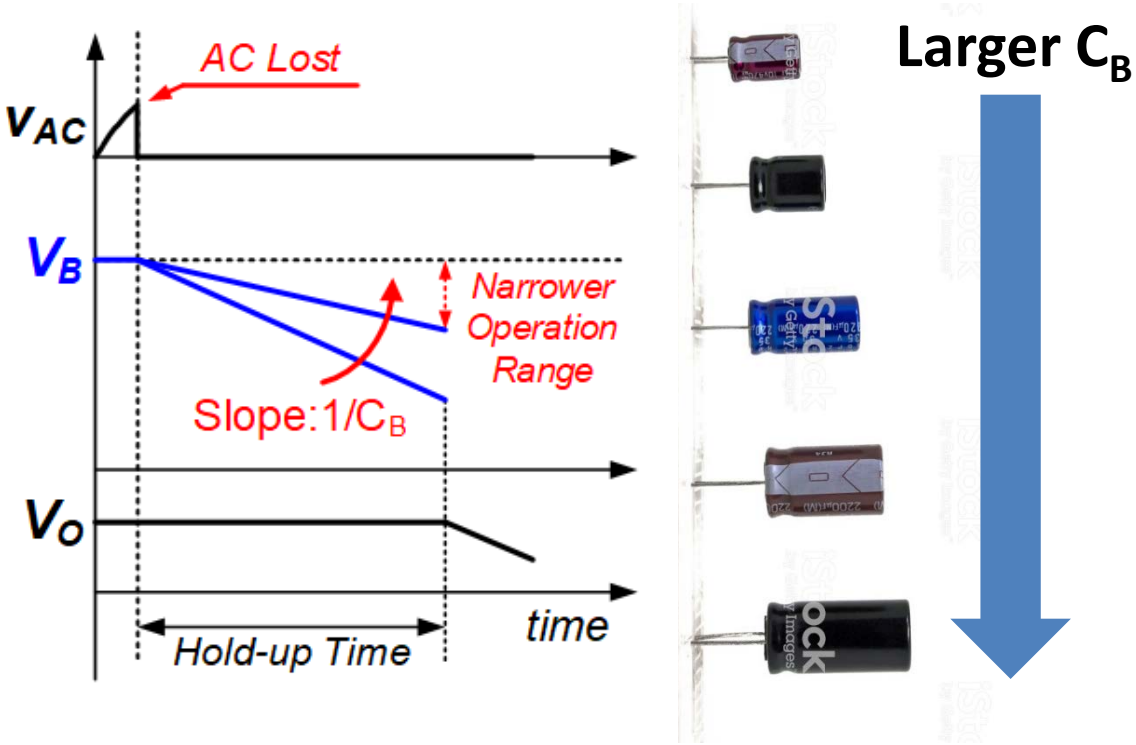


[*Operations and waveforms of PFC during hold-up time*]

- The HUT requirement set the limit for efficiency & energy buffer capacitor size

Methods for extending the hold-up time

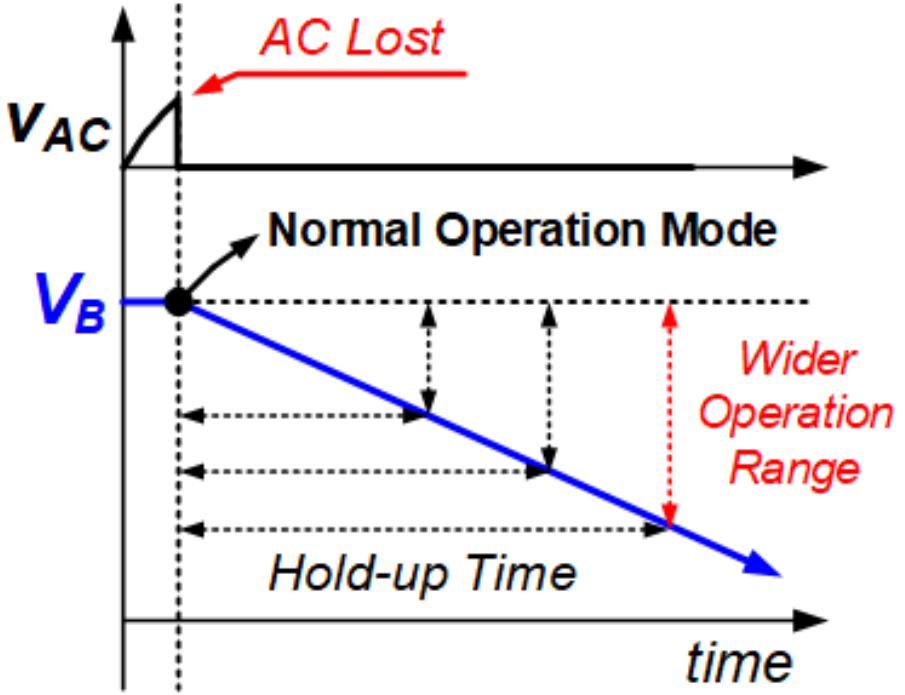
Larger energy buffer capacitor (C_B)



[*Effects of large C_B*]

- Larger C_B ➔ Lower power density

Wider operation range for Dc-Dc

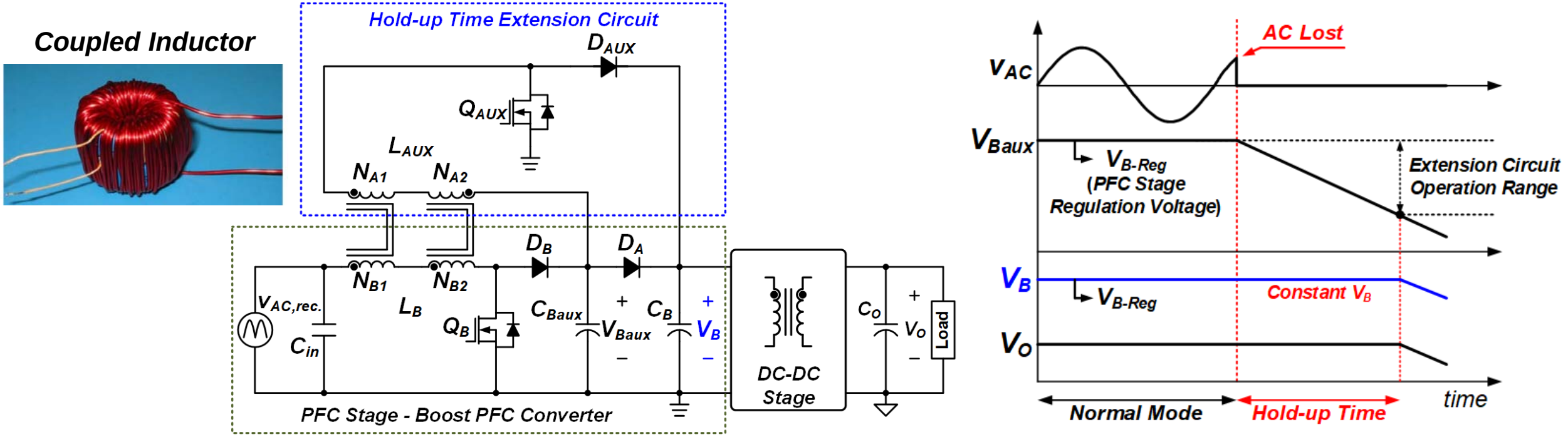


[*Effects of wide V_B*]

- Wider range ➔ Lower peak efficiency

Dr. Jovanovic's hold-up time contribution

Hold-up Time Extension Circuit

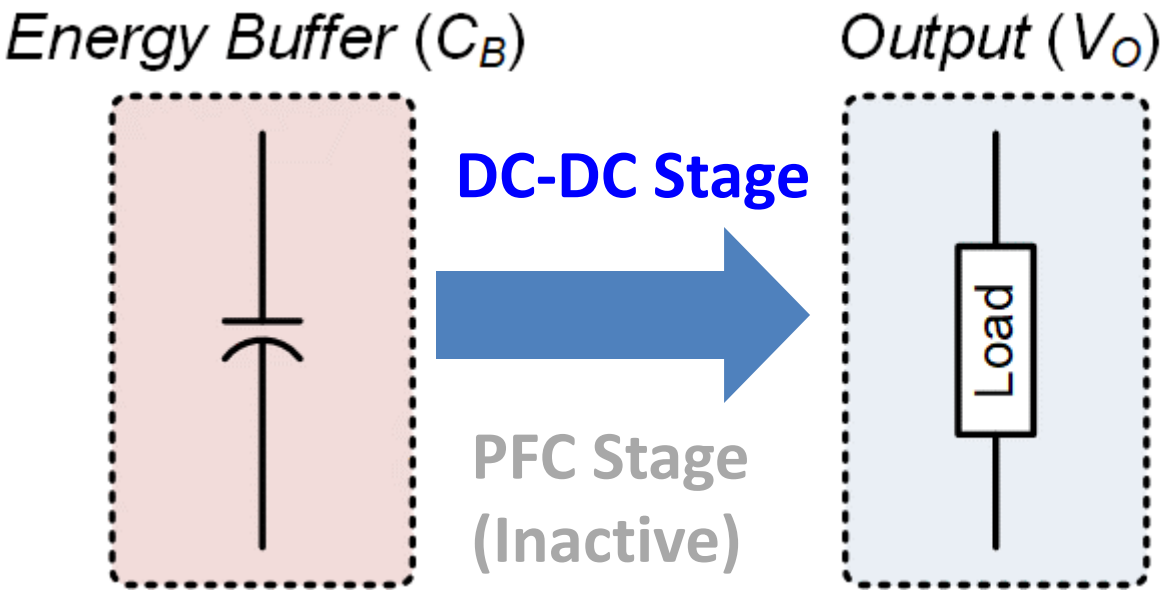


[*Dr. Jovanovic's hold-up time compensation circuit* [8]]

- Use a HUT extension circuit to reduce the dc-dc operation range
- Loss of D_A in normal mode, large size of hold-up time extension circuit

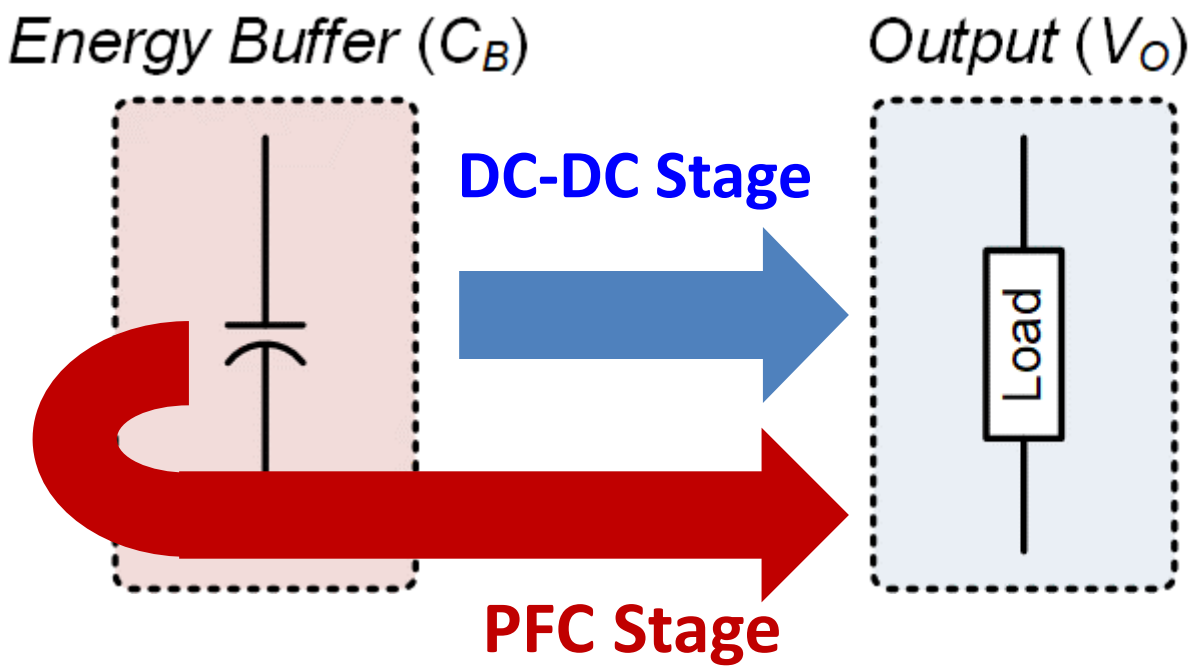
Reverse-feeding strategy for two-stage PFC

Conventional strategy



- Forward feeding
  : C_B → DC-DC Stage → V_O

Reverse-feeding strategy



- Two-way feedings
  - Forward: C_B → DC-DC Stage → V_O
  - **Reverse: C_B → PFC Stage → V_O**

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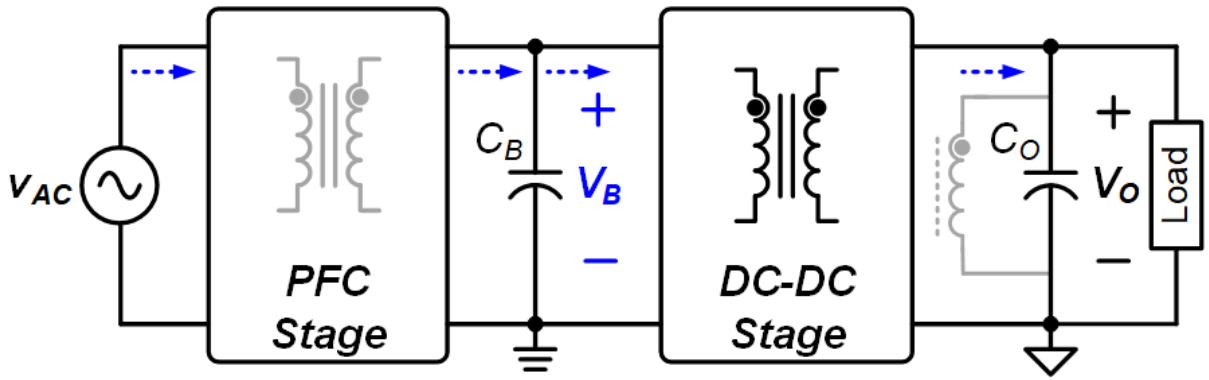
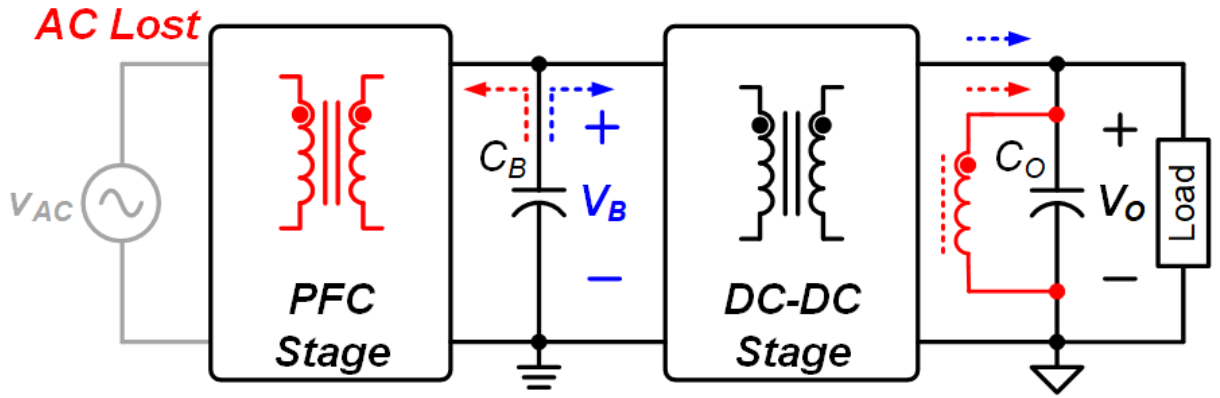
Advantages of reverse-feeding strategy

Normal mode operation



Hold-up time operation

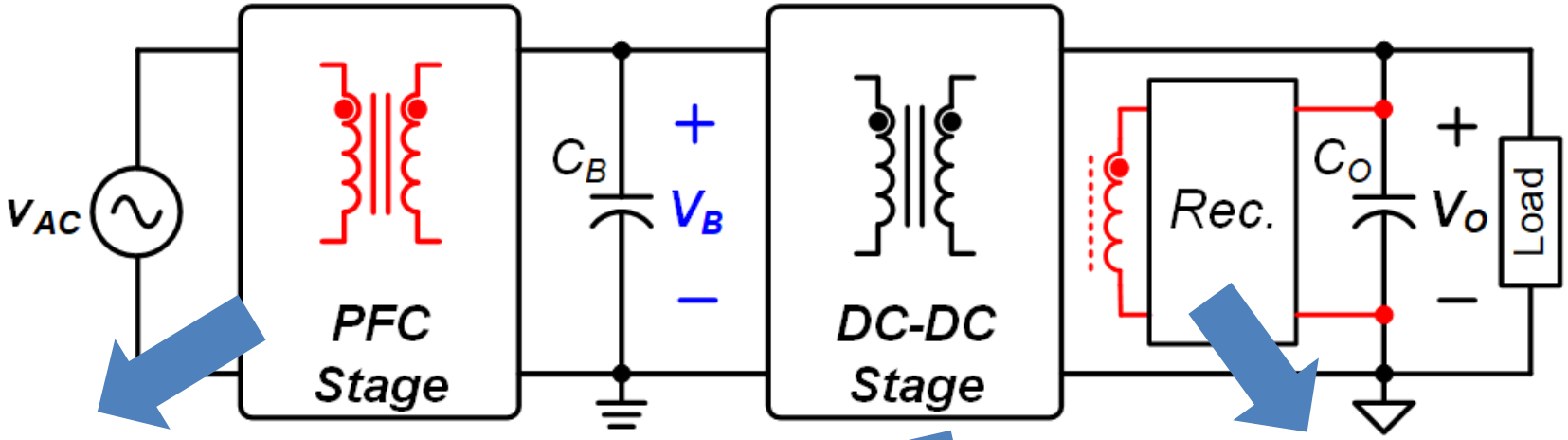


1. Reusing the inactivated PFC stage ➔ **Extended hold-up time**
2. Easier DC/DC stage design like DCX transformer

   ➔ **Improved peak efficiency in normal mode**
3. Wider operation range ➔ **Reduced buffer capacitor size**

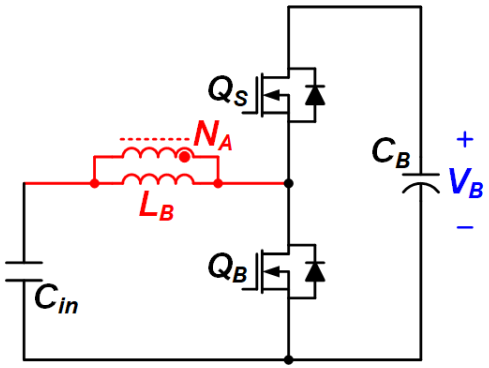
Embodiments of reverse-feeding strategy

Applicable to a variety of PFC & DC/DC topologies



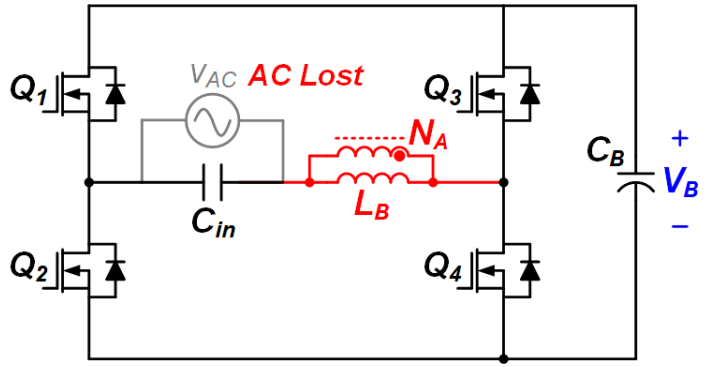
Boost converter

➔ **Half-bridge**



Bridgeless boost converter

➔ **Full-bridge**



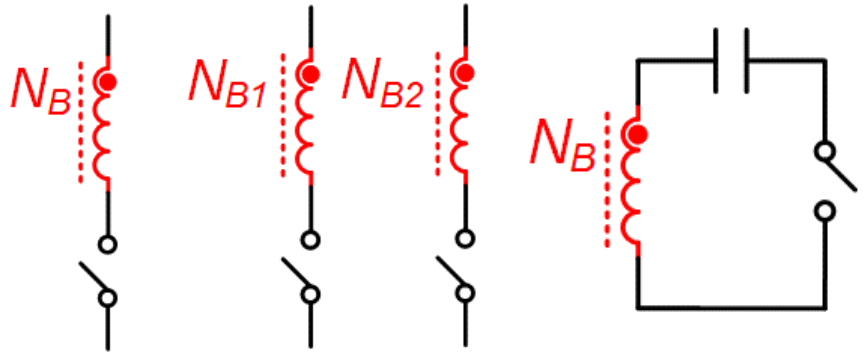
AHB, PSFB

LLC, DAB

…

Various rectifier circuits

➔ **Single/double ended, voltage doubler**



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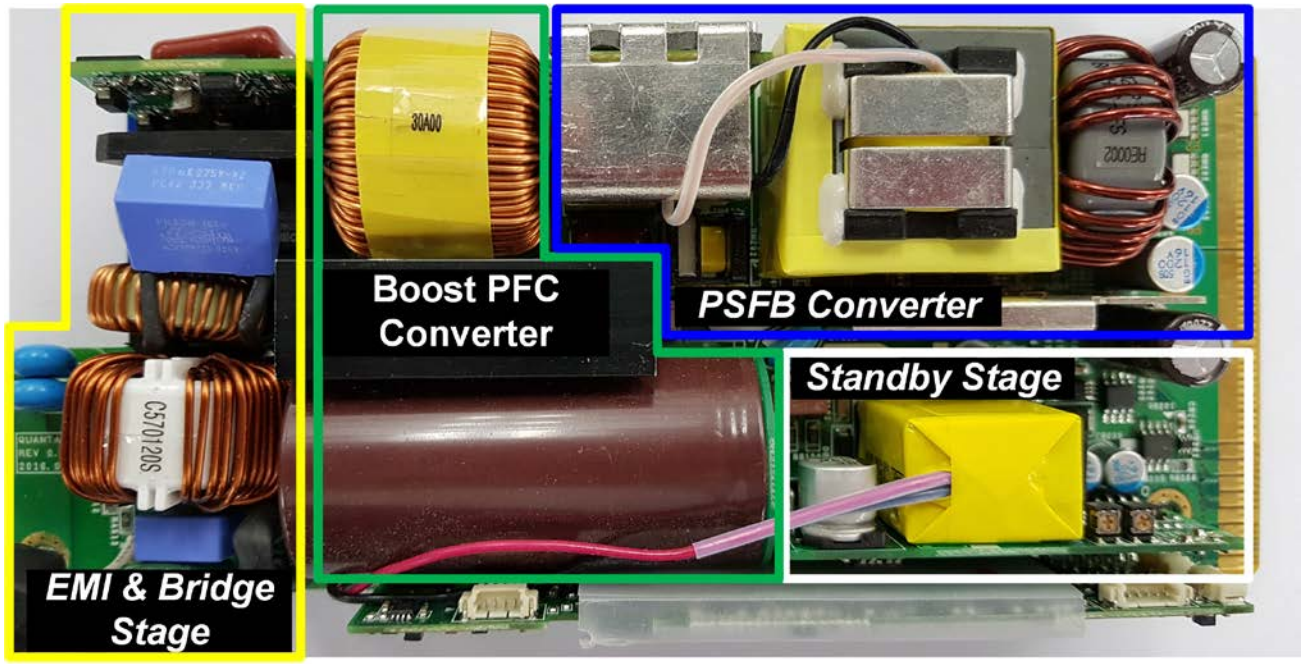
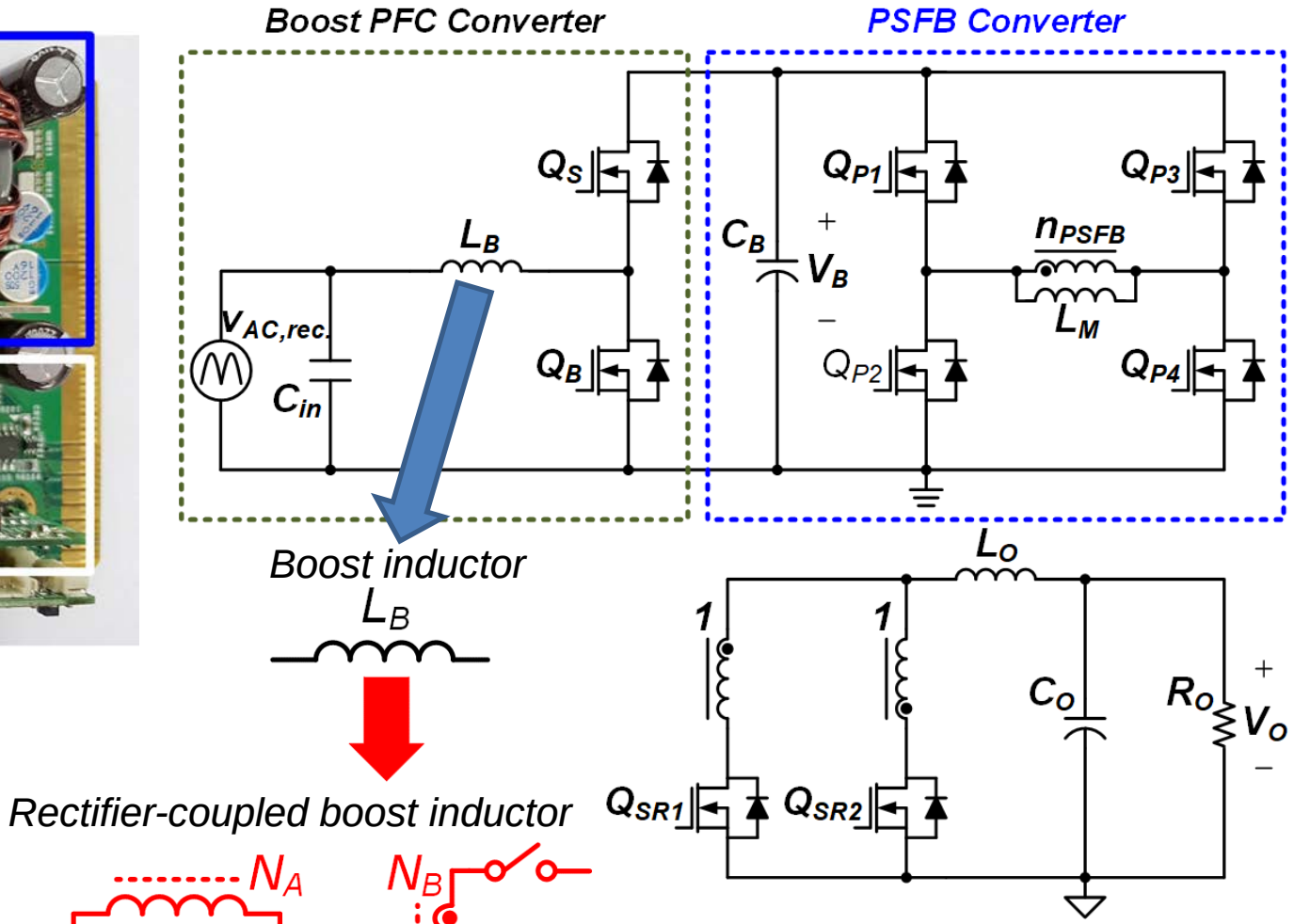
Design example of a reverse-feeding PFC

800W server power supply (100-240V_{RMS}, 12V/66.7A)

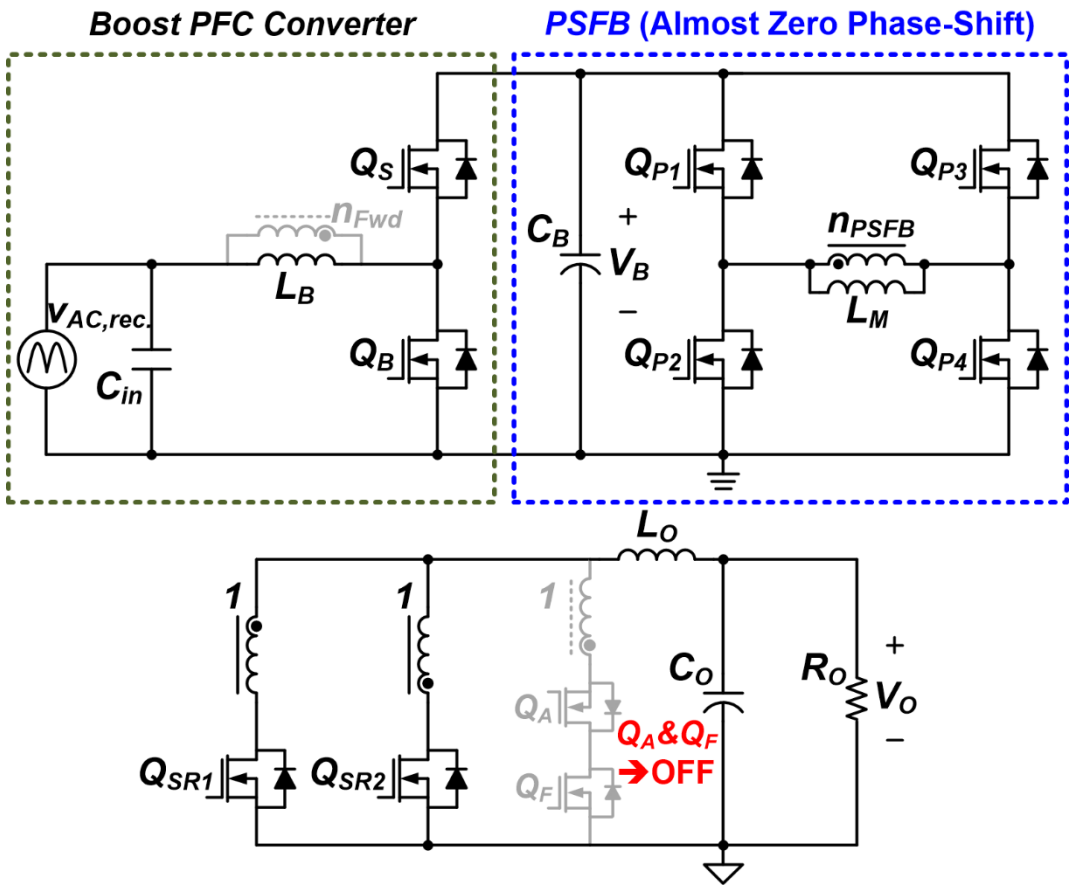


[*800W server power supply product*]



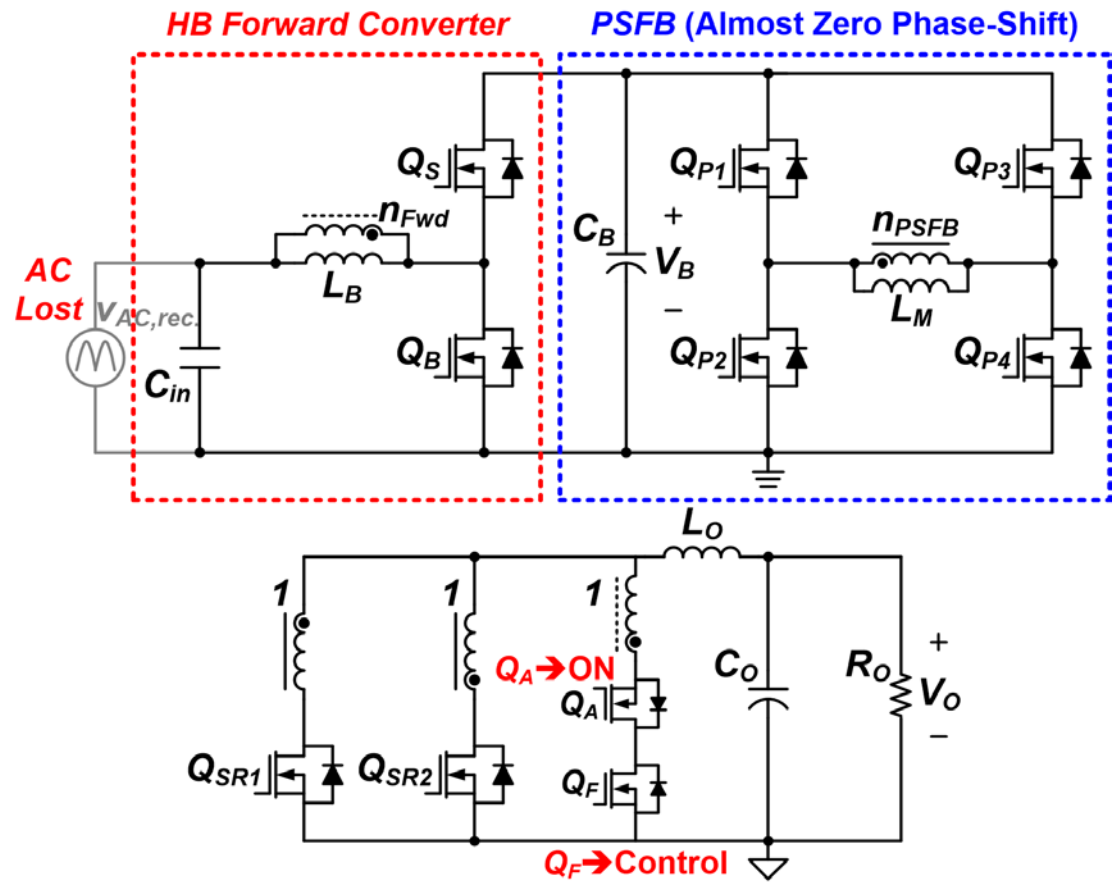
Operational circuits – Two operation modes

Normal operation



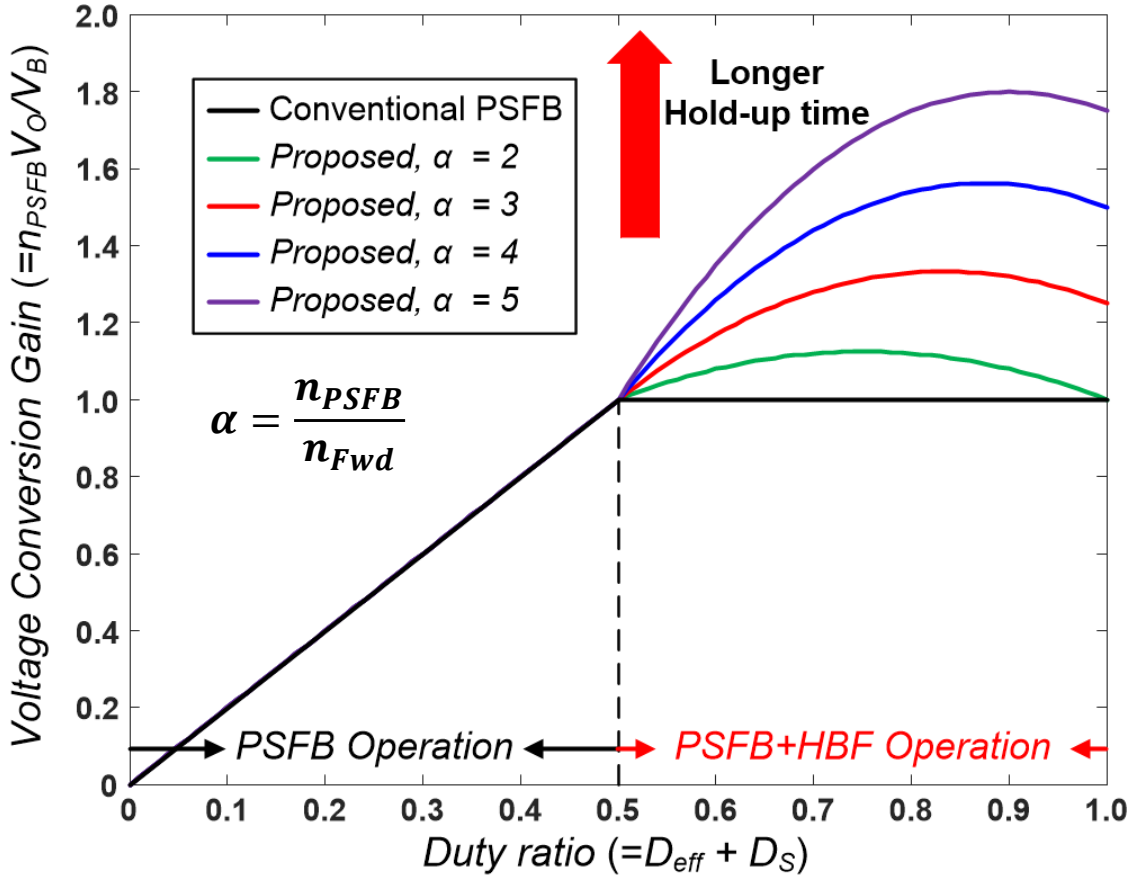
- Normal mode → Q_A & Q_F OFF
- Boost PFC + PSFB → V_O regulation

During HUT



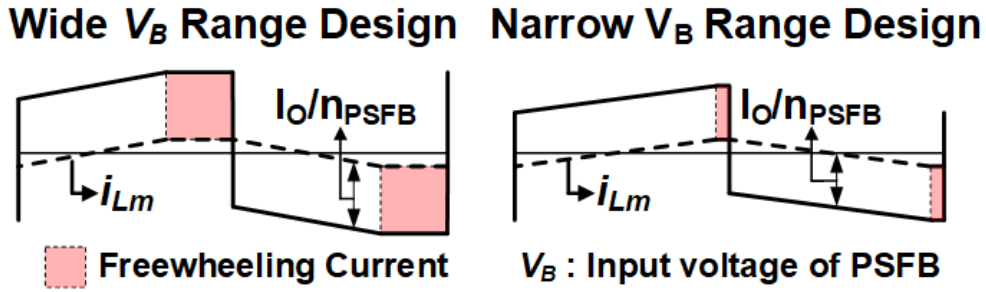
- Hold-up time → Q_A ON, Q_F control
- PSFB + HB forward → V_O regulation

Longer hold-up time & Higher efficiency

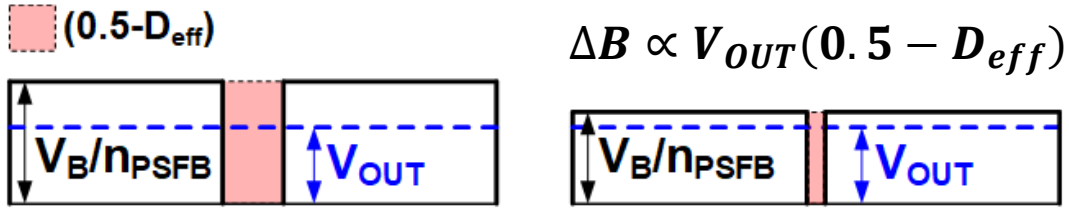


- Additional voltage gain of reverse feeding
  - ➔ Longer hold-up time
  - ➔ Narrower operation range design of PSFB

- Narrow operation range design of PSFB
  - ➔ Lower primary conduction loss



  - ➔ Lower output inductor core loss



  - ➔ Lower snubber loss

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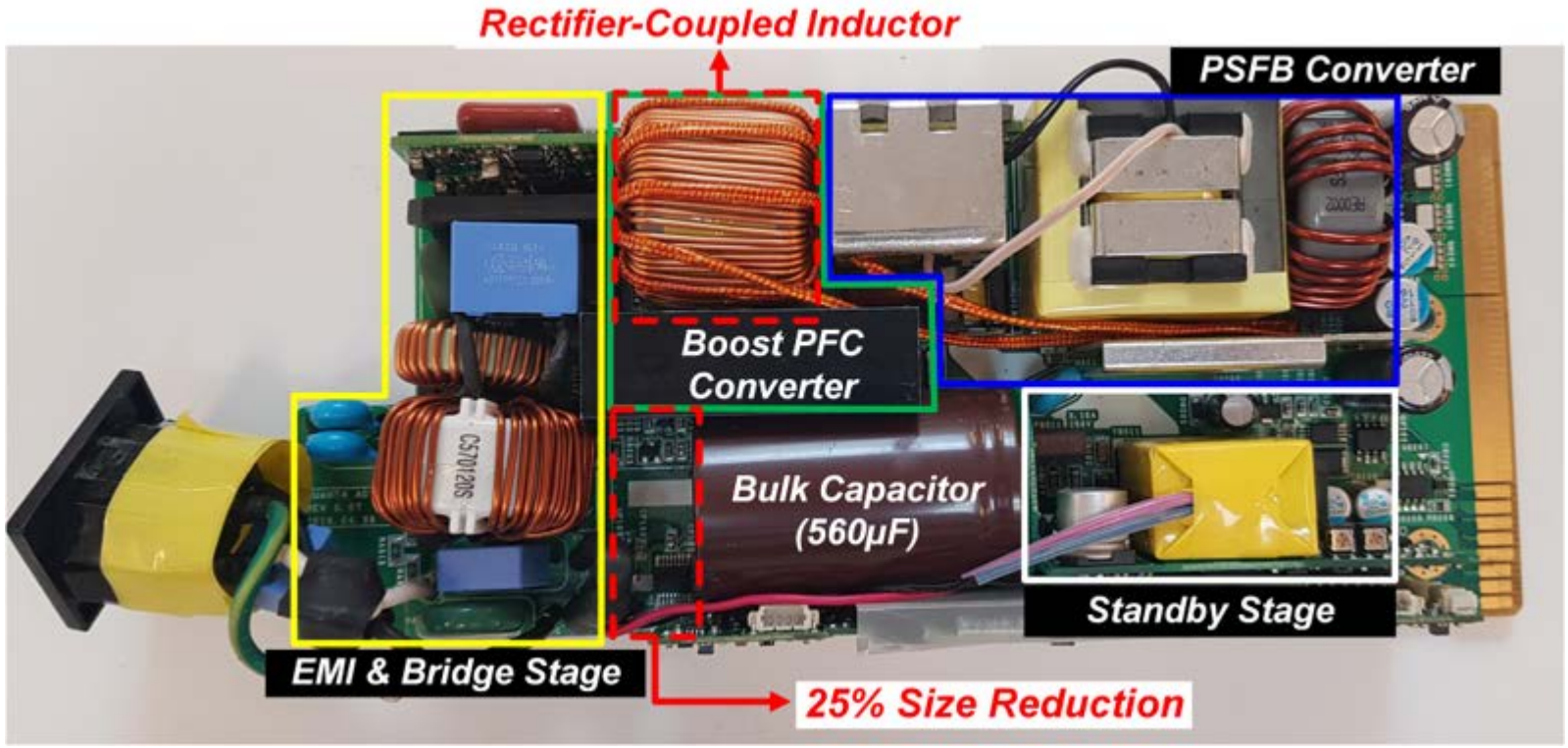
Modified 800W server power supply prototype



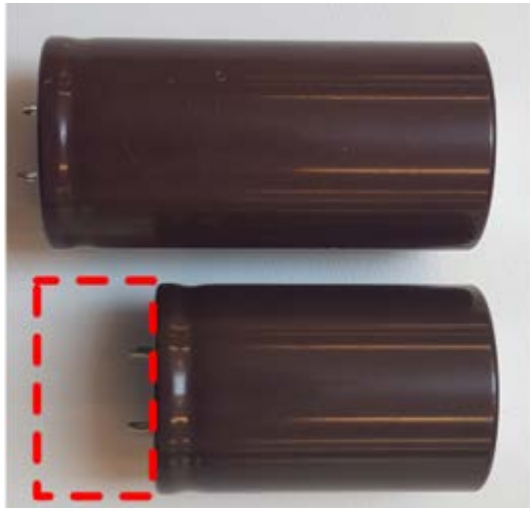
Conventional Inductor
N_A: 1.2Φ, 72 turns

Rectifier-Coupled Boost Inductor
N_A: 1.1Φ, 72 turns
N_B: 0.05Φ×320, 8 turns

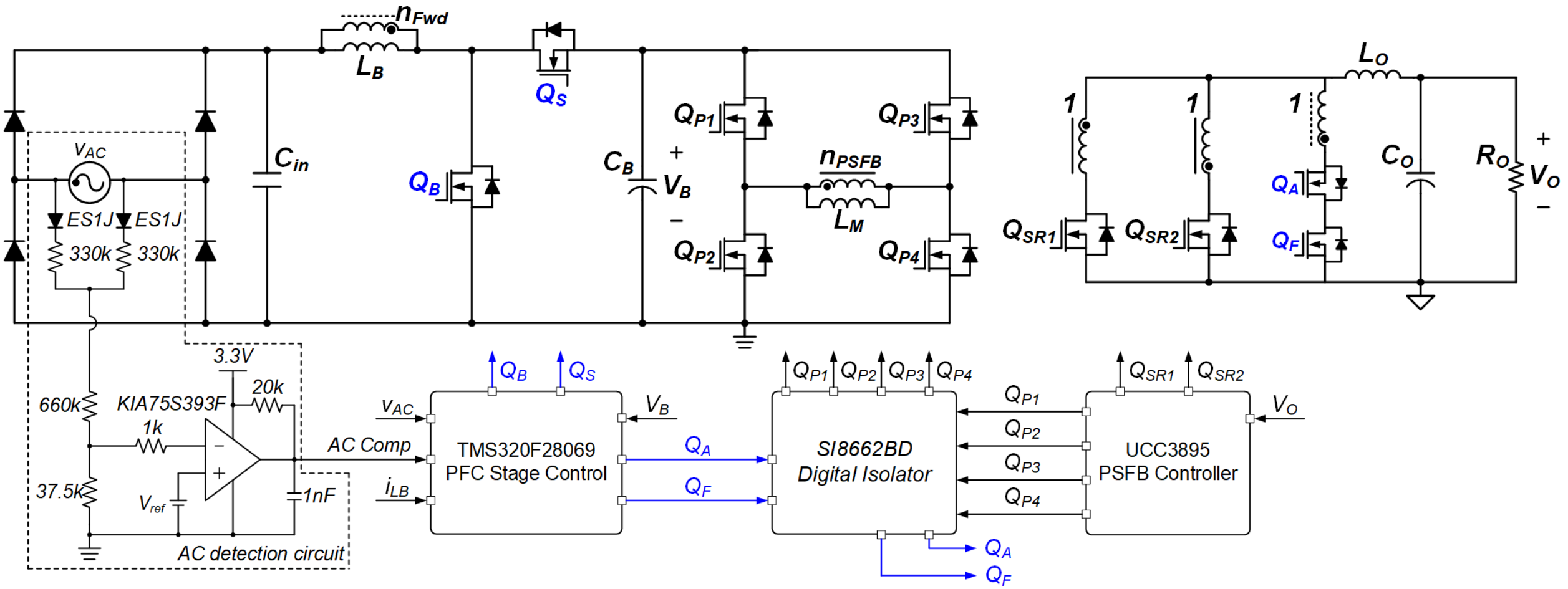
- Same size of rectifier-coupled boost inductor
- Smaller size of buffer capacitor (25% size reduction)
- Higher peak system efficiency in normal mode (95% -> 96%)

810μF
(42.411cm^3)

560μF
(31.809cm^3)



Control block diagram of prototype



1. Conventional method : Q_B & Q_S ➔ Always boost PFC operation
2. Reverse-feeding strategy : Q_B & Q_S ➔ Half-bridge forward operation (hold-up time)

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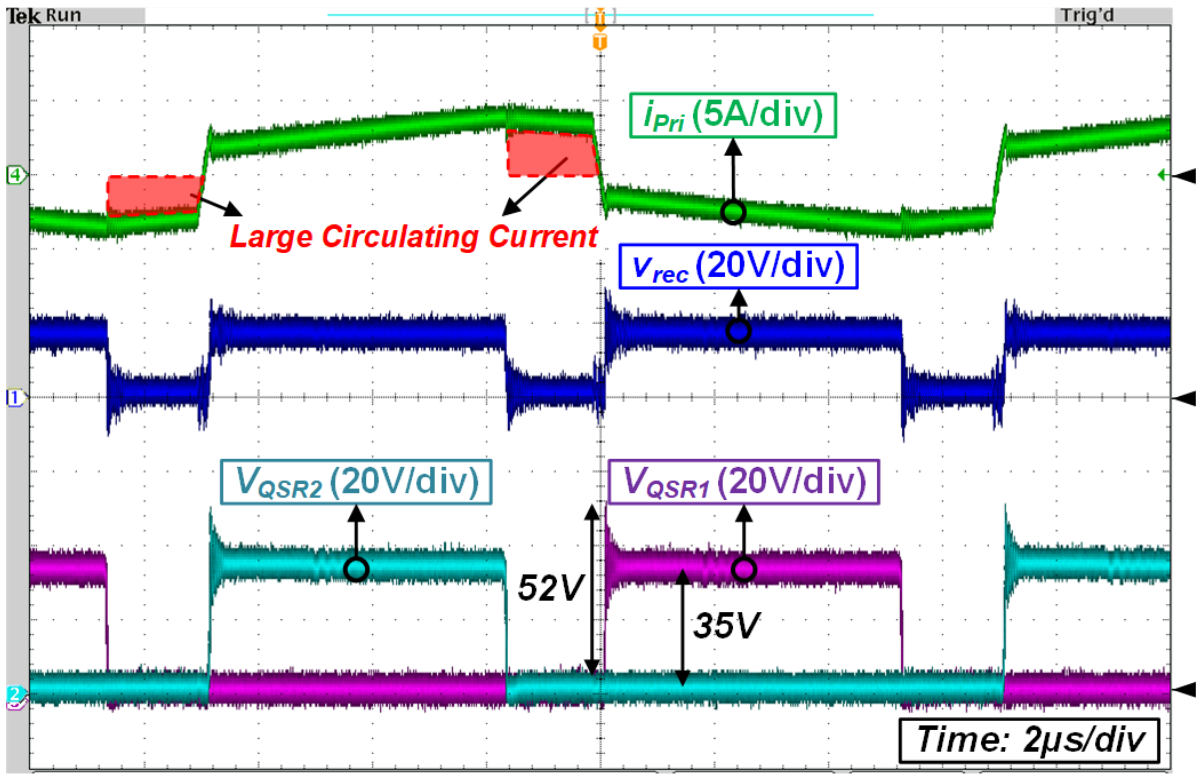
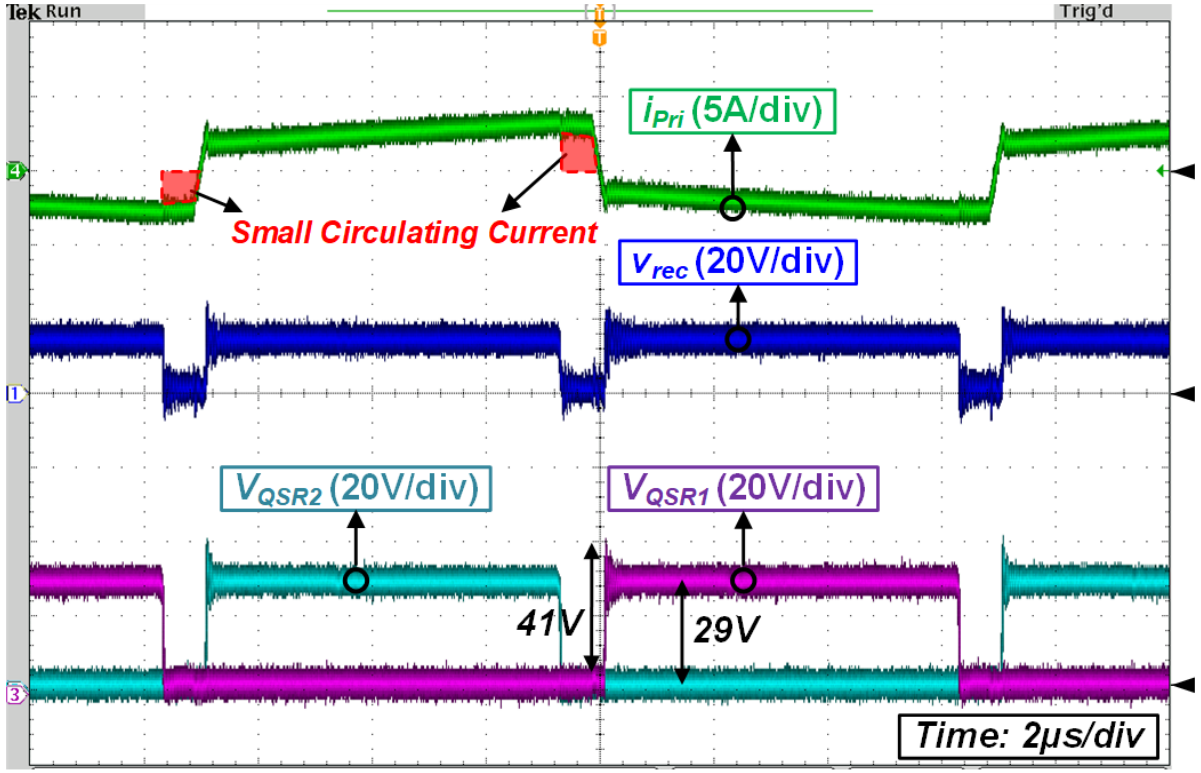
Measured waveforms in normal mode



[*Conventional PSFB converter*]

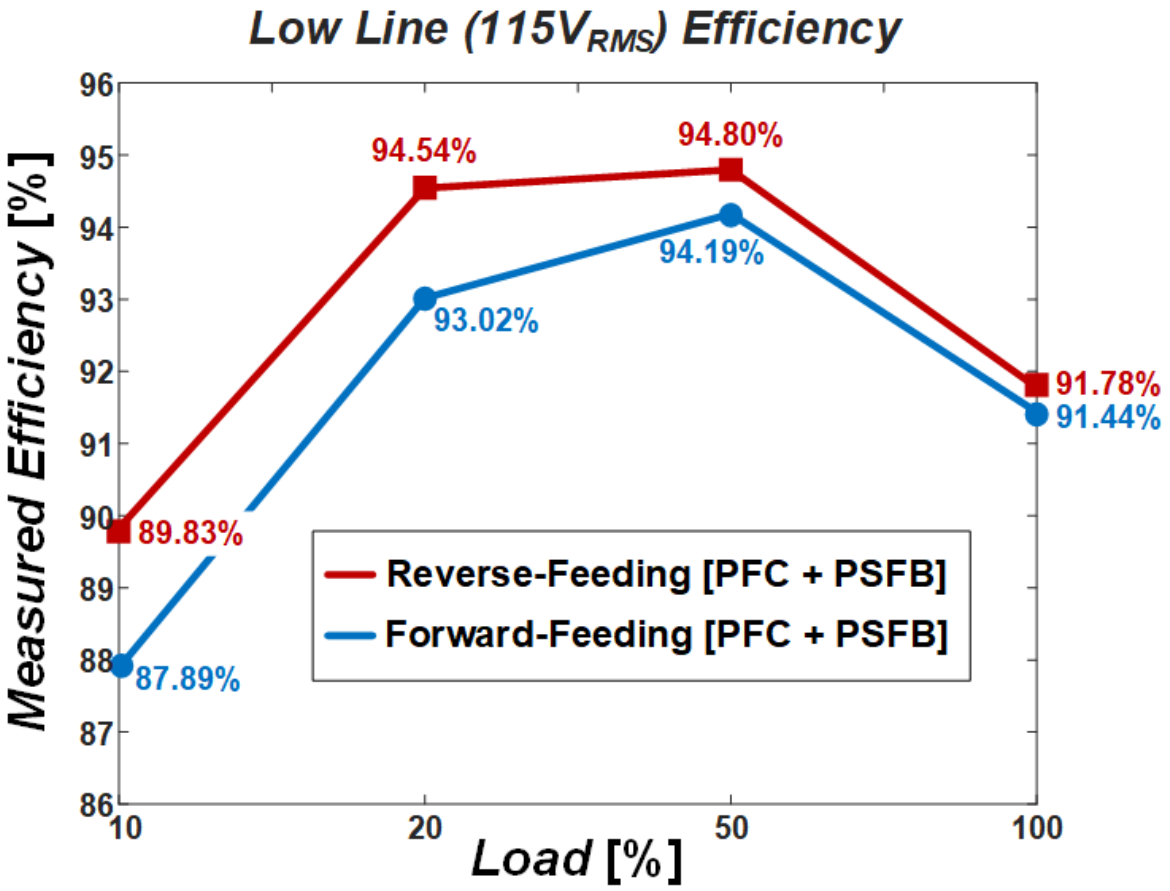
- Wide operation range design (320V-400V)
- High circulating current
- High inductor core loss, High voltage stress

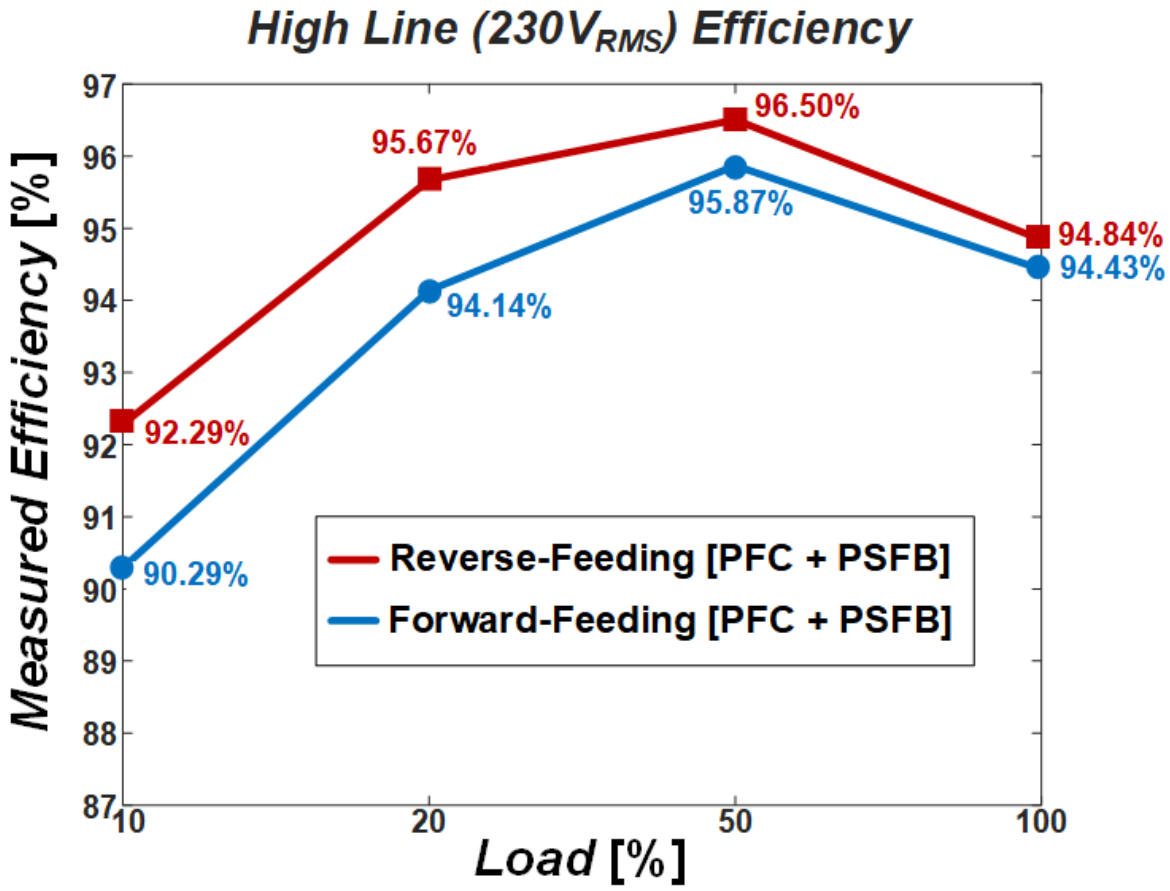


[*PSFB converter with reverse-feeding*]

- Narrow operation range design (380V-400V)
- Lower circulating current
- Lower core loss, Lower voltage stress

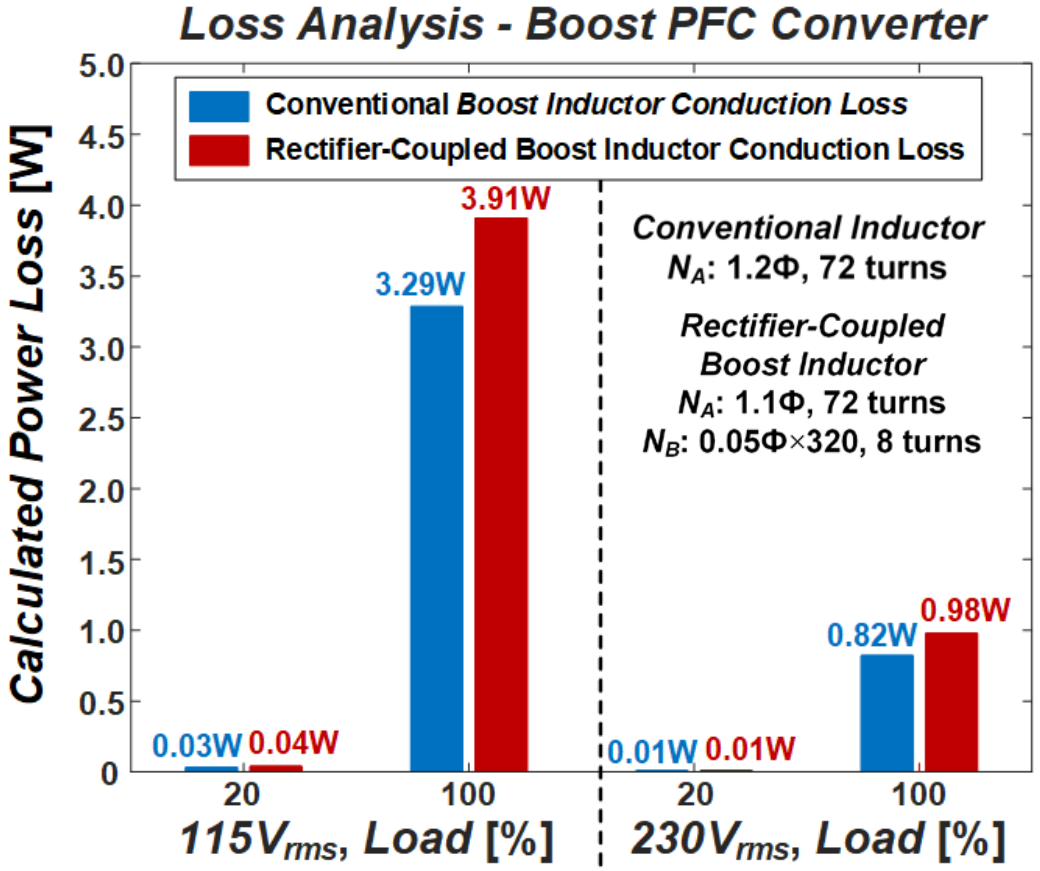
System efficiency in normal mode

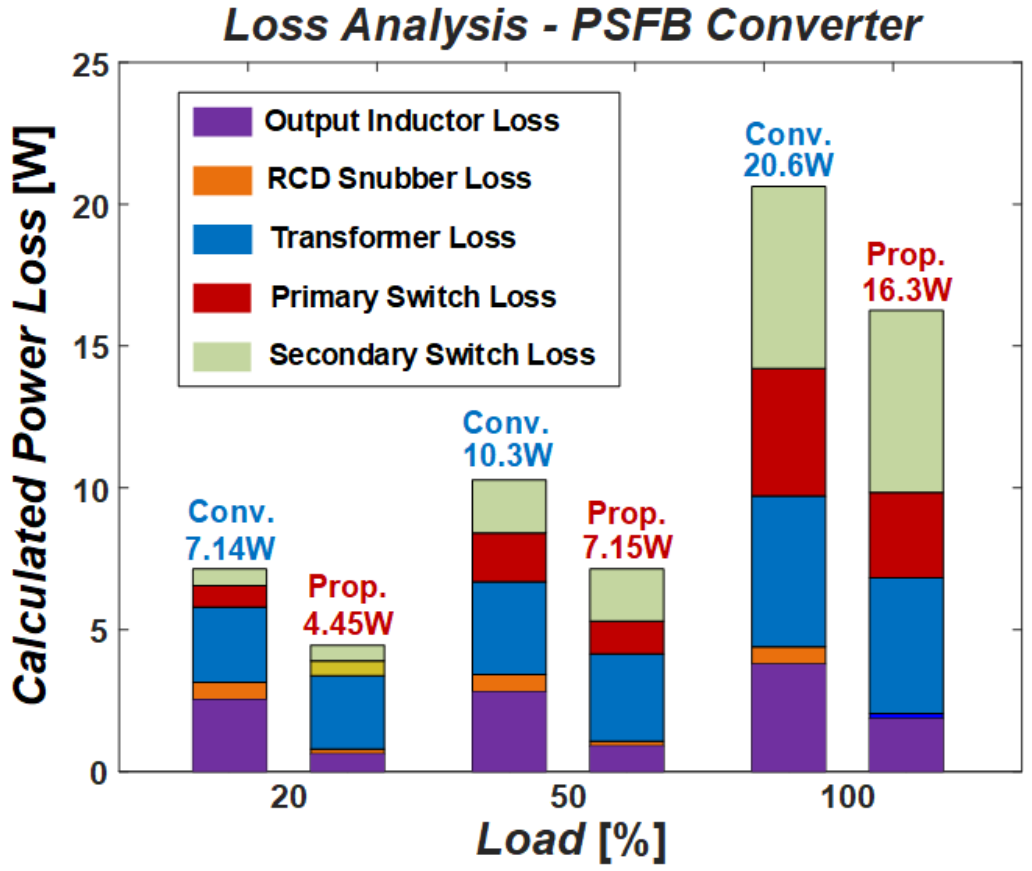




- Peak efficiency : 94.8% @ 115V$_{RMS}$ (+0.59%), 96.5% @ 230V$_{RMS}$ (+0.63%)

Normal mode loss analysis





- Similar boost PFC converter efficiency, Higher efficiency PSFB converter
- Reverse-feeding ➔ Higher system efficiency in universal line

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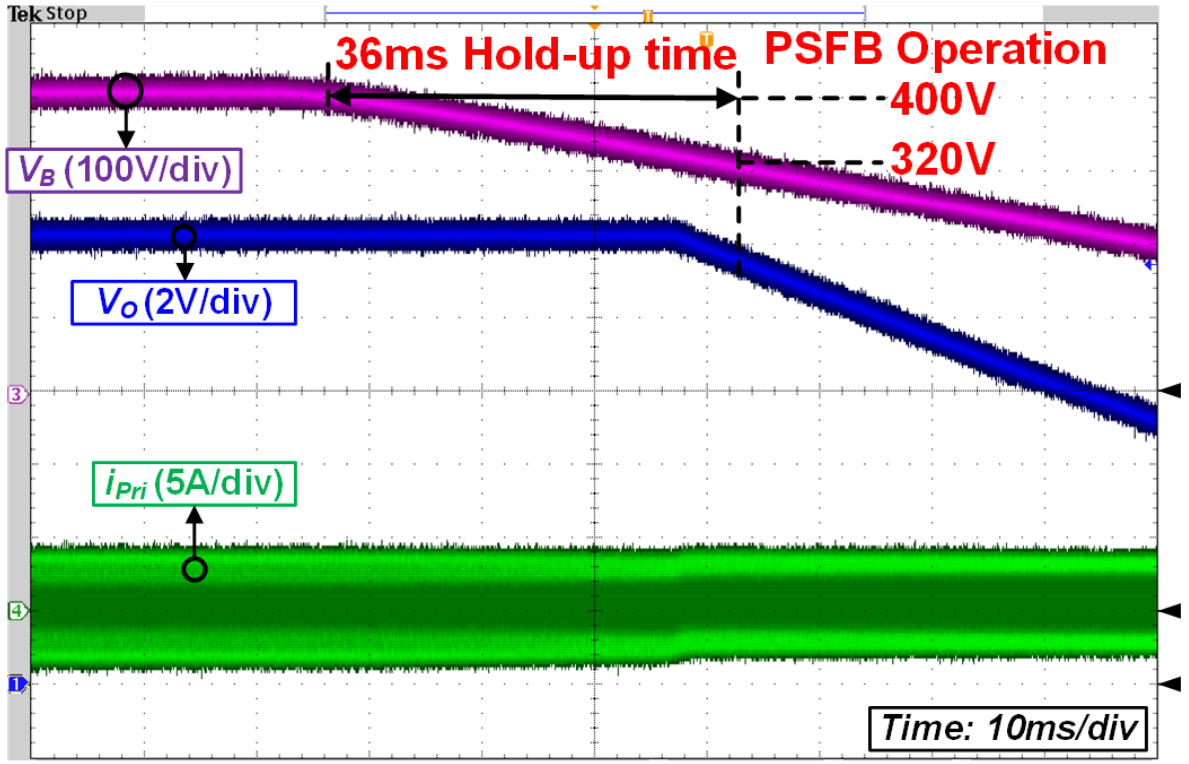
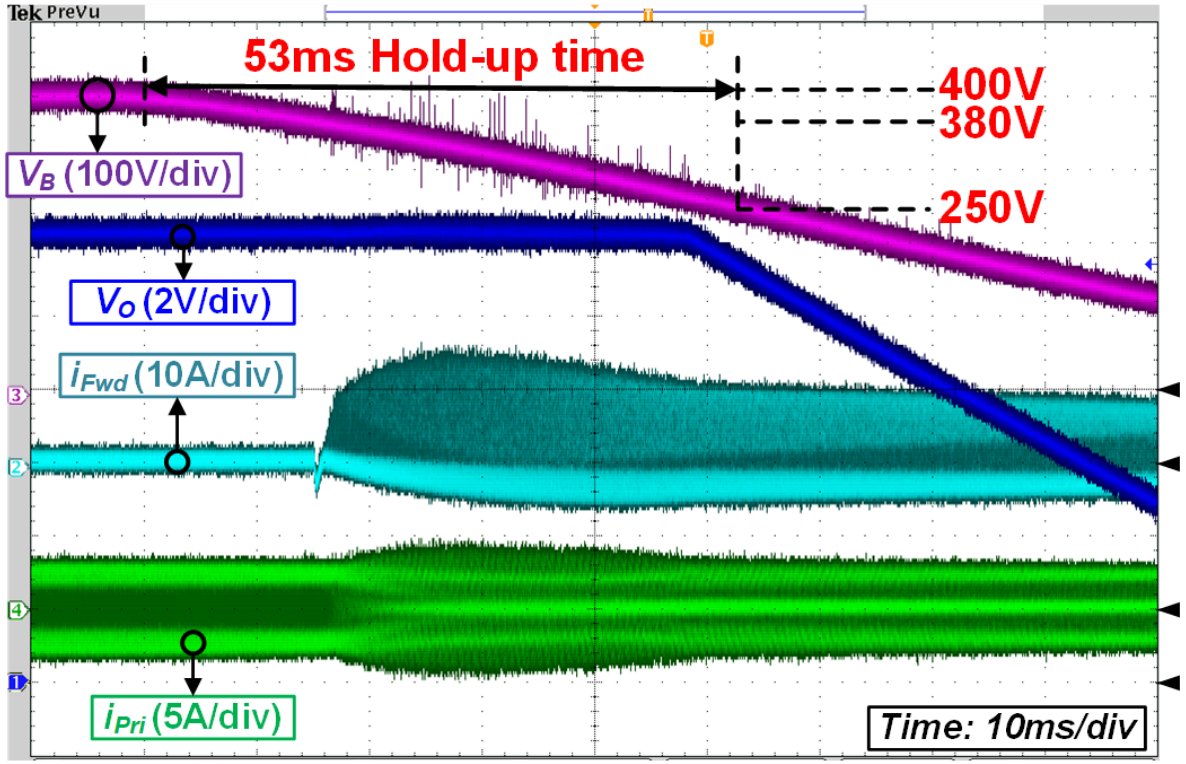
Measured hold-up time





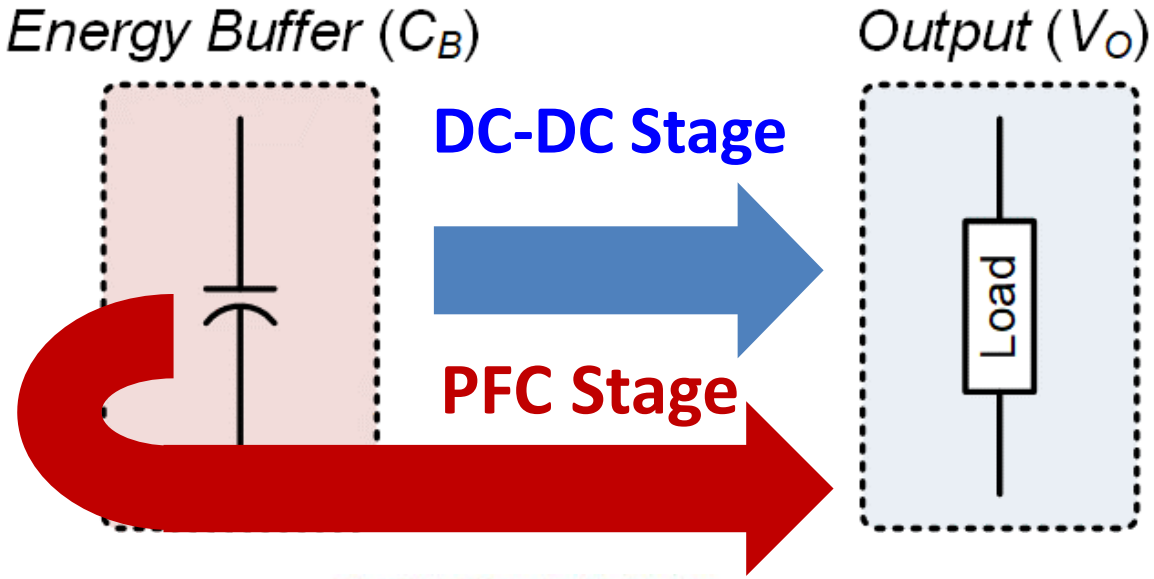
[*Conventional PSFB converter, n_{PSFB}=23:1*] [*PSFB converter with reverse-feeding, n_{PSFB}=28:1*]

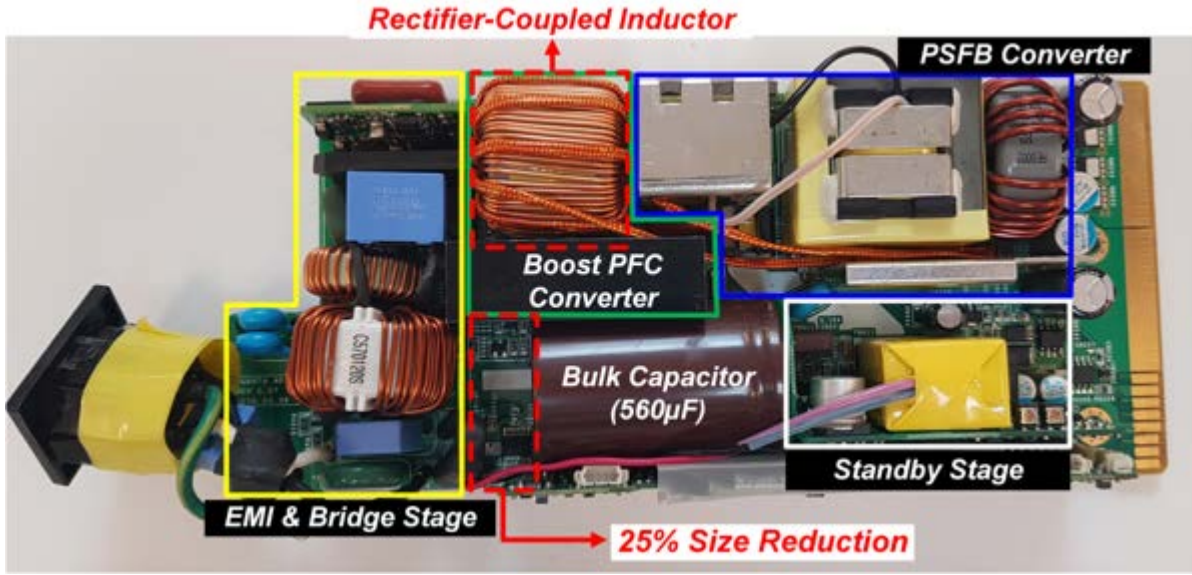
- Conventional forward feeding: 400V-320V ➔ PSFB operation (36ms hold-up time)
- Reverse feeding : (1) 400V-380V ➔ PSFB, (2) 380V-250V ➔ HB Forward + PSFB

(47% longer hold-up time with the same buffer capacitor)

Summary

- Reverse-feeding strategy for two-stage grid-interface PFC applications
  1. Inactivated PFC stage ➔ Reverse feeding
  2. Easier DC/DC stage design (DCX transformer)
  3. Wider operation range during hold-up time
- Applicable to a variety of PFC and DC/DC topologies
- Design example : 800W server power supply
- 96.5% (+0.63%) peak efficiency at $230V_{RMS}$
- 25% size reduction of buffer capacitor
  or 25% hold-up time extension





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