Multitrack Power Factor Correction Architecture

Minjie Chen, Sombuddha Chakraborty, David Perreault

Princeton University

Texas Instruments

Massachusetts Institute of Technology

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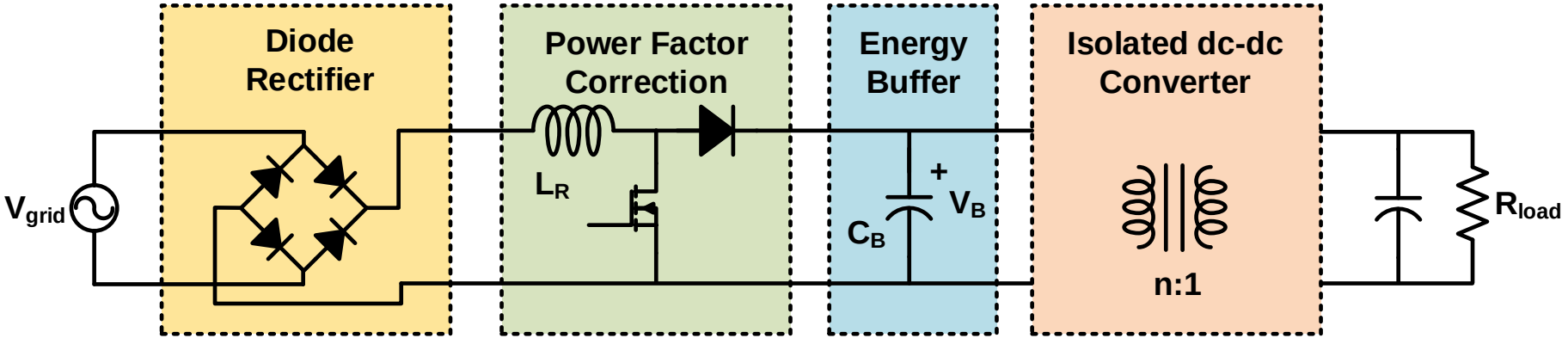
Typical isolated PFC architectures

Needed in a wide range of applications

Telecom supplies / EV chargers / Adapters / Industry Applications



Design targets:

(1) Higher efficiency
(2) Higher density
(3) Better grid interface

Challenges and opportunities:

(1) Smaller passive component size
(2) Higher frequency
(3) ZVS with universal input

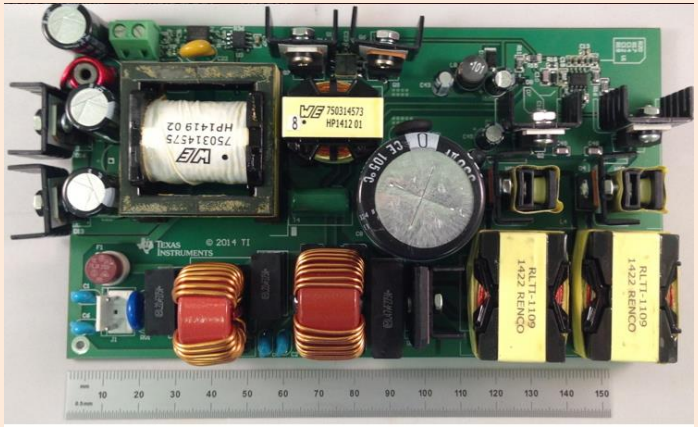
Existing solutions and design targets

Conventional "single-target" methods

- ***Diode loss*: bridgeless, totem-pole**
- ***Boost inductor*: FCML, Ćuk/SEPIC**
- ***Energy buffer size*: active energy buffer**
- ***Isolated dc-dc efficiency*: DAB, LLC**
- ***Smaller magnetics*: higher frequency**

- ***New architecture***
- ***5x - 10x Higher frequency***
- ***50W/inch³, 92% efficiency***

TI UCC25600 PFC Demo

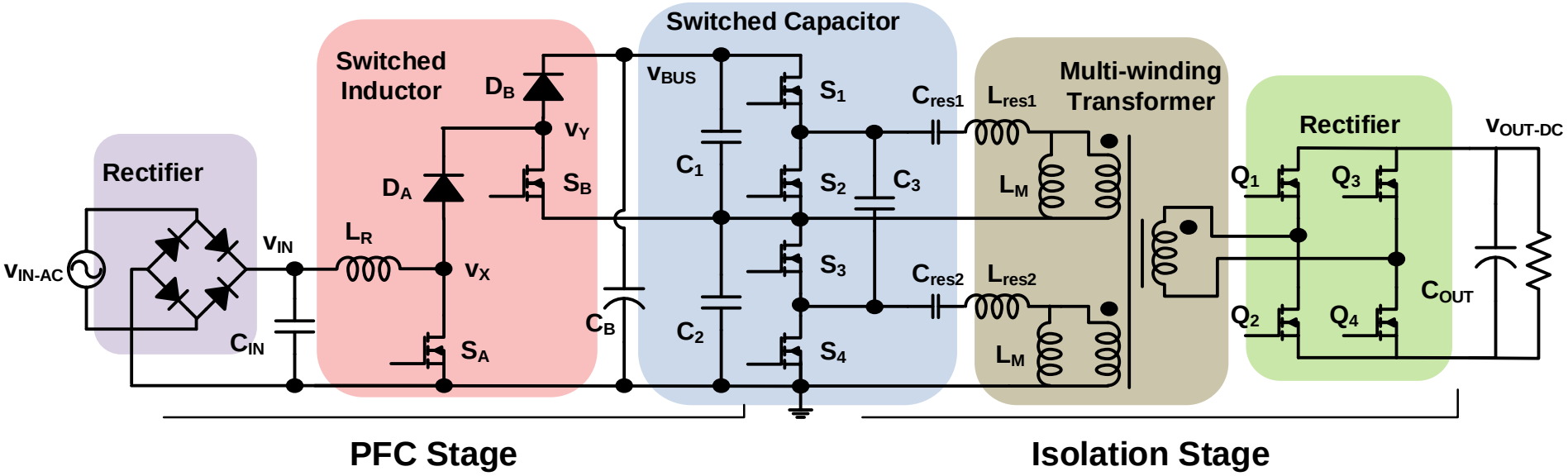


~ 10W/inch³, 200kHz
~ 92% efficiency

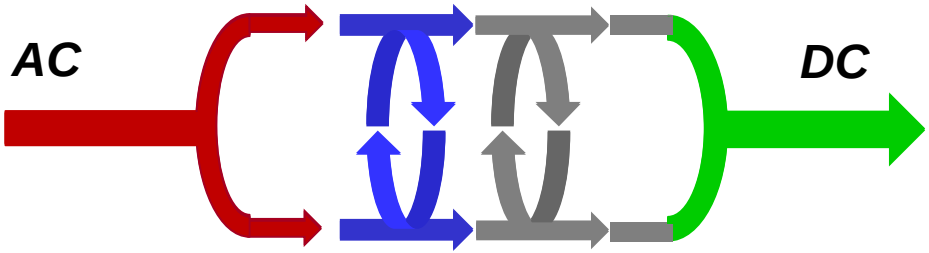
5x smaller ?

Develop a systems method to create mutual advantages

Multitrack PFC architecture

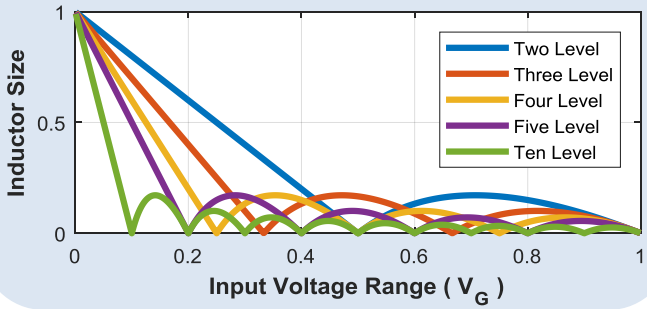


Deliver power in two or more balanced TRACKs



Advantages of the Multitrack PFC

Reduced inductor size (Multilevel)

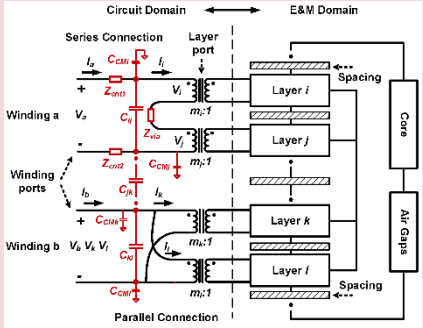


Reduced device rating

ZVS of switched-cap

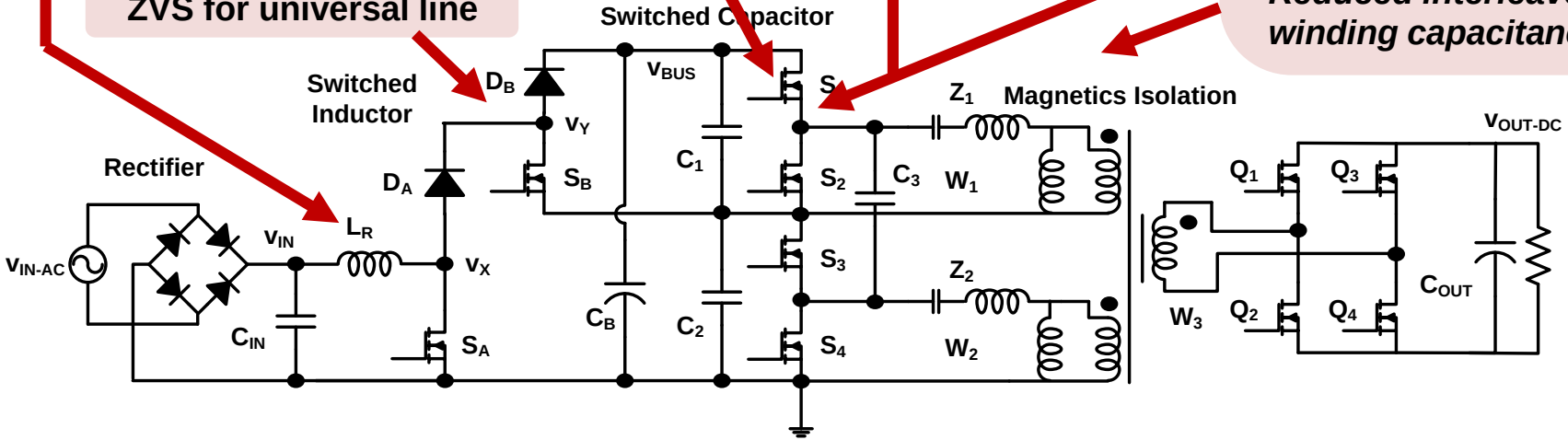
Reduced *dv/dt*

High Performance DCX



Reduced interleaved winding capacitance

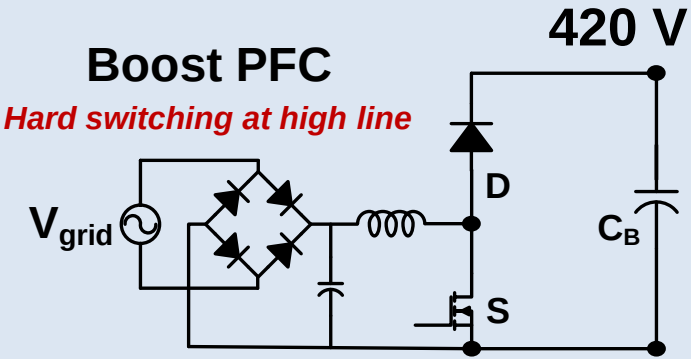
ZVS for universal line



Smaller inductor size and ZVS

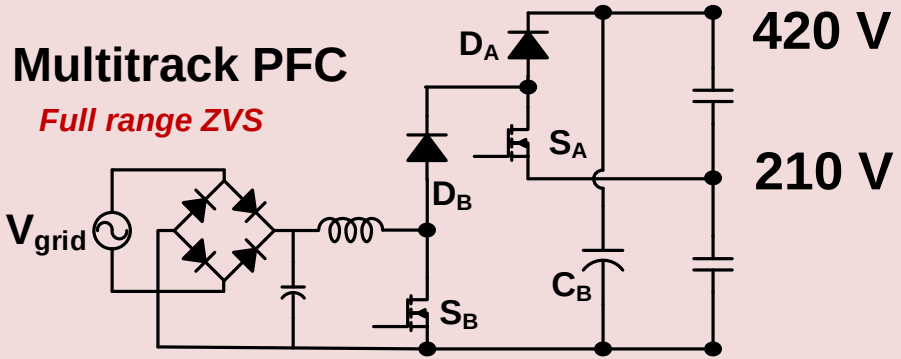
Boost PFC

Hard switching at high line



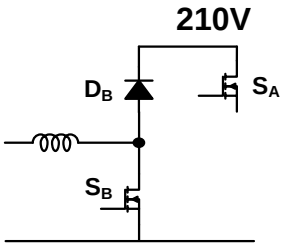
Multitrack PFC

Full range ZVS



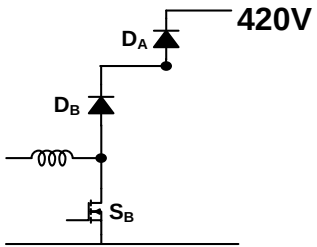
Three operation modes

Low Line



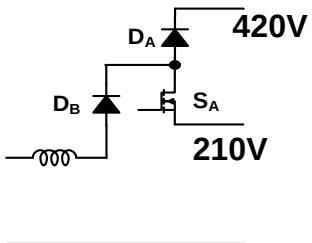
$|V_{grid}|<105V$

Mid Line

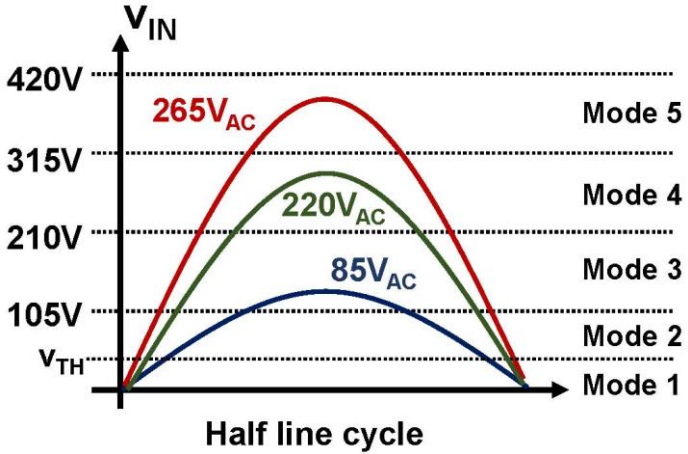


$105V<|V_{grid}|<210V$

High Line



$210V<|V_{grid}|<420V$

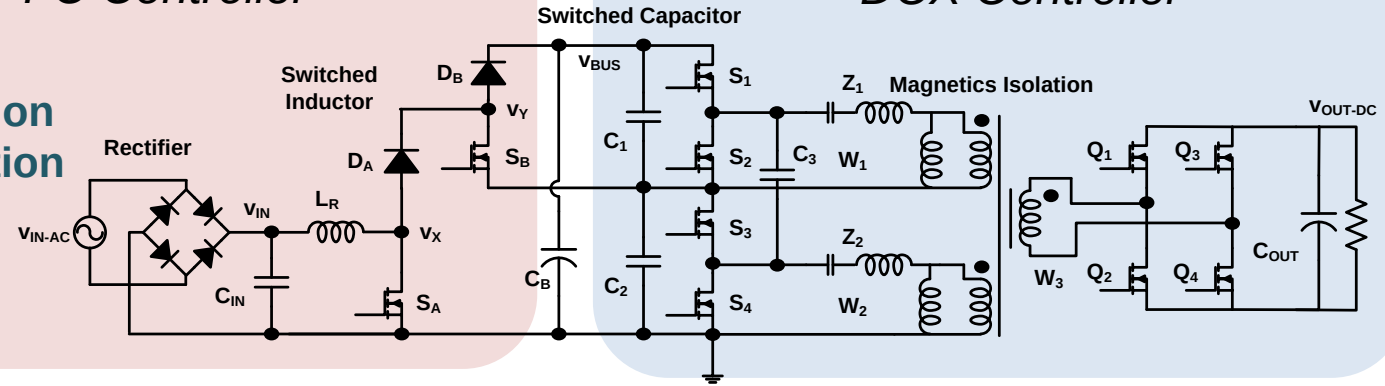


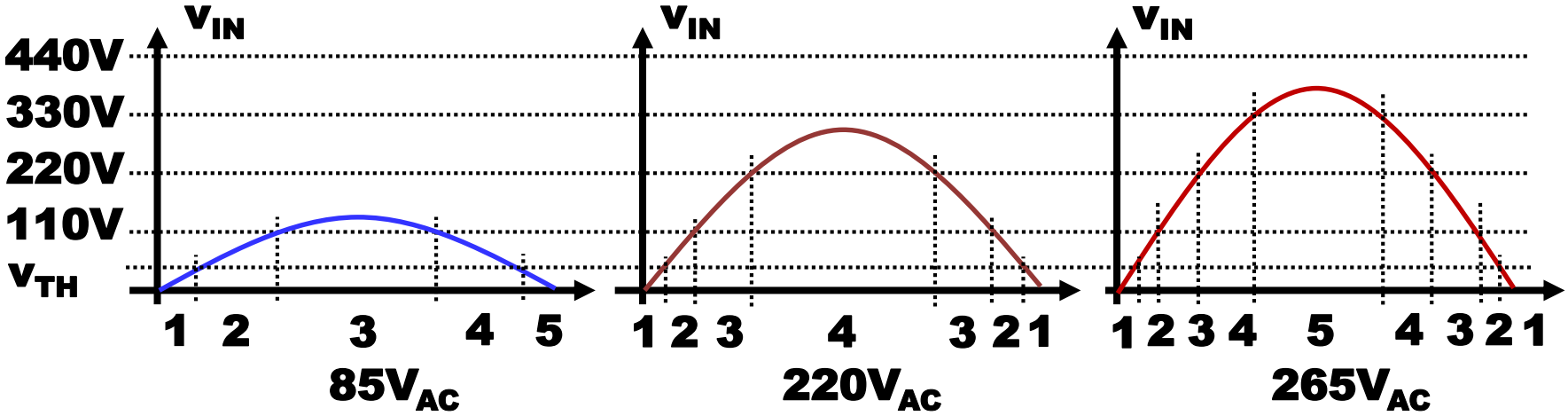
Control function blocks of the Multitrack PFC

Multitrack PFC Controller

- Voltage Regulation
- Current Modulation
- ZVS Timing
- Mode Selection

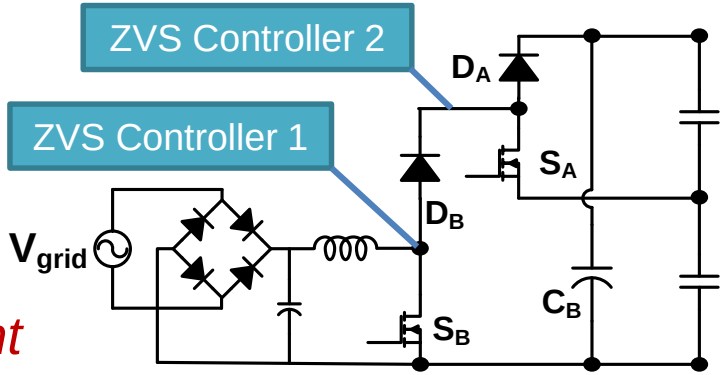
DCX Controller





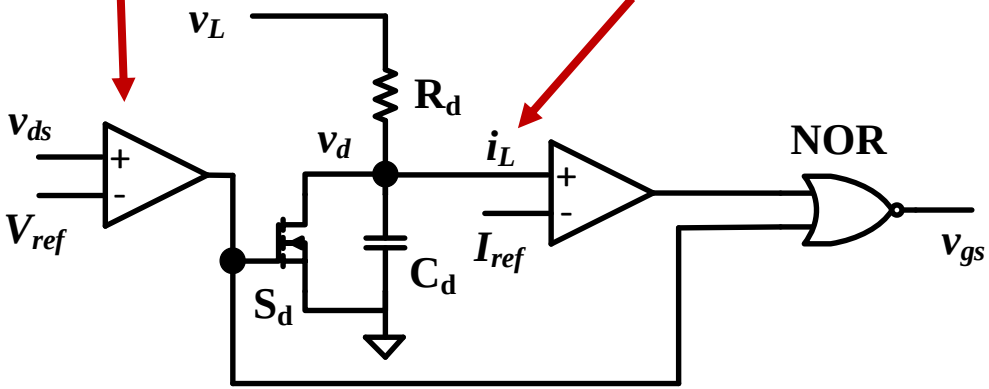
ZVS valley-detection circuits at MHz

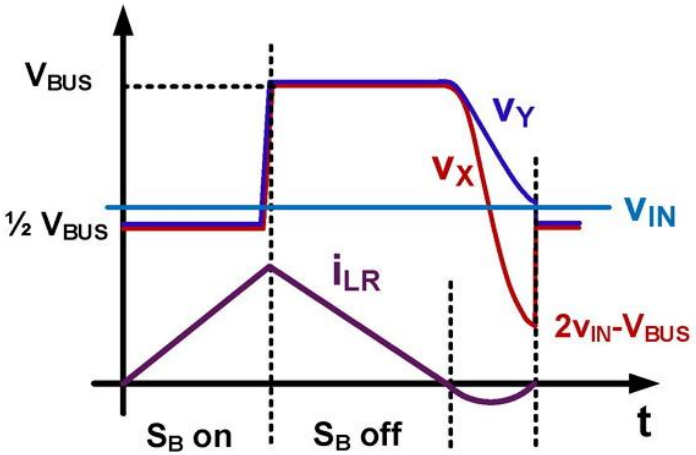
- *QSW-ZVS at 1-4 MHz*
- *Implemented as logic gates*



monitor drain voltage

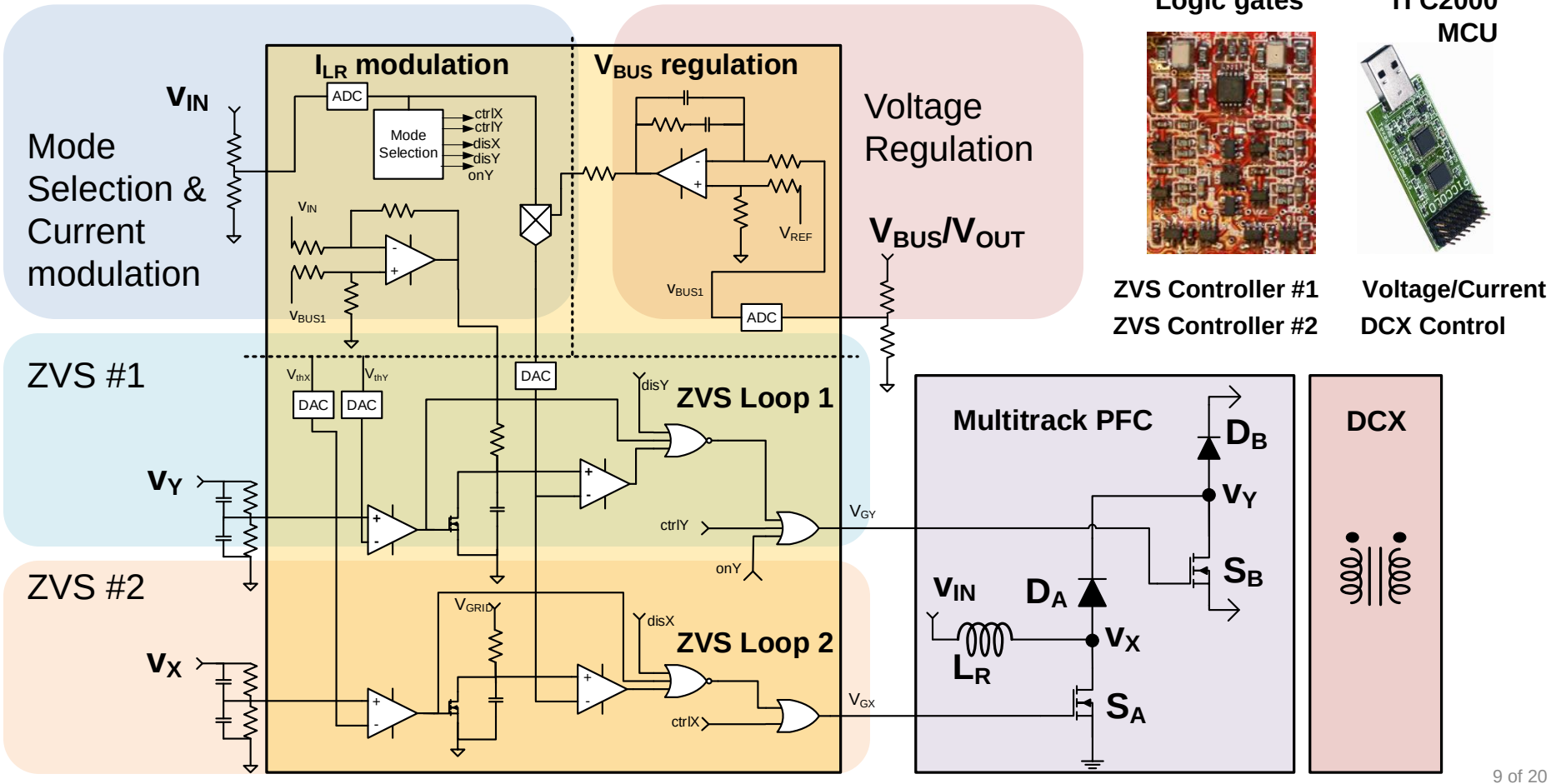
monitor inductor current (no current sensor)



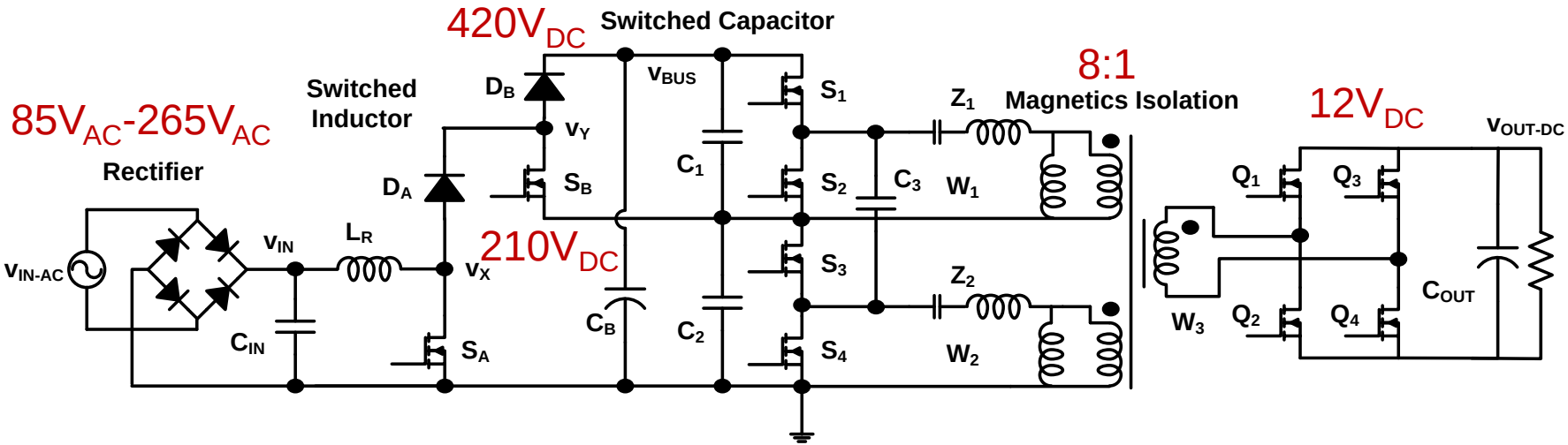


[S. Lim, J. Ranson, D. M. Otten and D. J. Perreault, “Two-Stage Power Conversion Architecture Suitable for Wide Range Input Voltage,” IEEE Transactions on Power Electronics, 2015.]

Complete Multitrack PFC controller

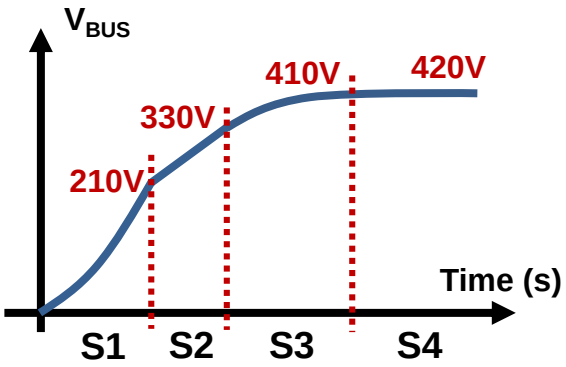


Startup and pre-charge of the Multitrack PFC



Startup Strategy:

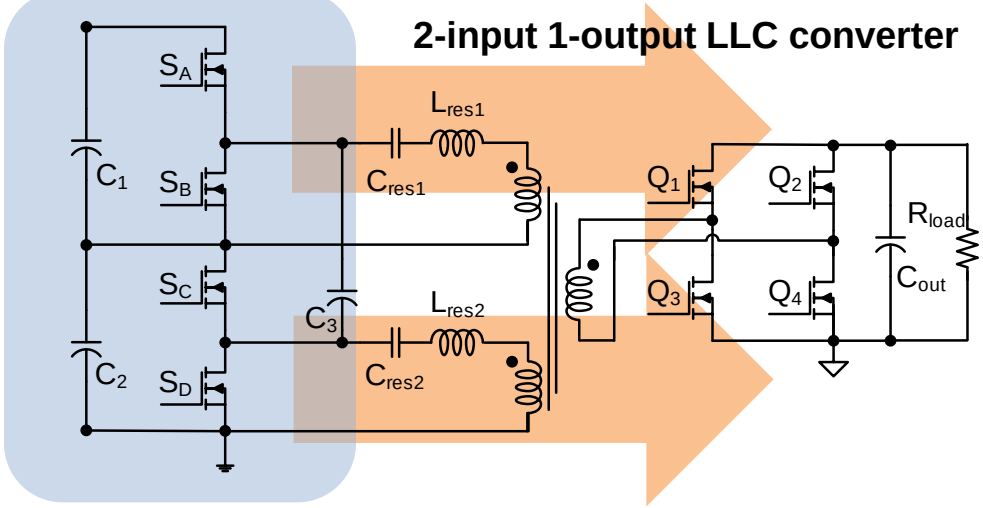
- Step 1: Inrush to 210V - keep SC operating, S_A off, S_B on until bus voltage reach 210V (50% of 420V).
- Step 2: Boost to 330V - force S_A on for a period (e.g., 100ns, 10% duty ratio), keep S_B off until bus voltage reach 315V.
- Step 3: PI + Non-ZVS - start PI regulation, non-ZVS.
- Step 4: PI + ZVS - continue PI regulation, maintain ZVS.



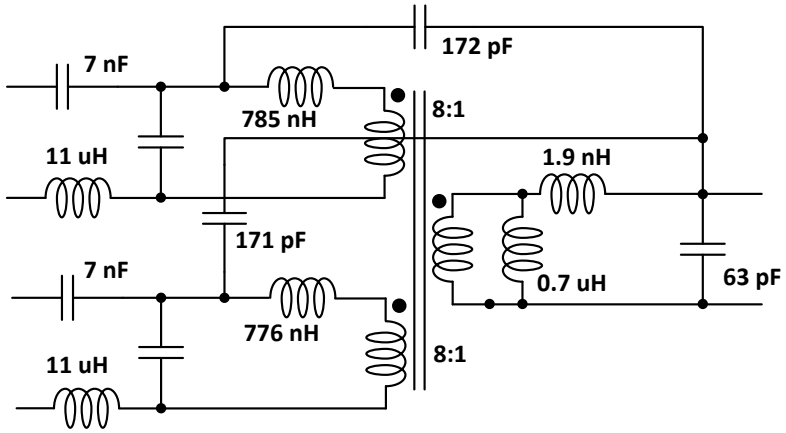
Design of the Multitrack DC transformer

2:1 switched cap converter

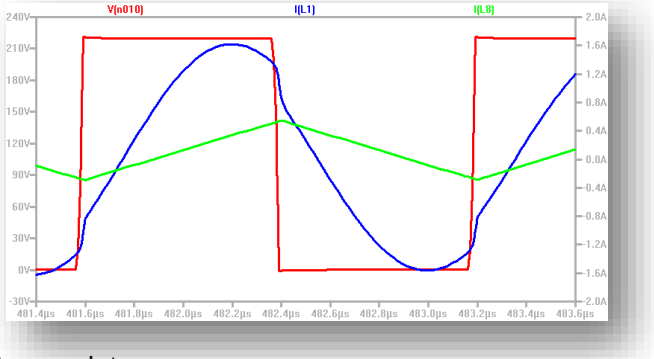
2-input 1-output LLC converter

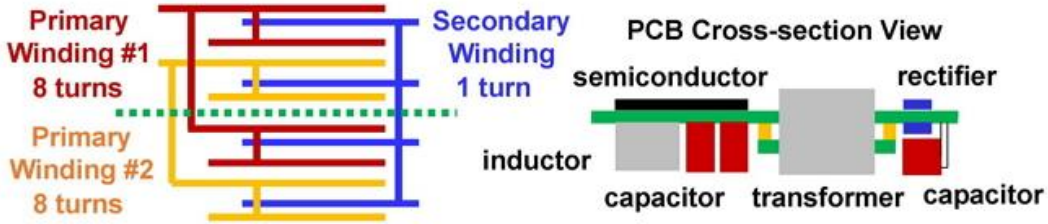


Extracted magnetics model



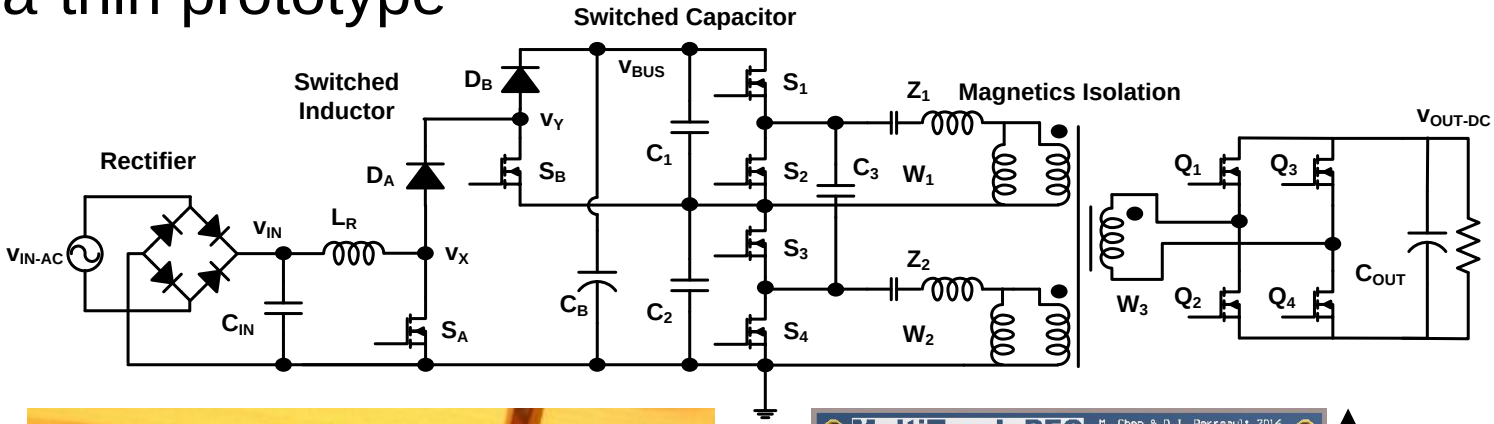
Low-Q LLC operation with ZVS

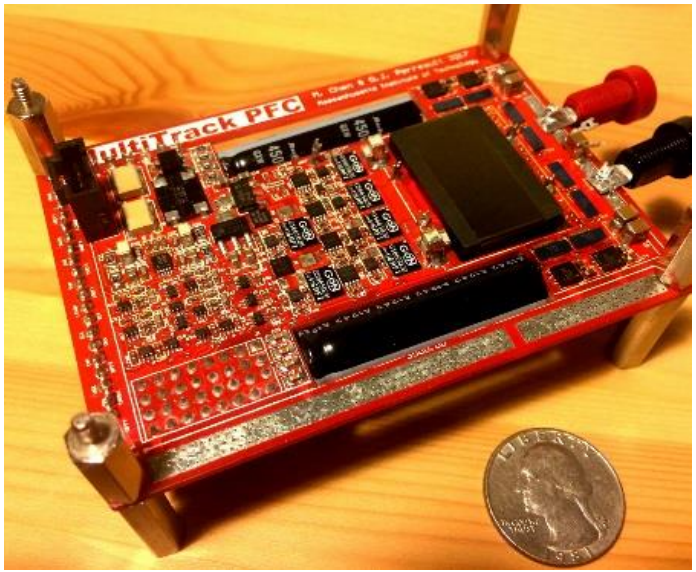


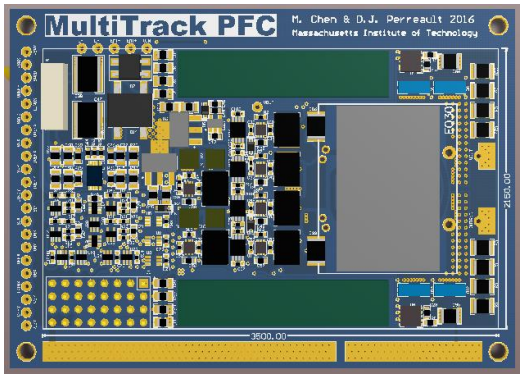


M. Chen, M. Araghchini, K. K. Afridi, J. H. Lang, C. R. Sullivan, and D. J. Perreault, “A Systematic Approach to Modeling Impedances and Current Distribution in Planar Magnetics,” IEEE Transactions on Power Electronics, 2016.

Ultra-thin prototype







Volume: 3 inch^3
Power: 150W
Efficiency target: 92%
Peak loss: 15W

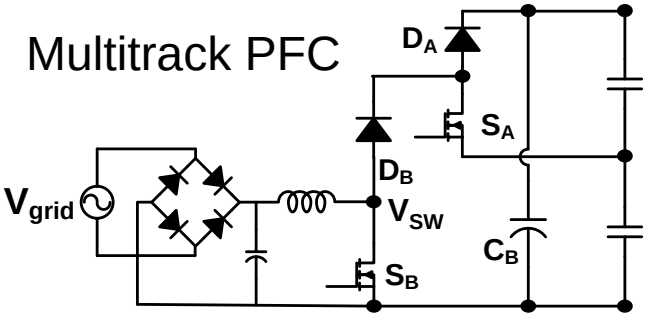
3.5 inch

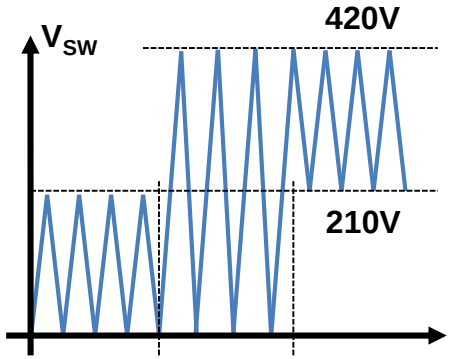
0.4 inch

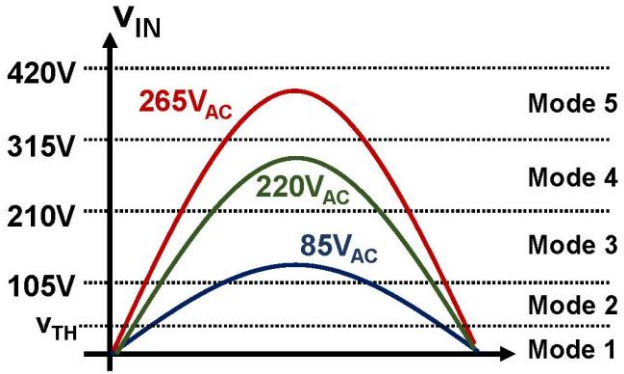
2.15 inch

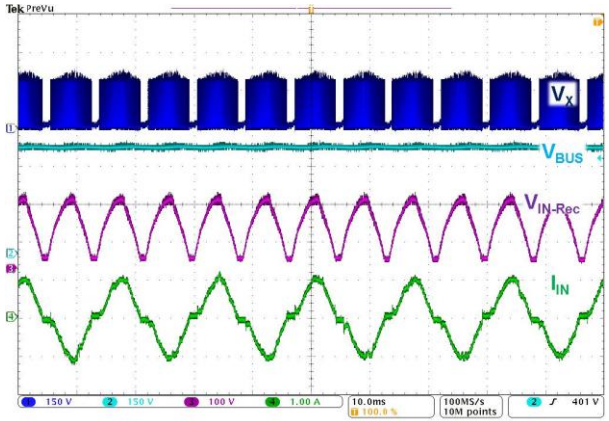
Electrolytic cap sets the height limit

Steady-state grid interface waveforms

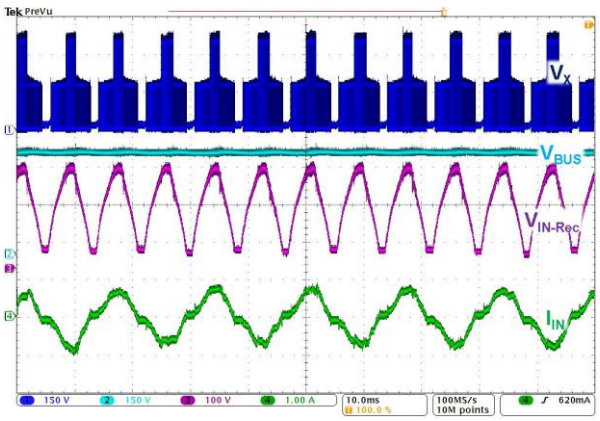




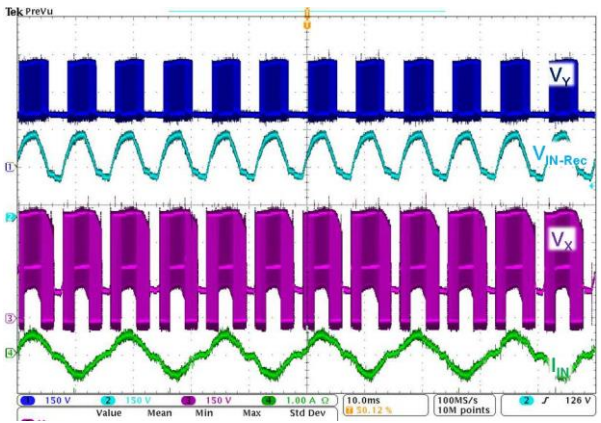




Low Line: 110 V_{AC}, 50 W



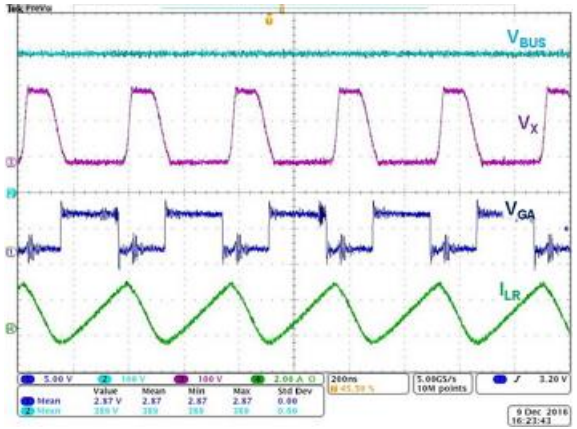
Mid Line: 220 V_{AC}, 100 W



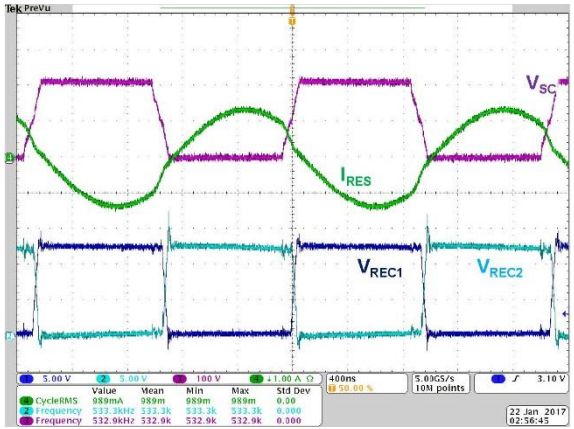
High Line: 250 V_{AC}, 120 W

Soft-switching operation

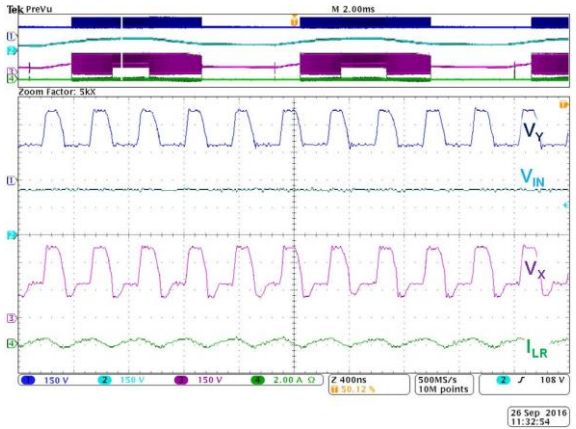
QSW-ZVS of the Multitrack PFC



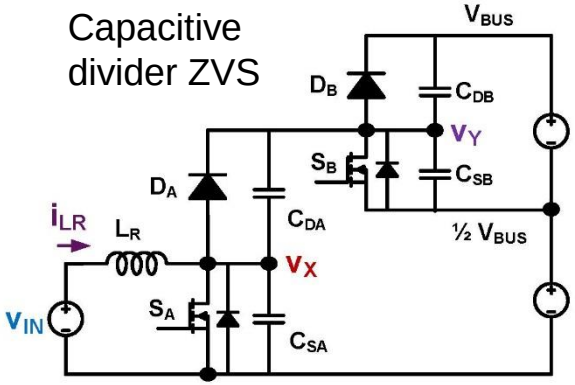
LLC-ZVS of the Swtched Cap

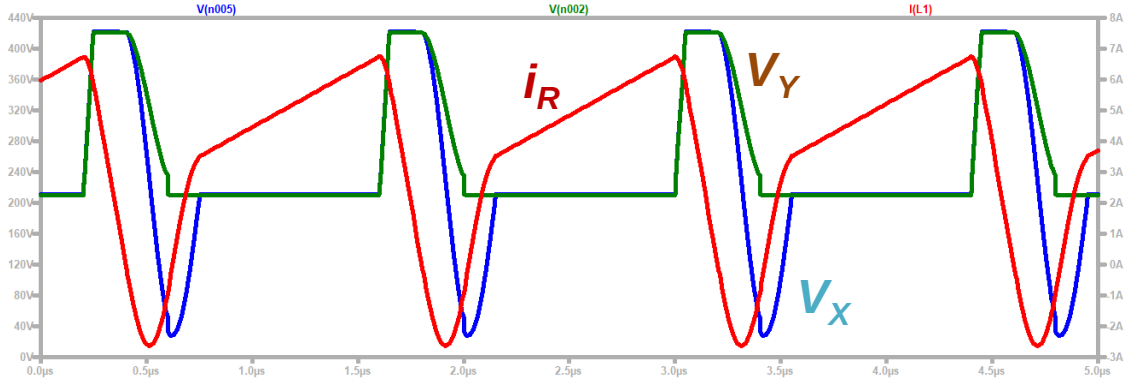


An unique Multitrack ZVS mechanism

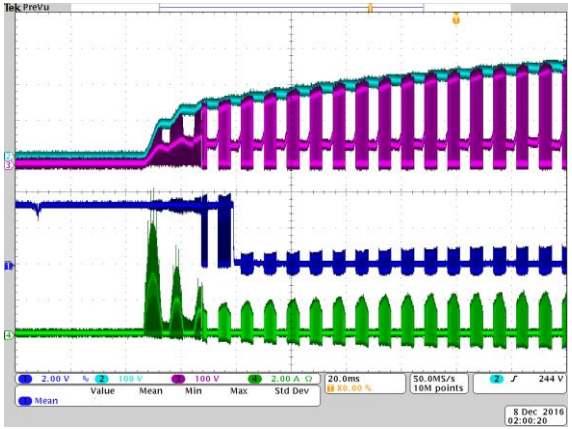


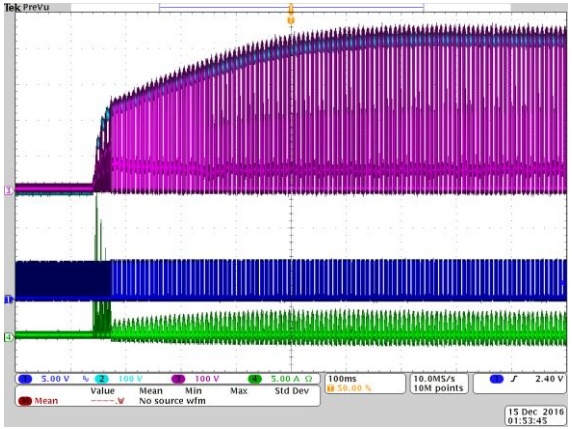
Capacitive divider ZVS

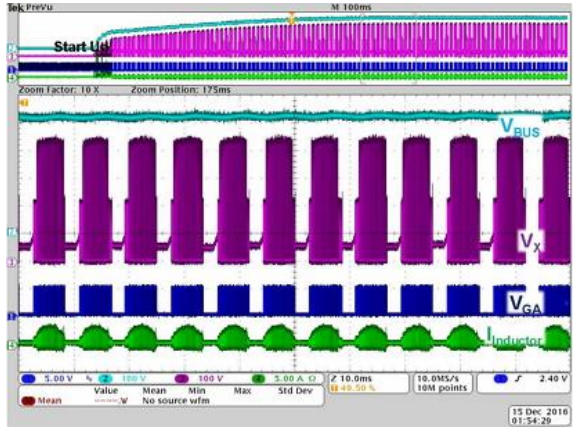




Startup waveforms





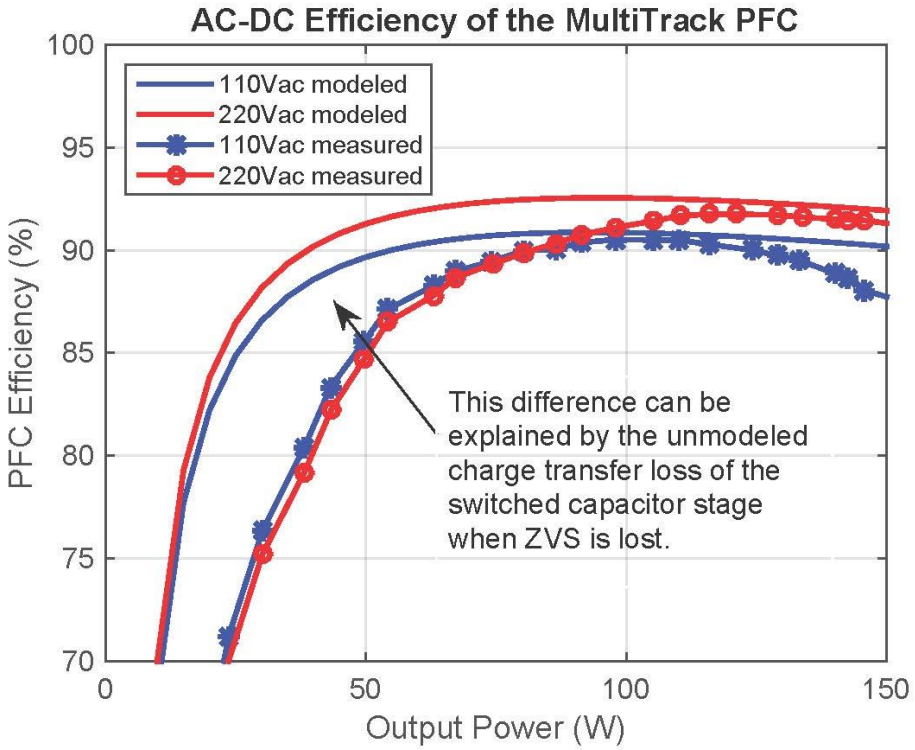


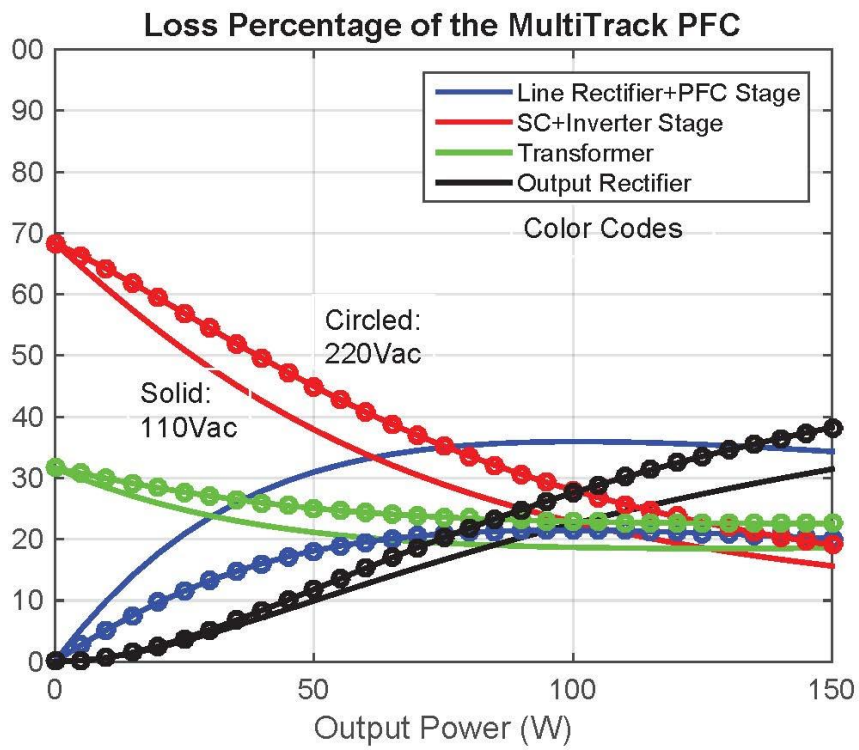
Inrush current Boost About 500ms PI control operation with ZVS

Startup Strategy:

- Step 1: Inrush to 210V - keep SC operating, S_A off, S_B on until bus voltage reach 210V.
- Step 2: Boost to 330V - force S_A on for a period (e.g., 100ns, 10% duty ratio), keep S_B off.
- Step 3: PI + Non-ZVS - start PI regulation, non-ZVS.
- Step 4: PI + ZVS - continue PI regulation, maintain ZVS.

Measured efficiency



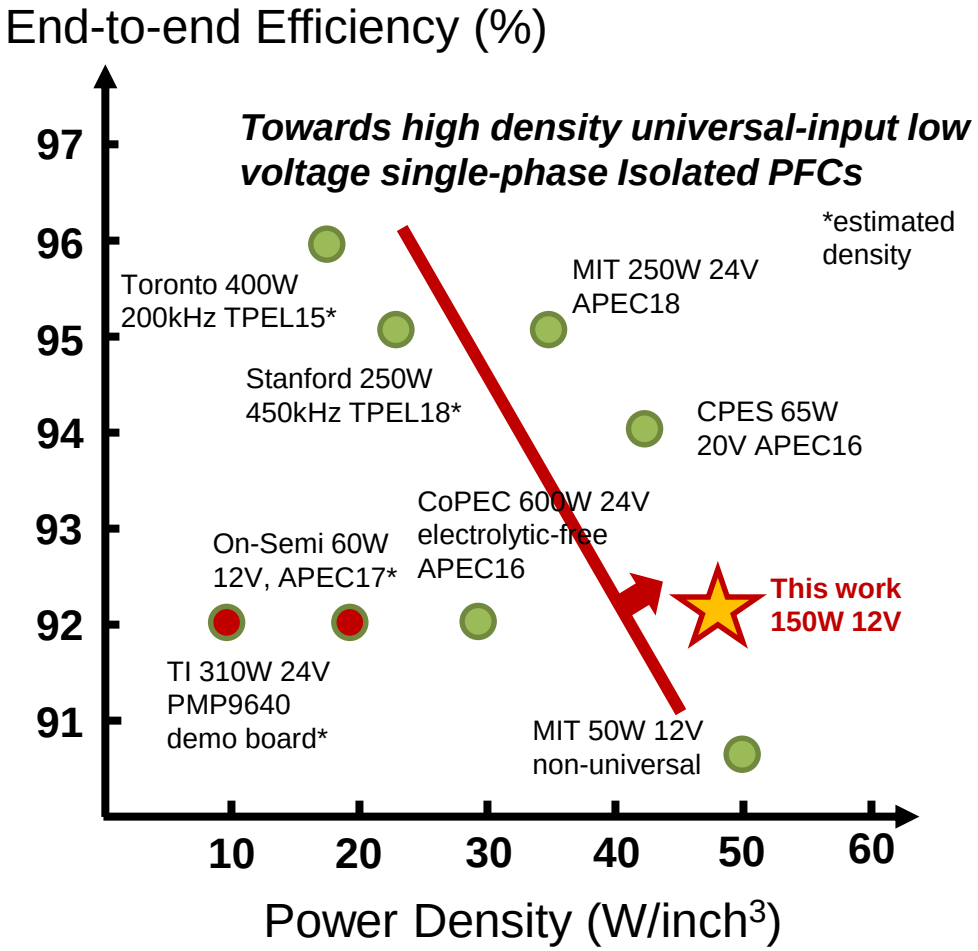


- High line efficiency: 92.0%
- Low line efficiency: 90.5%

- Light load: switched-cap loss
- Heavy load: rectifier loss

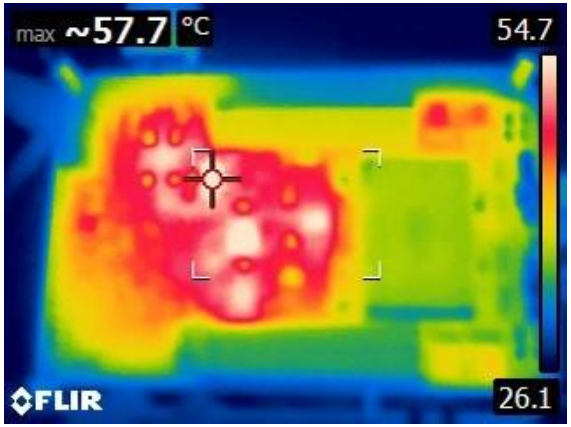
Summary

- A Multitrack PFC architecture for single-phase grid-interface.
- Density 50W/inch^3.
- 92.0% efficiency with 220V input.
- 90.5% efficiency with 110V input.
- Reduced inductor size.
- Reduced *dv/dt* on transformer.
- ZVS for MHz grid-interface.
- ZVS on switched capacitor.
- 1MHz-4MHz operation, potential to operate at higher frequencies.
- **A new design concept of creating mutual advantages.**



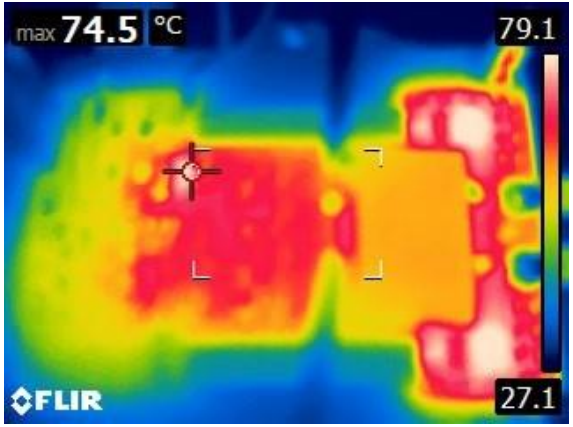
Thermal imaging of the Multitrack PFC

~200LPF forced air flow from left to right



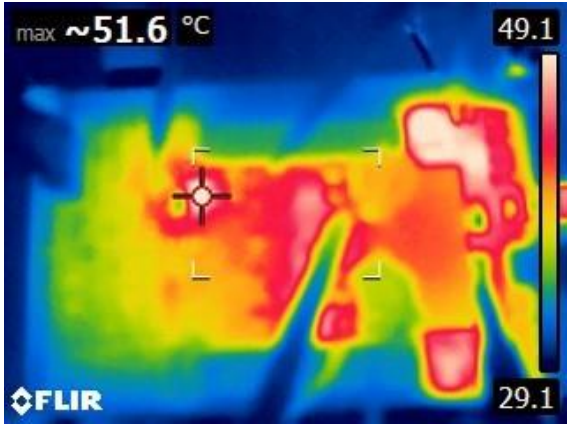
110Vin, ~50W

- System works in low line
- Switched cap circuit has high stress



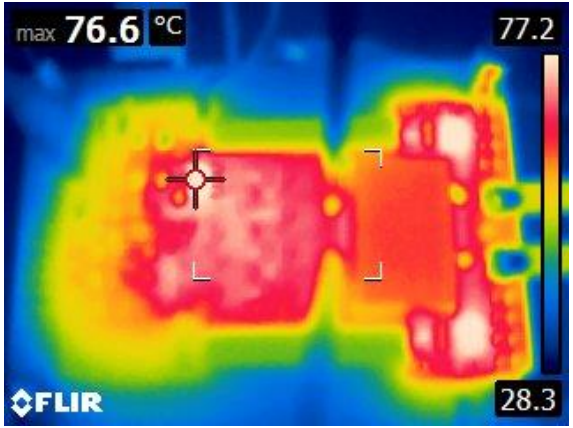
110Vin, ~100W

- System works in low line
- Rectifier loss dominating



220Vin, ~50W

- System works in high line
- Switched cap circuit has lower stress



220Vin, ~100W

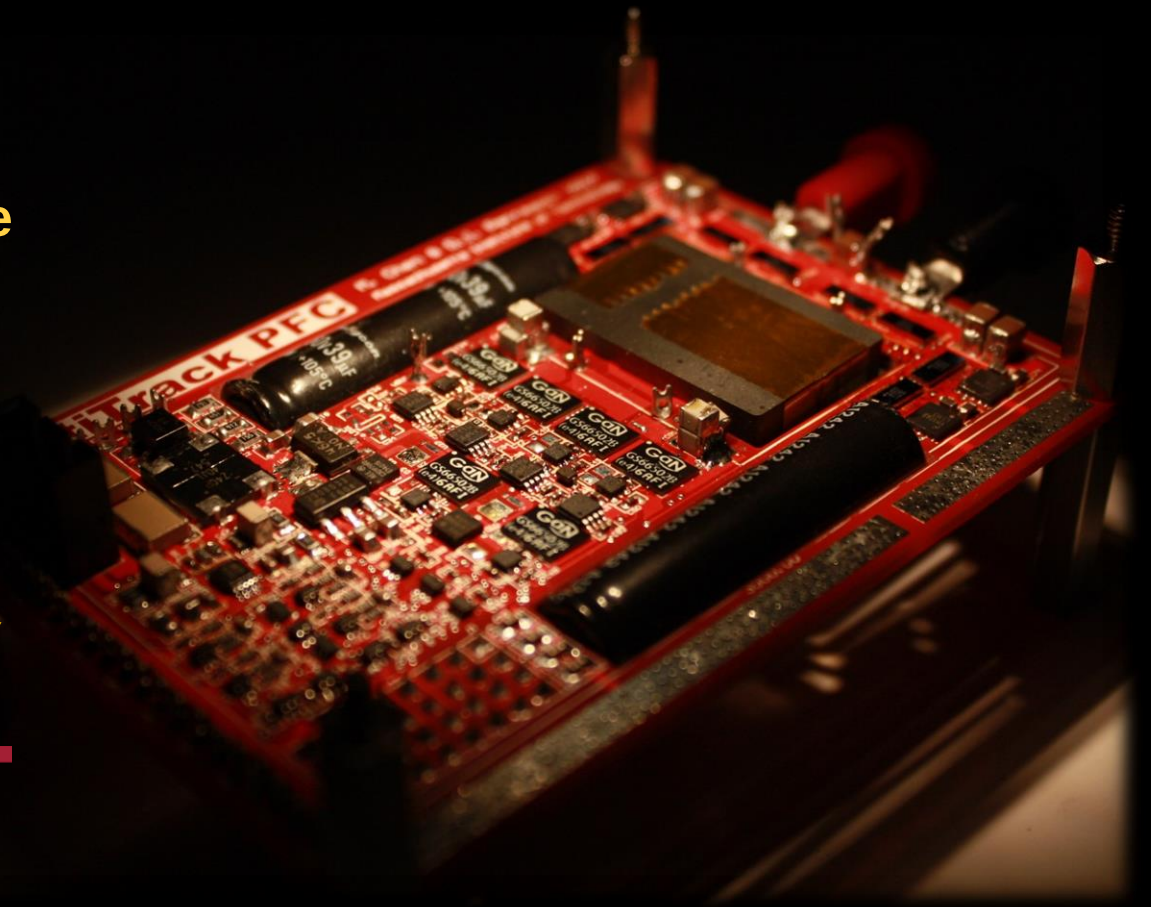
- System works in high line
- Rectifier loss dominating
- Primary side is very efficient

Thanks + Q&A

Multitrack PFC Architecture

Minjie Chen
Sombuddha Chakraborty
David Perreault

Princeton University
Texas Instruments
Massachusetts Institute of Technology



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Benchmark references

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