Series Voltage Compensator for Differential Power Processing

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***Abstract*—Differential power processing (DPP) has been proved effective in many applications. This paper presents a Series Voltage Compensator (SVC) with partial power processing to compensate for the voltage difference between a variable dc bus voltage and a regulated load voltage required by the DPP system. The SVC is connected in series between the variable dc bus and the DPP system. It regulates the input voltage while only processing a fraction of the overall power. A variety of SVC topologies are compared and their performance limits are studied, providing insights into the power rating design and regulation range selection of SVC topologies. To validate the principles of the SVC, a buck-derived SVC is designed and applied to a 10-port MAC-DPP converter. The buck-derived SVC can efficiently convert an input voltage ranging from 50 V to 85 V into a regulated 50 V and feed it to the DPP system. It achieved 98.8% peak system efficiency while converting 55 V into 50 V.**

***Index Terms*—differential power processing, voltage regulation, partial power processing, data center, photovoltaic system**

I. Introduction

Power delivery from high voltage dc bus to low voltage dc loads tends to require power converters that are bulky and inefficient. By stacking multiple loads in series, inherent voltage step down can be achieved. Only the power mismatch between series loads needs to be processed by the differential power processing (DPP) converter. The DPP architecture can minimize the power conversion stress and greatly improve the system efficiency [1]. DPP architecture has been proved effective in a wide range of applications such as battery management systems, solar photovoltaic, and servers and telecom loads in data centers [2]–[6].

One challenge of the DPP architecture is to regulate the stacked string voltage. In DPP systems where the series loads are directly connected to the input dc bus, the stacked DPP string voltage is fixed to the input dc bus voltage. The tightly-coupled load voltage and bus voltage might deteriorate the system performance. For example, in solar photovoltaic applications, the stacked string voltage needs to be adjusted in order to achieve maximum power point tracking (MPPT), but the dc bus voltage is relatively fixed. In other cases such as servers in data centers, the dc bus voltage in a server rack may change between 48 V to 54 V, whereas the IT equipment needs precisely regulated voltage (e.g., 24 V, 12 V, or 5 V) to function properly. A regulation stage is needed to decouple the series stacked load from the dc voltage bus, achieving a wide input voltage range while maintaining high performance.

The most straightforward way of implementing the voltage regulator is to design a standalone front-end dc-dc converter. In this case, however, full load power needs to be processed by the front-end dc-dc converter, limiting the overall system efficiency and power density that can be achieved. An alternative way is to regulate the DPP string voltage through partial power processing. A composite converter concept was proposed in [7], [8]. The power processing is split into a main path and a partial path. The main path is a high efficiency dc-dc converter with a fixed conversion ratio, and the partial path is a partial power converter. The fixed-ratio converter may not be needed if the main power is directly delivered to the loads [9]–[11]. The partial power converters have been implemented in photovoltaic systems to realize MPPT [12], [13].

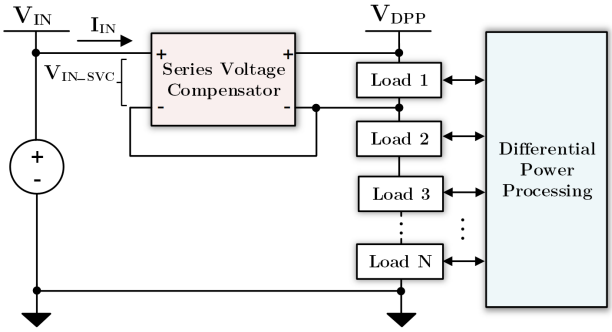

Fig. 1. A series voltage compensator (SVC) leveraging the partial power processing concept in DPP systems. The SVC is connected in series between the DPP stack and the input voltage.

Leveraging the partial power processing concept, this paper presents a Series Voltage Compensator (SVC) for voltage pre-regulation in DPP architectures. Different from a standalone voltage pre-regulator, the SVC is connected in series with the DPP loads, compensating for the voltage difference between the input dc bus and DPP systems, as illustrated in Fig. 1. The SVC inherits the advantages of the series-stacked DPP architecture. It only processes a portion of the overall system power and delivers it to the top few voltage domains. The majority of power is directly delivered to the DPP loads. The SVC can be implemented as many different topologies with tradeoffs in voltage regulation range, control complexity, efficiency, and component count. To validate the SVC concept, a buck-derived SVC topology is designed and applied to a multiport-ac-coupled DPP (MAC-DPP) converter [6]. In addition to reduced power rating, the buck-derived SVC can also enable soft-start and fault protection functions. A decoupled control strategy for the SVC and MAC-DPP is developed and validated with transient simulations. Experimental results show that the SVC can precisely regulate the DPP load voltage, and can achieve over 98.8% peak system efficiency.

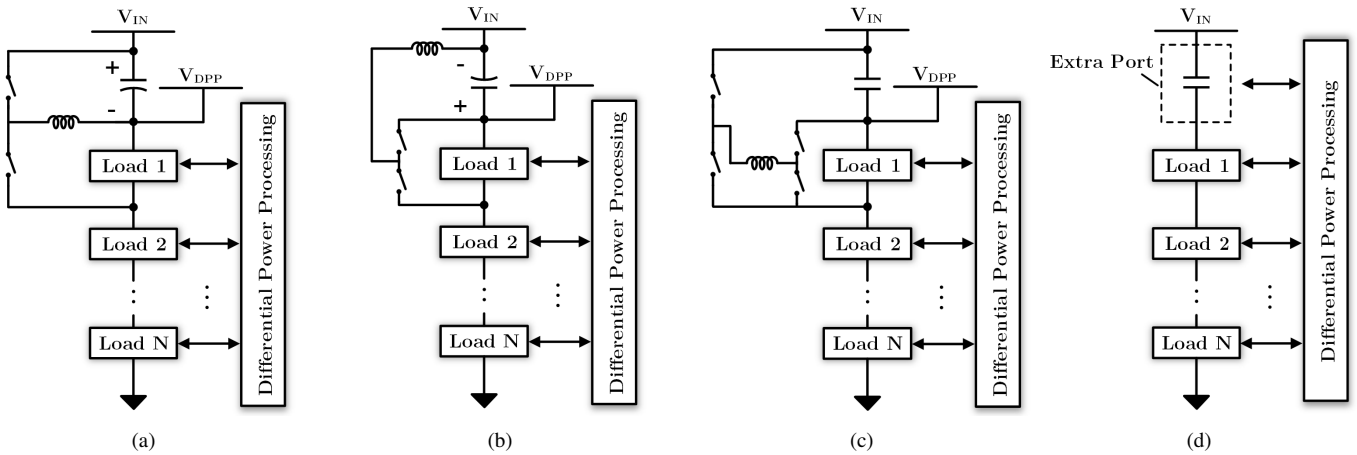

Fig. 2. A variety of topology options for the SVC: (a) buck-derived; (b) boost-derived; (c) buck-boost-derived; (d) extra DPP port. The output side of the SVC is connected to the first voltage domain as an example. It can be connected to lower voltage domains to obtain a wider regulation range if needed.

TABLE I
COMPARISON OF A FEW SVC TOPOLOGIES (N: # OF DPP STACK; K: SVC-TIED VOLTAGE DOMAIN; M_V: VOLTAGE REGULATION RATIO)

SVC Topology	Normalized SVC Power (ρ_{SVC})	Normalized Additional DPP Power (ρ_{DPP})	$\rho_{SVC}+\rho_{DPP}$
Buck-derived	$1-\frac{N-K}{N}\cdot\frac{1}{M_V}, (M_V>1)$	$\frac{N-K}{N}\cdot\left(1-\frac{1}{M_V}\right)$	$\frac{2N-K}{N}-\frac{2N-2K}{N}\cdot\frac{1}{M_V}$
Boost-derived	$1-\frac{N-K}{N}\cdot\frac{1}{M_V}, \left(\frac{N-K}{N}<M_V<1\right)$	$\frac{N-K}{N}\cdot\left(\frac{1}{M_V}-1\right)$	$\frac{K}{N}$
Buck-Boost-derived	$1-\frac{N-K}{N}\cdot\frac{1}{M_V}, \left(\frac{N-K}{N}<M_V\right)$	$\frac{N-K}{N}\cdot\left\|1-\frac{1}{M_V}\right\|$	$1-\frac{N-K}{N}\cdot\left(\frac{1}{M_V}-\left\|1-\frac{1}{M_V}\right\|\right)$
Extra-Port	N/A	$\left\|1-\frac{1}{M_V}\right\|$	$\left\|1-\frac{1}{M_V}\right\|$

The remainder of this paper is structured as follows: Section II introduces the working principle of the SVC and compares a few different SVC implementations. Section III presents the buck-derived SVC together with the MAC-DPP converter in detail, designs the power rating of both converters, and develops a decoupled control strategy validated in transient simulations. Experimental results are provided in Section IV, including voltage regulation waveforms and efficiency measurements. Finally, Section V concludes this paper.

II. PRINCIPLES OF THE SERIES VOLTAGE COMPENSATOR

The series-connected SVC can be modeled as a controllable voltage source as shown in Fig. 1. The stacked DPP load voltage can be precisely regulated by controlling the SVC to compensate for the difference between the input dc bus voltage and the desired DPP load voltage. Compared to a cascaded standalone dc-dc converter, the benefits of SVC comes from partial power processing [7]–[13]. The current ratings of the SVC and the DPP system are the same (because they are connected in series). The voltage rating of the SVC is only a portion of the overall input voltage. The SVC only processes a fraction of the full load power. As a result, the SVC has a much lower power rating and significantly reduced power loss and component size compared to a standalone dc-dc converter.

Fig. 2 shows a few different ways of implementing the SVC. The SVC can be either implemented separately as a dc-dc converter (Fig. 2a∼2c), or merged into the DPP converter as one extra port (Fig. 2d). Fig. 2a shows a buck-derived SVC that applies to the circumstances where the input voltage is higher than the DPP load voltage. In the case when the input voltage is lower, the SVC can be designed as a boost converter as shown in Fig. 2b. The buck-derived SVC and boost-derived SVC have very low component count. However, they only regulate the input voltage towards one direction (either up or down). Fig. 2c is a buck-boost-derived SVC that regulates the input voltage in both directions. It requires more components and more sophisticated control, but it offers a wider regulation range. Fig. 2d shows an SVC topology implemented as an extra port of the DPP converter. The input current of the extra port is bypassed through the DPP converter. It can either step up or step down the input voltage depending on the designed polarity of the extra port. The voltage control of the extra port can be merged with the master controller of the DPP converter.

A. Normalized SVC Power

The performance of a standalone SVC topology (Fig. 2a∼2c) can be evaluated based on the normalized SVC input power, which is defined as:

$$\rho_{SVC}=\frac{\text{SVC Input Power}, P_{SVC}}{\text{Total Input Power}, P_{IN}}. \tag{1}$$

A lower normalized power ρ_{SVC} indicates less power processed by the SVC regulator. Fig. 3 shows the detailed analysis

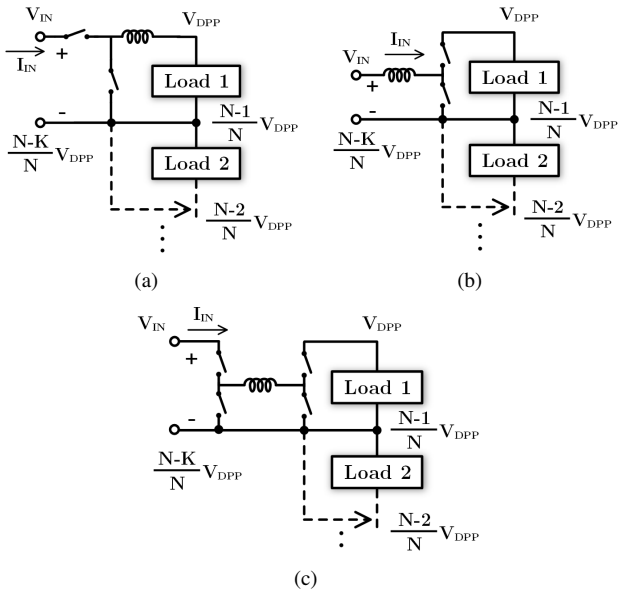

Fig. 3. Voltage and current rating analysis of the SVC implemented as: (a) buck-derived; (b) boost-derived; (c) buck-boost-derived topologies.

of the voltage and current rating of the buck-derived, boost-derived and buck-boost-derived SVC, respectively. To simplify the analysis, the SVC topologies in Fig. 3 only interfaces with the first voltage domain of the DPP system. The SVC can be connected to lower voltage domains depending on the required voltage regulation range. In these SVC topologies, the input voltage is: $V_{IN} - \frac{N-K}{N} V_{DPP}$. Define M_V as the voltage regulation ratio $\frac{V_{IN}}{V_{DPP}}$, and assume the SVC is connected to the top K^{th} voltage domains of the DPP architecture. The normalized input power of the buck-derived, boost-derived and buck-boost derived SVC is:

$$\rho_{SVC} = \frac{(V_{IN} - \frac{N-K}{N} V_{DPP}) I_{IN}}{V_{IN} I_{IN}} = 1 - \frac{N-K}{N M_V}. \quad (2)$$

For a boost-derived SVC or a buck-boost-derived SVC operating in boost mode, the input voltage (V_{IN}) should be larger than the ground plane voltage of the K^{th} voltage domain, so the regulated voltage ratio is within the range, $\frac{N-K}{N} < M_V < 1$. As for the buck-derived SVC or buck-boost-derived SVC in buck mode, the regulation ratio $M_V > 1$.

Fig. 4 plots the SVC normalized power (ρ_{SVC}) as a function of the voltage regulation ratio (M_V) in DPP systems with different numbers of voltage domains (N). As N increases, ρ_{SVC} decreases, so an SVC offers more advantages in a DPP system with a higher number of stacked voltage domains. In the buck region ($M_V > 1$), as the regulated voltage ratio increases, more partial power goes through the SVC, but it is always less than the total input power as indicated in Eq (2). In the boost region ($M_V < 1$), less power goes through the SVC as the input voltage decreases (i.e. the voltage gap becomes larger). However, the input voltage in the boost region needs to be larger than $\frac{N-K}{N} V_{DPP}$ if the SVC was connected to the top K^{th} voltage domain. If the input voltage further decreases, the SVC needs to be connected to the ground plane of a lower

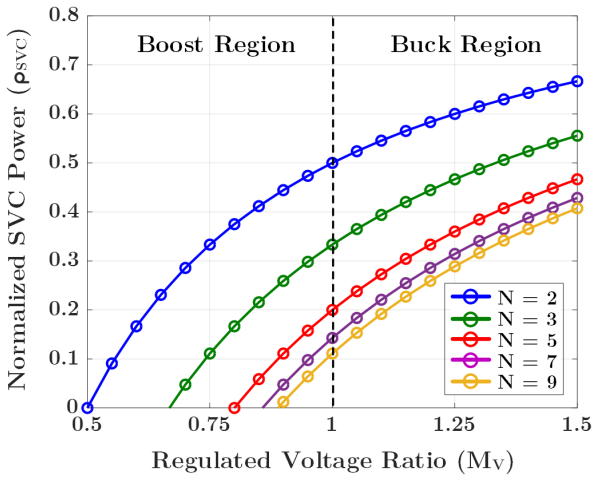

Fig. 4. ρ_{SVC} as a function of M_V in DPP systems of different number of series-stacked voltage domains (assume K = 1).

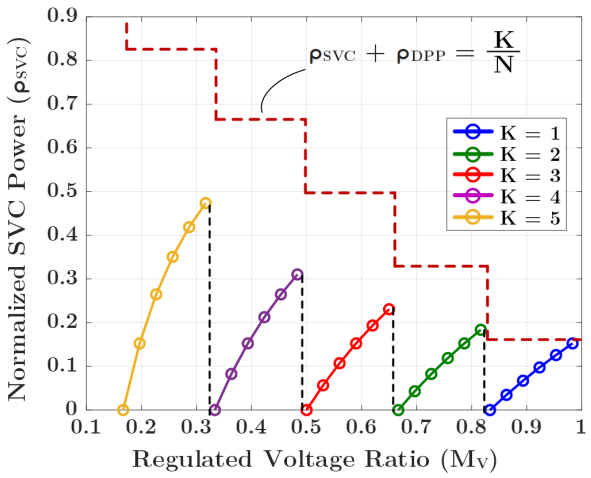

Fig. 5. ρ_{SVC} as a function of M_V when the SVC is connected to different voltage domains (assume N = 6). The normalized SVC power is lower if K is smaller. For each K selected, ρ_{SVC} is plotted in its optimum regulation range: $\frac{N-K}{N} < M_V < \frac{N-K+1}{N}$.

voltage domain, leading to higher power going through SVC as shown in Fig. 5.

B. Normalized Additional Differential Power

When the SVC is implemented as an extra port, the input current from the dc bus needs to be processed by the DPP converter, leading to additional power loss in the DPP converter. The bypassed power at the extra port is the additional differential power that the DPP converter needs to process due to the voltage regulation. Define the normalized additional differential power as:

$$\rho_{DPP} = \frac{\text{Additional Differential Power}, \Delta P_{DPP}}{\text{Total Input Power}, P_{IN}}. \quad (3)$$

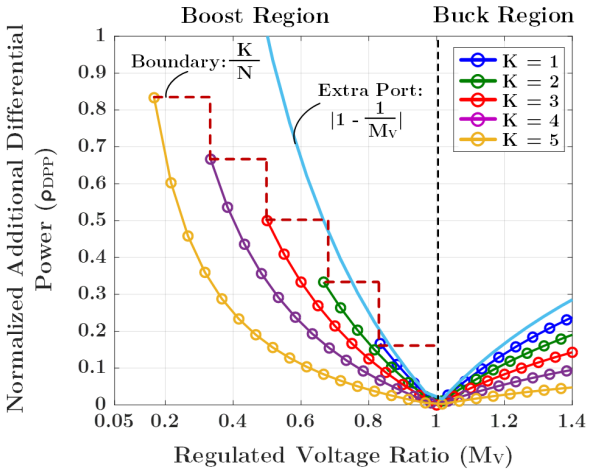

Fig. 6. ρ_{DPP} as a function of M_V if the SVC is connected to different voltage domains of the DPP system. (N = 6).

The normalized additional differential power of the extra-port SVC is:

$$\rho_{DPP} = \frac{|V_{IN} - V_{DPP}| \times I_{IN}}{V_{IN} I_{IN}} = \left|1 - \frac{1}{M_V}\right|, \quad (4)$$

which is irrelevant to the number of DPP stacks.

The buck-derived, boost-derived, and buck-boost-derived SVC also increase the power that the DPP converter has to process. Assuming that the load power across all voltage domains are uniform in the DPP system, if the SVC (in Fig. 2a∼2c) works in the buck region, the partial power delivered by the SVC to the top K voltage domains is larger than the average load power of the K voltage domains (i.e. $P_{SVC} > \frac{K}{N} P_{IN}$). The DPP converter delivers the power difference ($P_{SVC} - \frac{K}{N} P_{IN}$) from the top K voltage domains to the the other $N - K$ voltage domains. The normalized increased differential power of DPP converter is:

$$\rho_{DPP} = \frac{P_{SVC} - \frac{K}{N} P_{IN}}{P_{IN}} = \frac{N-K}{N}\left(1 - \frac{1}{M_V}\right). \quad (5)$$

When SVC is working in the boost region, on the contrary, the partial power delivered to the top K voltage domains is less than the average load power of K voltage domains. Therefore, the DPP converter will deliver the power difference from the lower $N - K$ voltage domains to the top K voltage domains, and the normalized increased differential power is:

$$\rho_{DPP} = \frac{\frac{K}{N} P_{IN} - P_{SVC}}{P_{IN}} = \frac{N-K}{N}\left(\frac{1}{M_V} - 1\right). \quad (6)$$

Fig. 6 illustrates the relationship between the increased differential power and regulated voltage ratio when different numbers of voltage domains are connected to SVC. The ρ_{DPP} of the extra-port SVC is plotted in solid line, while the ρ_{DPP} of other SVC implementations (in Fig. 2a∼2c) are plotted in circled line. As the voltage difference increases (i.e. M_V increases if it is larger than one, or decreases if it is smaller than one), more additional differential power needs to be processed. When the partial power of SVC is delivered to more voltage domains (i.e., if K increases), less power difference exist among the DPP voltage domains, and the additional DPP power reduces. If the SVC converter in Fig. 2a∼2c works in boost region, for each K selected, the regulated voltage ratio is limited ($M_V > \frac{N-K}{N}$), so the normalized additional DPP power has an upper bound: $\frac{K}{N}$. Define the normalized total additional processed power for regulation purpose as $\rho_{SVC} + \rho_{DPP}$. The upper bound $\frac{K}{N}$ is also the normalized total additional power for boost-derived SVC or buck-boost-derived SVC in boost mode as shown in Fig. 5.

Table I summarizes the normalized SVC power, normalized additional differential power, and normalized total additional power of different SVC implementations. For buck-derived SVC or buck-boost derived SVC operating in buck mode, $\rho_{SVC} + \rho_{DPP}$ is larger than one when $M_V > 2$, indicating that the SVC is not more attractive than a standalone dc-dc converter if the regulation ratio is large. As for the extra-port SVC, it will lose the advantages when $M_V < \frac{1}{2}$.

III. A Buck-derived SVC for MAC-DPP Converter

To validate the effectiveness of the SVC concept and the derived the performance limits, a buck-derived SVC is designed and tested with a multiport ac-coupled DPP (MAC-DPP [6]) converter. Fig. 7 shows the detailed circuit topology of the buck-derived SVC and MAC-DPP converter. N voltage domains are stacked in series and connected to a dc voltage bus. The MAC-DPP converter balances the differential power among the DPP loads, making the dc bus voltage evenly distributed into series-stacked voltage domains. The buck-derived SVC feeds the input power to the first voltage domain with its switch node linked to the DPP dc bus through a filter inductor. By controlling the duty ratio of the buck stage, the DPP dc bus voltage can be precisely regulated. As explained in Section II, the buck-derived SVC has a reduced power rating due to the partial power processing, and it will provide advantages over standalone dc-dc converter when the regulated voltage ratio $M_V < 2$. Besides, the buck-derived SVC has the following other advantages:

- Soft Start: In a DPP architecture, multiple voltage domains are connected in series to the input side. If the input voltage has a high slew rate, small power unbalance might cause significant voltage overshoot at some of the series stacked voltage domains, leading to severe damage on the loads in that voltage domain. By adjusting the duty ratio, the buck-derived SVC can control the voltage difference between the input bus and the load, limiting the load voltage skew rate during startup and input voltage step transient.
- Fault Protection: Since the SVC is connected in series between the DPP loads and input dc bus, it can block the DPP loads from the dc bus by disabling the upper arm switches, realizing fast protection in fault conditions.

A. Power Rating Design of SVC and MAC-DPP Converter

Assume a buck-derived SVC with MAC-DPP converter is applied to a DPP system of N series-connected voltage

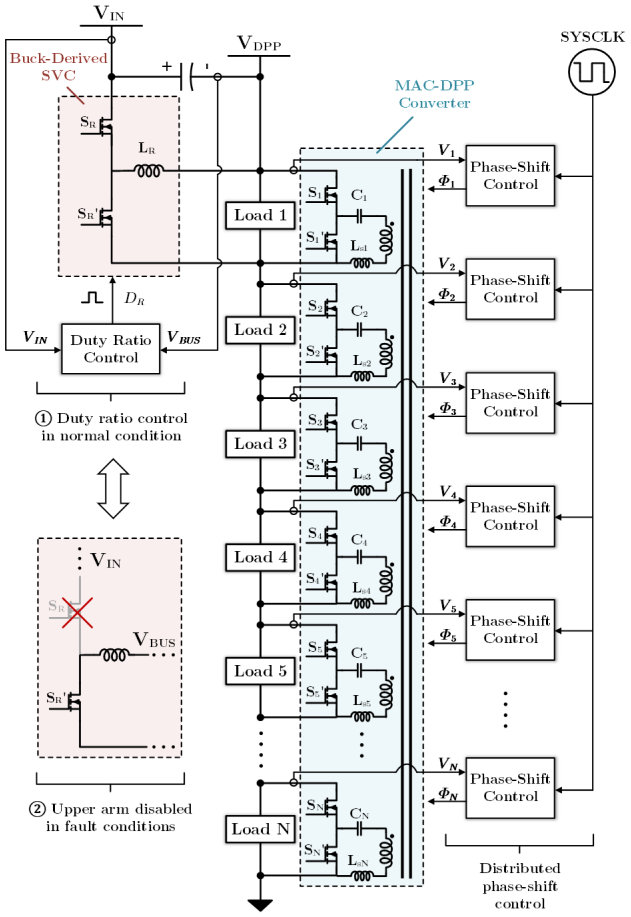

Fig. 7. Circuit topology of a buck-derived series voltage compensator for the multiport ac-coupled DPP converter.

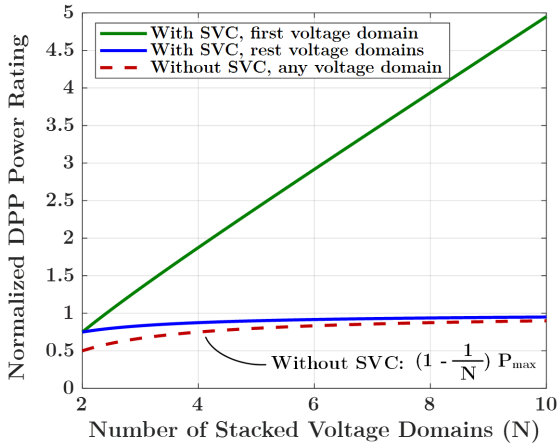

Fig. 8. Normalized differential power rating (normalized to $P_{\max}$) in different voltage domains of MAC-DPP converter with and without the SVC.

domains, and the SVC is connected to the first voltage domain. The load power ($P_{load,i}$) at each voltage domain is within the range between $[0, P_{\max}]$. To maintain the benefit, the regulated voltage ratio (M_V) of the buck-derived SVC is larger than 1 and smaller than 2. The input power of the SVC is:

$$P_{SVC} = \rho_{SVC} \cdot P_{IN} = \left(1 - \frac{N-1}{N} \cdot \frac{1}{M_V}\right) \cdot \sum_{i=1}^{N} P_{load,i} \quad (7)$$

According to Eq. (7), the maximum input power of SVC is reached when all voltage domains consume full load power ($P_{\max}$), and the input voltage is regulated from $2V_{DPP}$ to V_{DPP}. In this case, the power rating of the buck-derived SVC should be designed to be larger than $\frac{N+1}{2} P_{\max}$.

To balance the differential power in all operating points, the differential power rating of each voltage domain in an N-port MAC-DPP converter should be designed for the worst case with the largest differential power. In the first voltage domain, the differential power processed by the MAC-DPP is:

$$P_{DPP,1} = P_{SVC} - P_{load,1} = \rho_{SVC} \cdot \sum_{i=1}^{N} P_{load,i} - P_{load,1}. \quad (8)$$

ρ_{SVC} is in the range of $[\frac{1}{N}, \frac{N+1}{2N}]$, so the maximum differential power of the first voltage domain is:

$$\max\{P_{DPP,1}\} = \frac{N^2-1}{2N} P_{\max} \quad (9)$$

The maximum differential power of the first voltage domain is reached when the first voltage domain consumes zero power and the rest of the voltage domains consume full load power at the voltage regulation ratio $M_V = 2$. Therefore, the power rating of the MAC-DPP converter for the first voltage domain should be designed following Eq. (9). As N increases, the system input power rating increases linearly, and the differential power rating of first voltage domain also increases linearly with a slower slew rate.

The total differential power that needs to be processed by other voltage domains is:

$$\begin{aligned} P_{DPP,k(k\geq 2)} &= \frac{P_{IN} - P_{SVC}}{N-1} - P_{load,k} \\ &= \frac{1-\rho_{SVC}}{N-1} \cdot \sum_{i=1}^{N} P_{load,i} - P_{load,k} \end{aligned} \quad (10)$$

The maximum value of Eq. (10) is reached when the K^{th} voltage domain consumes full load power and other voltage domains consume zero power when $M_V = 2$:

$$\max\{P_{DPP,k(k\geq 2)}\} = \left(1 - \frac{1}{2N}\right) P_{\max} \quad (11)$$

Fig. 8 compares the differential power rating of the MAC-DPP converter for different voltage domains. Applying the SVC to the MAC-DPP system significantly increases the differential power of the first voltage domain. The differential power of other voltage domains remain roughly the same. The power rating design method presented in this section is also applicable to other SVC-DPP topologies.

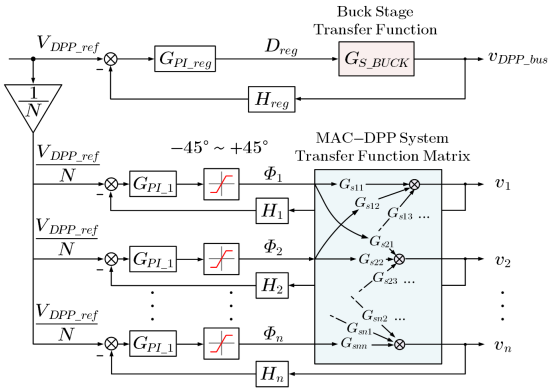

Fig. 9. An example control block diagram which enables precise DPP load voltage regulation and rapid differential power balancing.

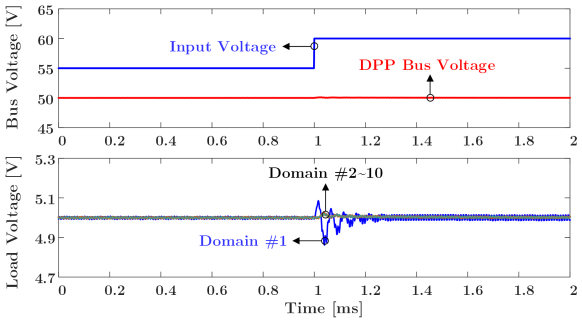

Fig. 10. Simulated transient response of an input voltage step. The input voltage steps from 55 V to 60 V.

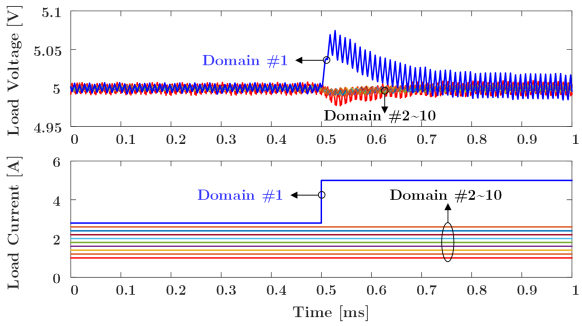

Fig. 11. Simulated transient response of a step load change at domain #1. The load current of domain #1 steps from 2.8 A to 5 A.

B. Control Strategy and Simulation Results

Fig. 9 shows one way of implementing the closed-loop control for the buck-derived SVC. The DPP load bus voltage ($V_{\text{DPP\_BUS}}$) is regulated by controlling the duty ratio (D_{SVC}) of the buck stage. The steady state duty ratio of the SVC switch is a function of V_{IN}, $V_{\text{DPP\_BUS}}$, and N:

$$D_{\text{SVC}} = \frac{V_{\text{DPP\_BUS}}}{NV_{\text{IN}} - (N-1)V_{\text{DPP\_BUS}}}. \tag{12}$$

As the duty ratio increases, the DPP bus voltage monotonically increases, so a simple PI-loop can regulate the dc bus voltage. A distributed phase-shift control strategy is utilized to control the closely-coupled power flow of the MAC-DPP system [6]. A fully distributed modular feedback loop is

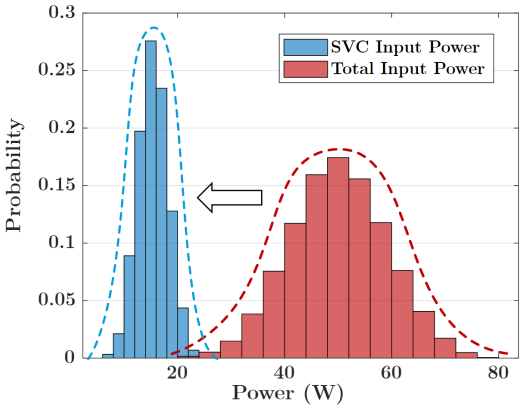

Fig. 12. Distribution histogram of the SVC input power and total input power.

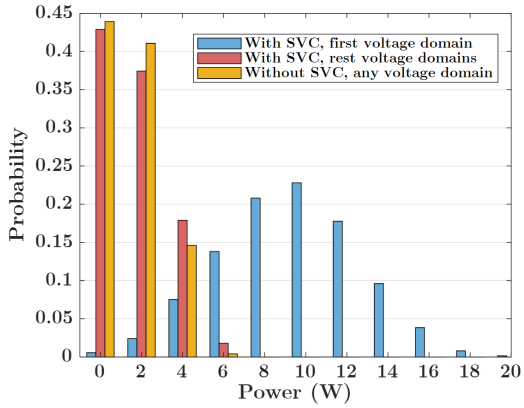

Fig. 13. Probabilistic histogram of processed differential power in different voltage domains with and without SVC. In the case with SVC, all other voltage domains (besides the first domain) are symmetric, so the differential power distribution of the second domain is plotted as an example. Similar in the case without SVC, an arbitrary voltage domain is shown as an example.

implemented in each voltage domain to control the phase-shift based on the locally measured voltage. The reference DPP bus voltage is divided by N as the reference voltage for each voltage domain. As shown in Fig. 7, the distributed phase-shift control can be implemented as multiple individual phase-shift modules synchronized to a clock signal. Both the control and power circuit can be extended to very-large-scale DPP systems comprising hundreds of voltage domains in series [14].

A SPICE simulation platform is built to validate the control strategy of the buck-derived SVC. Here, ten series-stacked voltage domains are supported by a 10-port MAC-DPP converter, and each voltage domain supports 5 V load, so the nominal stacked string voltage of the ten voltage domains is 50 V. The input dc bus provides a 55 V dc voltage, and the SVC needs to compensate for the 5 V difference between the input dc bus and the nominal DPP load voltage. Fig. 10 and Fig. 11 shows the transient response of an input voltage step change and a load current step change, respectively. The voltage of the first domain had larger overshoot and longer settling time than other domains due to the additional partial

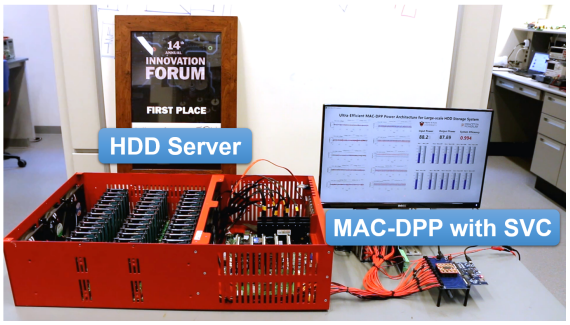

Fig. 14. A picture of the HDD testbench powered by MAC-DPP converter with the SVC voltage pre-regulator.

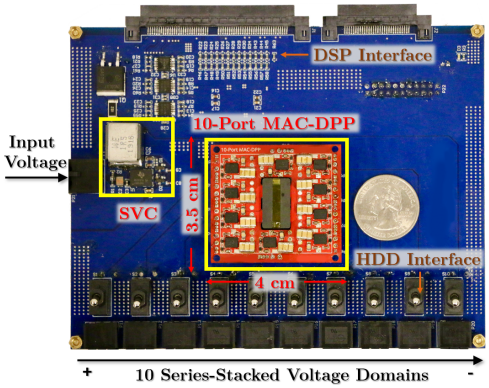

Fig. 15. A picture of the prototype 10-port MAC-DPP converter with a miniaturized SVC and a US quarter. The operation range of the SVC is between 50 V and 85 V.

TABLE II
BILL-OF-MATERIAL OF THE PROTOTYPE

Device & Symbol	Component Description
SVC Half-Bridge Switch, S_R	DrMOS, LMG5200MOFT
SVC Series Inductor, L_R	WE-HCM Shielded, 1.5μH
SVC Switching Frequency, f_{sw}	500 kHz
MAC Half-Bridge Switch, $S_1 \sim S_{10}$	DrMOS, CSD95377Q4M
MAC Blocking Capacitor, $C_1 \sim C_{10}$	Murata X5R, 100 μF $\times$ 3
MAC Series Inductor, $L_{s1} \sim L_{s10}$	Coilcraft SLC7649, 100 nH
MAC Switching Frequency, f_{sw}	100 kHz

power that SVC delivered to this domain. The maximum voltage overshoot in all voltage domains is less than 2%.

A Monte Carlo simulation with 10,000 iterations was also performed on the 10-stacked DPP system. In the simulation, the SVC regulated the 65 V input bus voltage into 50 V DPP stacked-load voltage. The load power of each voltage domain is uniformly distributed between 0∼10 W. At each iteration, the total input power, SVC input power, and the differential power processed at each voltage domain are recorded, and their probability distributions are plotted in Fig. 12 and 13. As shown in Fig. 12, the input power of SVC is much less than the total input power. In tradition solutions, the total input power will be processed by a standalone pre-regulator. The SVC can significantly reduce the power conversion stress by pushing the power distribution curve leftwards. Fig. 12 plots the probabilistic distribution of the differential power at each voltage domain in the case with and without the SVC regulator.

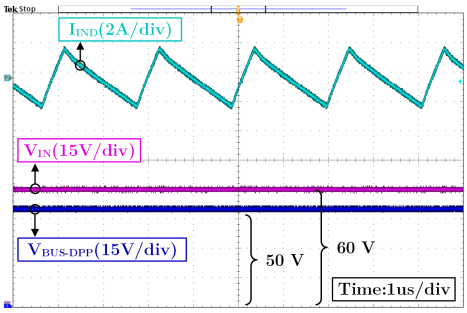

Fig. 16. Measured waveforms of SVC inductor current, input dc bus voltage, and the regulated voltage for DPP system.

As expected, the differential power at the first voltage domain is higher, because the partial power is directly delivered to the first voltage domain by the SVC. However, the differential power of the other voltage domains is close to the case without SVC and is close to zero.

IV. Experimental Results

To experimentally verify the performance of the SVC converter, a buck-derived SVC was designed and attached to a 450 W 10-port MAC-DPP converter. Table II listed their component values. Fig. 14 shows the complete setup of the testbench, where the MAC-DPP converter is powering a 50-HDD storage server. The SVC is utilized to regulate the input dc bus voltage ranging from 50 V∼85 V into 50 V for the MAC-DPP converter. The 50 V DPP system dc bus voltage is split into ten series-stacked voltage domains with each voltage domain supporting five 5 V 2.5-inch HDDs. Fig. 15 shows a picture of the buck-derived SVC and a MAC-DPP converter. Based on the input voltage range and Eq. (2), the SVC only processes 10% $\sim$ 50% of the overall load power, and the physical size of the SVC is less than 1/4 of the MAC-DPP converter. Fig. 16 shows the measured waveforms of the buck-stage inductor current, the input dc bus voltage, and the DPP load voltage bus. The SVC effectively compensated for the difference between the input voltage and the DPP load voltage, converting 60 V into 50 V for the DPP system.

The MAC-DPP converter also needs to process differential power caused by unbalanced load power. In the experiment, in order to eliminate the influence of the unbalanced load power and focus on how much power loss is generated due to the voltage regulation, the load power of each voltage domain was kept the same. The total system efficiency is calculated as total load power divided by input power. Fig. 17 plots the measured system efficiency, SVC converter efficiency, and MAC-DPP converter efficiency when SVC converting 55 V dc bus into 50 V DPP load voltage. In this case, the MAC-DPP converter is delivering the increased differential power from the first voltage domain to the other nine voltage domains. The input power of the SVC converter and the total differential power of the MAC-DPP converter is labeled aside, which are only a small portion of the total load power. The converter efficiency of the SVC and the 1-port-to-9-port DPP converter efficiency is around 95%. The efficiency of the full MAC-DPP system is

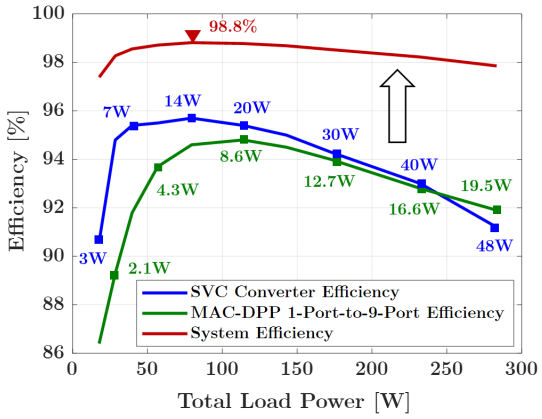

Fig. 17. Measured SVC conversion efficiency, MAC-DPP 1-port-to-9-port efficiency (as defined in [6]) and the system efficiency when SVC converted 55 V input dc bus voltage into 50 V DPP string voltage. The input power of SVC and MAC-DPP processed differential power is labeled on the curves.

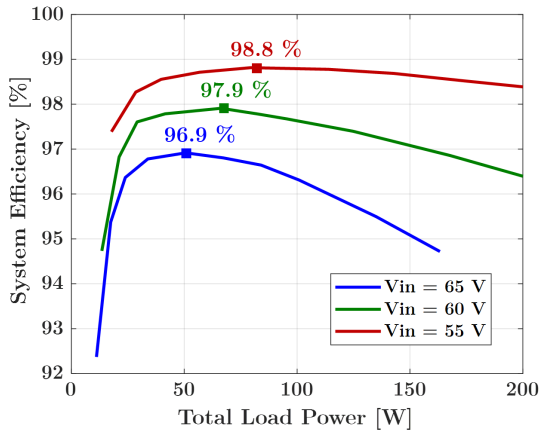

Fig. 18. Measured system efficiency when converting input dc bus voltage from 55 V, 60 V, 65 V into 50 V for DPP system. The peak system efficiency is 98.8%, 97.9%, and 96.9%, respectively.

significantly higher, reaching 98.8% peak efficiency at 80 W load power (defined as the total power consumed by the load divided by the total power sourced from the input). Fig. 18 plots the system efficiency of different input voltages. As the input voltage increases, the power processed by the SVC and MAC-DPP also increase, and the system efficiency drops.

In summary, the SVC leverages the partial power processing concept and only process the differential voltage between the input voltage bus and the needed DPP string voltage. The DPP system only processes the differential power among the series stacked voltage domains and inherits natural voltage step-down. The combination of the SVC-DPP architecture optimize the power flow and enables ultra high system efficiency and power density for large scale modular energy systems.

V. Conclusions

This paper presents the principles of the series voltage compensator for differential power processing. Compared to a standalone dc-dc converter, the SVC only processes a small fraction of the total load power. The size of the SVC is very small, and the power loss in voltage conversion is significantly reduced. A theoretical framework is developed to analyze the impact of many design factors on the performance of the SVC. A few different SVC topologies are compared and their performance limits are quantified. A buck-derived SVC converter is designed and applied to a 10-port MAC-DPP converter targeting ultra-efficient data center power delivery. In addition to improved efficiency and reduced size, the SVC also enables soft-start and fault protection of the DPP system. The theoretical analysis is verified by Monte Carlo simulations. Experimental results show that the SVC can effectively regulate the DPP bus voltage with very high system efficiency.

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