Performance Limits of Differential Power Processing

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Abstract: This paper investigates the performance limits of differential power processing (DPP) and presents quantitative and systematic design guidelines for the selection and comparison of DPP topologies. A stochastic model is developed to evaluate the expected power losses of a variety of DPP topologies with probabilistic load distribution. The expected losses of several DPP topologies are derived and compared against traditional dc-dc converters to reveal their performance limits. The impacts of the load distribution and load scale on the expected losses are investigated. The theoretical models are verified with SPICE simulations and experimental results.

1 Introduction

Differential power processing (DPP) has been proved effective in many applications including solar photovoltaics, battery management systems, and computers on server racks (Fig. 1) [1–4, 6]. DPP converters only process the differential power and can greatly reduce the power conversion stress and losses. Various DPP topologies have been explored, with tradeoffs in efficiency, size, cost, and control complexity. Empirical work has been done to compare DPP topologies with traditional dc-dc topologies using numerical and SPICE simulations [2]. An analytical model providing generalized design guidelines for DPP topologies under a set of rigorous assumptions is needed and is the main focus of this paper.

This paper systematically investigates the performance



Fig. 1: A $N \times M$ differential power processing system with N series-stacked voltage domains, each comprising M modular loads. The modular load units can be battery cells, PV panels, or hard disk drives (HDD).

limits of differential power processing. A performance scaling factor, $S(\bullet)$, is introduced to describe how the performance of a DPP converter changes as the system size scales up. The model has a minimum set of assumptions, offers rich design insights, and is verified with SPICE simulations and experimental results. Extended theoretical derivations, modeling details, and experimental results will be provided in the full paper.

2 Stochastic Loss Model and Scaling Factor of DPP Topologies

Fig. 2 shows several example DPP topologies classified into two categories: 1) fully-coupled DPP, where there is a direct power flow path between two arbitrary voltage domains; and 2) ladder DPP, where the power is processed by numerous standalone dc-dc converters. Fig. 2a~2b are fully-coupled DPP topologies, and Fig. 2c~2d are ladder DPP topologies. Similar analysis will be extended to other DPP topologies in the final paper. DPP solutions are typically applied to systems with stochastic loads. We develop a generalized analysis framework for DPP systems with series-stacked voltage domains and stochastic loads, and compare their performance against an N:1 converter.

The DPP system in Fig. 1 has N series-stacked voltage domains, each comprising M loads connected in parallel. The voltage of each voltage domain is V_0 . Assume that the instantaneous power of the j^{th} load in the i^{th} voltage



Fig. 2: Example DPP topologies: (a) ac fully-coupled DPP [3]; (b) dc fully-coupled DPP [4]; (c) ladder DPP with dual-active-bridge cells [5]; (d) ladder DPP with buck-boost cells [6]. There are many different ways of implementing these topologies.



Fig. 3: Simplified models of DPP topologies with the converter modeled as an ideal transformer and an output resistance: (a) ac fully-coupled DPP; (b) dc fully-coupled DPP; (c) ladder DPP with dual-active-bridge cells; (d) ladder DPP with buck-boost cells.

domain is $P_{ij}(t)$. All $P_{ij}(t)$'s are *independent and identically distributed* (i.i.d) random variables. The total power consumed by the i^{th} voltage domain is the summation of the M random variables: $P_i(t) = P_{i1}(t) + P_{i2}(t) + ... + P_{iM}(t)$. A DPP converter manipulates the power flow and balances the series-stacked voltage domains. The instantaneous differential power of the i^{th} voltage domain is the difference between its power and the average power of all domains:

$$\Delta P_i(t) = \frac{P_1(t) + P_2(t) + \dots + P_N(t)}{N} - P_i(t) = \overline{P}(t) - P_i(t).$$
(1)

 $\Delta P_i(t)$ is the minimum power to be processed by the DPP converter. The conduction loss of the DPP converter is directly related to $\Delta P_i(t)$. Here we derive the conduction loss of example DPP topologies as a function of $\Delta P_i(t)$. • Fully-Coupled DPP Converter: A fully-coupled DPP topology can be modeled as an *N*-port network with all ports connected to an *N*-winding ideal transformer of uniform turns ratio as shown in Fig. 3a (which is functionally equivalent to Fig. 3b). The conduction loss of the DPP converter is captured by an output resistance R_{out} as labeled in Fig. 3, which is assumed to be identical for all ports. In a fully-coupled DPP converter, the i^{th} port is processing a differential power of $\Delta P_i(t)$, and the total conduction loss of the full *N*-port DPP system is:

$$P_{loss}(t) = R_{out} \sum_{i=1}^{N} \Delta I_i(t)^2 = R_{out} \sum_{i=1}^{N} \left(\frac{\Delta P_i(t)}{V_0}\right)^2 = \frac{R_{out}}{V_0^2} \sum_{i=1}^{N} \left(P_i(t) - \overline{P}(t)\right)^2.$$
(2)

 $P_{loss}(t)$ reflects the variance of an independently repeated sampling experiment of the random variable $P_i(t)$. Its

statistical expectation, the average power loss of the DPP system over a long enough period, is:

$$\mathbb{E}[P_{loss}(t)] = \frac{R_{out}}{V_0^2} \times \mathbb{E}\left[\sum_{i=1}^n (P_i(t) - \overline{P}(t))^2\right] = M(N-1)\frac{R_{out}}{V_0^2}\sigma^2(P_{ij}(t)) \Rightarrow \underbrace{\mathcal{S}(MN\sigma^2)}_{scaling \ factor},\tag{3}$$

where $\sigma^2(P_{ij}(t))$ is the variance of P_{ij} . We use the symbol $\mathcal{S}(\bullet)$ to represent the performance scaling factor of a DPP system, which illustrates the growth rate of the loss as the dimension of the DPP system increases. Eq. (3) indicates that the performance scaling factor of an $M \times N$ fully-coupled DPP system is $\mathcal{S}(MN\sigma^2)$. The expected loss of a fully-coupled DPP converter is only determined by the variance of each individual stochastic load, and scales linearly with M and N. The expected loss is independent from the total load power of the system.

• Ladder DPP Converter: In a ladder DPP topology, each DPP unit is a dc-dc converter as shown in Fig. 2c (equivalent as Fig. 3c). Power needs to go through multiple dc-dc converters from one domain to another domain. The differential power that the i^{th} DPP unit needs to process between the i^{th} and the $(i + 1)^{th}$ voltage domains is $\Delta P_{i\leftrightarrow i+1}(t) = \sum_{k=1}^{i} (\overline{P}(t) - P_k(t)) = i \times \overline{P}(t) - \sum_{k=1}^{i} P_k(t)$, and the total conduction loss is:

$$P_{loss}(t) = R_{out} \sum_{i=1}^{n-1} \Delta I_{i \leftrightarrow i+1}^2 = R_{out} \sum_{i=1}^{n-1} \left(\frac{\Delta P_{i \leftrightarrow i+1}(t)}{V_0} \right)^2 = \frac{R_{out}}{V_0^2} \sum_{i=1}^{n-1} \left(i \times \overline{P}(t) - \sum_{k=1}^i P_k(t) \right)^2.$$
(4)

Its expectation, the average power loss of the DPP system over a long enough period, is:

$$\mathbb{E}[P_{loss}(t)] = \frac{R_{out}}{V_0^2} \times \mathbb{E}\left[\sum_{i=1}^{n-1} \left(i \times \overline{P}(t) - \sum_{k=1}^i P_k(t)\right)^2\right] = \frac{M(N-1)(N+1)}{6} \frac{R_{out}}{V_0^2} \sigma^2(P_{ij}(t)) \Rightarrow \underbrace{\mathcal{S}(MN^2\sigma^2)}_{scaling \ factor}.$$
 (5)

The conduction loss of an ladder DPP increases linearly as M increases, and increases quadratically as N increases, so the performance scaling factor of a ladder DPP system with $M \times N$ stochastic load array is $S(MN^2\sigma^2)$. The expected loss of a ladder DPP topology is only determined by the variance of each individual load. It scales linearly with M, and scales quadratically with N, and is independent from the total load power of the system.

• Conventional N:1 Dc-Dc Converter: In a conventional N:1 dc-dc converter, the full power of the $M \times N$ load array needs to be processed by the dc-dc converter. Assuming the output resistance of a conventional N:1 dc-dc converter is R_{out} , the conduction loss of this converter when processing power for $M \times N$ i.i.d. loads is:

$$\mathbb{E}[P_{loss}(t)] = \frac{R_{out}}{V_0^2} \times \mathbb{E}\left[\left(\sum_{i=1}^n P_i(t)\right)^2\right] = \left(MN\sigma^2(P_{ij}(t)) + M^2N^2\mu^2(P_{ij}(t))\right) \times \frac{R_{out}}{V_0^2} \Rightarrow \underbrace{\mathcal{S}(M^2N^2\mu^2)}_{scaling \ factor}, \tag{6}$$

where the $\mu(P_{ij}(t))$ is the average power of each unit. The expected loss of a N:1 dc-dc converter is determined by the square of the total output power and the variance of each load, and scales quadratically with M and N.

Eq. (3) and (5) reveal that the average power loss of DPP architectures is independent from the average power μ but only determined by the variance σ , validating the fundamental benefit of DPP solutions: a DPP converter only needs to process the differential power. If the load power is uniform without variation, a DPP system is lossless.

	Topology	Output Resistance	Expected Loss	Scaling Factor
Fully-Coupled DPP	Ac-Coupled	$\frac{8N}{G_{SW}} + \frac{4N}{G_M}$	$M(N-1)\sigma^2(P_{\rm ex}(t)) \times \frac{R_{out}}{2}$	$S(MN\sigma^2)$
	Dc-Coupled	$\frac{32N}{G_{SW}} + \frac{16N}{G_M}$	V_0^2	8(11110)
Ladder DPP	DAB-cell	$\frac{32N - 32}{G_{SW}} + \frac{16N - 16}{G_M}$	$\frac{M(N-1)(N+1)}{6}\sigma^2(P_{ij}(t)) \times \frac{R_{out}}{V_0^2}$	$\mathcal{S}(MN^2\sigma^2)$
	Buck-Boost-cell	$\frac{8N-8}{G_{SW}} + \frac{4N-4}{G_M}$	$\frac{2M(N-1)(N+1)}{3}\sigma^2(P_{ij}(t)) \times \frac{R_{out}}{V_0^2}$	
N:1 Converter	DAB	$\frac{32}{G_{SW}} + \frac{16}{G_M}$	$\left(MN\sigma^2(P_{ij}(t)) + M^2N^2\mu^2(P_{ij}(t))\right) \times \frac{R_{out}}{V_0^2}\right)$	$\mathcal{S}(M^2 N^2 \mu^2)$

3 Performance Limits, SPICE Verification, and Experimental Results

We compare the performance limits of a variety of different differential power processing topologies based on the following assumptions: (a) all topologies have identical semiconductor die area represented by $\sum G_{sw}V_{sw}^2$ (G_{sw} is the switch conductance; V_{sw} is the switch voltage rating); all $\sum G_{sw}V_{sw}^2$'s are normalized to $G_{SW}V_0^2$. (b) all topologies have identical total magnetic window areas represented by $\sum G_m$ (G_m is the conductance of each winding); all $\sum G_m$'s are normalized to G_M . One way to design an optimal dc-dc converter is to equally allocate the semiconductor die area and transformer window area between input and output ports, and make the design as symmetric as possible. Following the methods in [7], we derive the output resistance of the example DPP topologies in Fig. 2, as well as the output resistance of an N:1 dual-active-bridge (DAB) dc-dc converter. The expected losses of DPP topologies and DAB converter are listed in Table 1. Detailed derivations will be provided in the full paper.

We use the ratio between the expected loss of a DPP converter and an N:1 DAB converter (namely Normalized Loss, $\frac{P_{loss,DPP}}{P_{loss,DAB}}$) as a figure-of-merit to evaluate the performance of DPP topologies. The coefficient of variance C_V of $P_{ij}(t)$ is σ/μ . The normalized loss of different DPP topologies are shown in Fig. 4. A lower normalized loss indicates lower loss or smaller volume. Monte Carlo SPICE simulations of DPP circuit models (in Fig. 3) are performed to validate the stochastic loss model. Switching losses are captured by paralleling an equivalent resistance $(1/C_{oss}f_{sw})$ at each port. The simulations are executed 10,000 times to obtain the normalized loss. The simulated normalized loss matches precisely with the calculated results from the theoretical derivation (Table 1).



Fig. 4: Calculated (curve, -) and simulated (dot, \blacksquare) normalized loss as functions of: (a) the number of series-stacked voltage domains (N); (b) the number of parallel modular loads within one voltage domain (M); (c) coefficient of variance $(C_V = \sigma/\mu)$ of the loads.

Fig. 4a and 4b show the normalized loss of different DPP topologies as N or M increases. As N increases, the normalized loss of the fully-coupled DPP topologies (blue and red) converges to an upper limit, while the normalized loss of the ladder DPP topology (green) keep increasing. This graph provides quantitative design insights for DPP architectures. For example, the normalized loss of the ac fully-coupled DPP topology will converge at $\frac{C_V^2}{4M}$ as N increases. With M = 4 and $N \ge 2$, if $C_V = 1$, the normalized loss of an ac fully-coupled DPP converter is always lower than 1/16, indicating over 16x loss reduction from a N:1 dc-dc converter. Fig. 4c shows the normalized losses of different DPP topologies as C_V changes. When C_V increases, the DPP converter needs to process more differential power, so the normalized losses of all topologies will increase, but they will all converge at an upper limit. This is because



Fig. 5: A 50-HDD storage server supported by a 10port MAC-DPP prototype with 450 W power rating and over 99.5% peak system efficiency.

the conduction loss of a N:1 converter converter when C_V is large is dominated by $MN\sigma^2$, scaling at the same rate as that of DPP converters. The mismatch at lower C_V range is caused by the switching loss which is not captured by the stochastic model. Fig. 4 reveals that the ac-coupled DPP is the most efficient among all selected DPP topologies. Fig. 5 shows the picture of a 10-port Multiport-Ac-Coupled DPP (MAC-DPP) converter powering a 10×5 hard-disk-drive (HDD) server. A LabVIEW platform was built to monitor the system efficiency in real time. The 450 W MAC-DPP system reached a peak efficiency of 99.5% with >630 W/in³ power density. Extended experimental results of the storage server with stochastic loads will be presented in the final paper.

4 Conclusions

This paper reveals the performance limits of differential power processing (DPP). A stochastic model is developed to evaluate the performance limits of DPP topologies as the dimension (M, N), expectation (μ) and variance (σ) of modular load array scales up. The performance limits of many DPP topologies are derived and compared, providing useful design guidelines for implementing DPP systems. The analytical framework is verified by SPICE simulations. Extended theoretical derivations and experimental results will be presented in the final paper.

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