



A 99.4% Efficient 450 W Hard Disk Drive Storage Server with Multiport Ac-Coupled Differential Power Processing (MAC-DPP) Architecture


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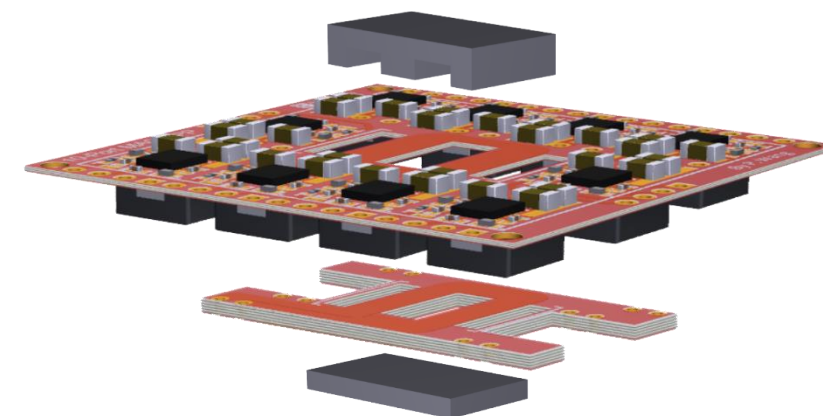
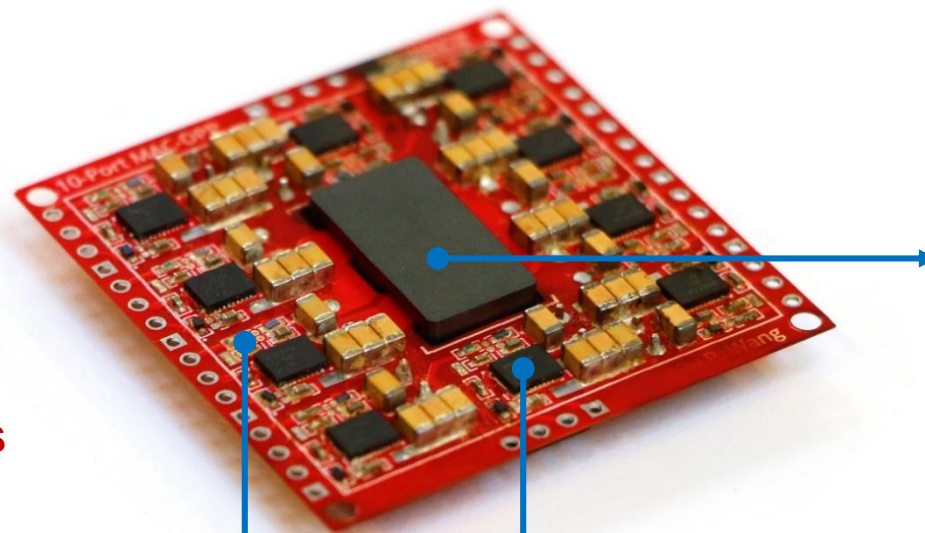
ECCE Student Project Demonstration Video Display

- Power rating: > 450 W
- Power density: > 630 W/in³
- System efficiency: > 99%
- Hot-swapping capability

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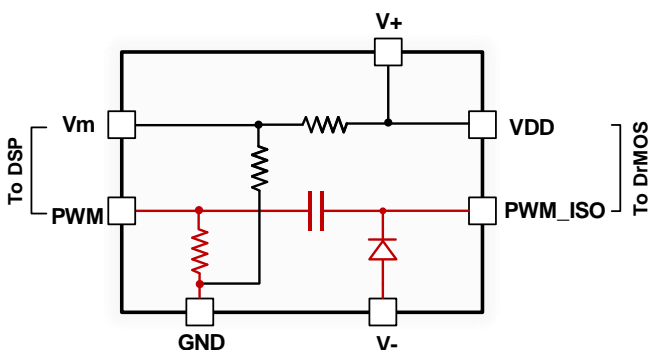
Stacked-PCB Planar Magnetics

- 10x magnetics core area reduction



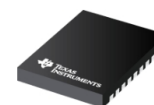
Modular Voltage Sampling & Bootstrap Gate Drive Circuits

- Modular & Scalable



DrMOS, TI-CSD95377Q4M

- 3.5 mm x 4.5 mm
- 35 A max continuous current



Data Center Energy Consumption

Data Center Industry



CO₂
kWh

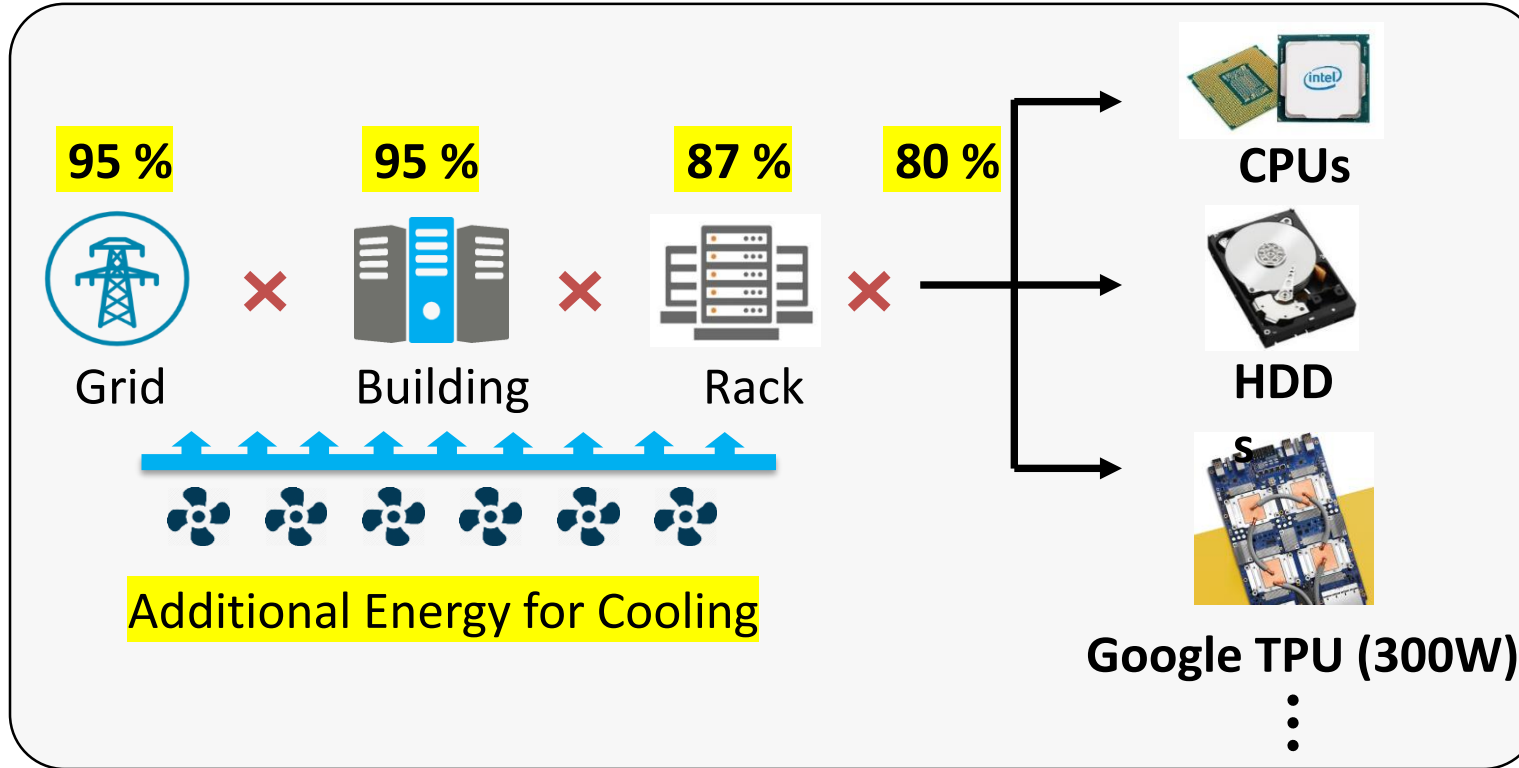
Airline Industry



- Consuming 90 billion kilowatt-hours per year in the U.S.^[1]
- Contributing 2% of the U.S. total electricity consumption (3% in worldwide)
- Comparable CO₂ emission as the entire airline industry

Power Delivery Architecture in Data Center

➤ Conventional Power Delivery Architecture^[2]



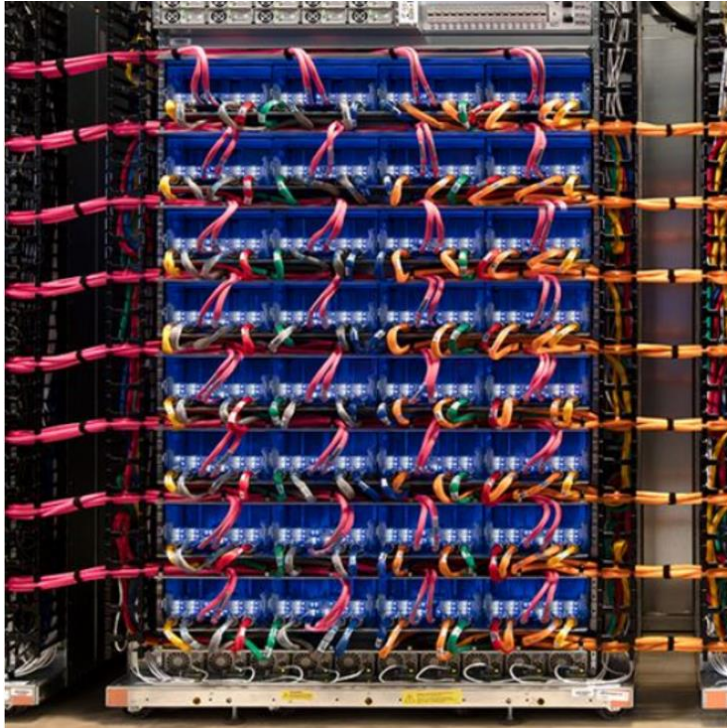
- Low grid to load efficiency:
≈ 60% $\xrightarrow{40\%}$ **HEAT**
- Emerging AI Applications
 - ➔ Higher current
 - ➔ Higher distribution losses

➤ Target for Advanced Power Architecture:

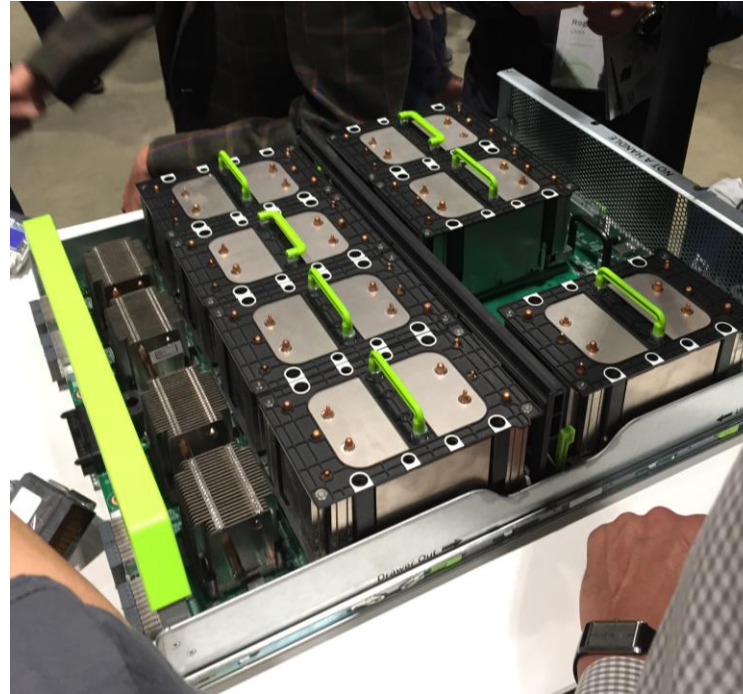
- Deliver power with less conversion stages
- Improve conversion efficiency at each stage

Large-Scale Modular Loads on Rack

- Google TPU Training Pod



- Facebook AI Accelerator



- Hard Drive Disk Array

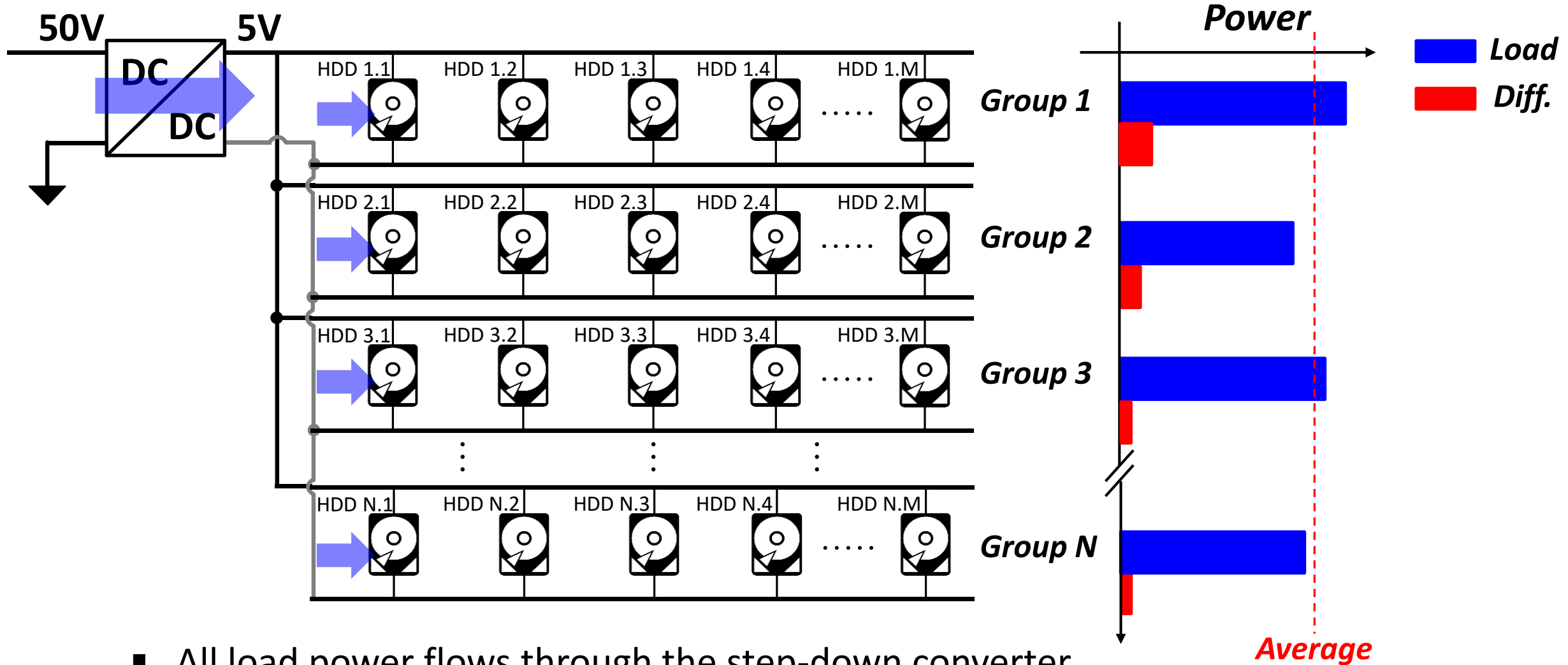


Fig. 3: Examples of Large-Scale Modular Loads in Contemporary Data Center

- Large-scale identical modules for intensive computing/storage applications
- Perform identical task with similar power consumption

Differential Power Processing for HDD Array

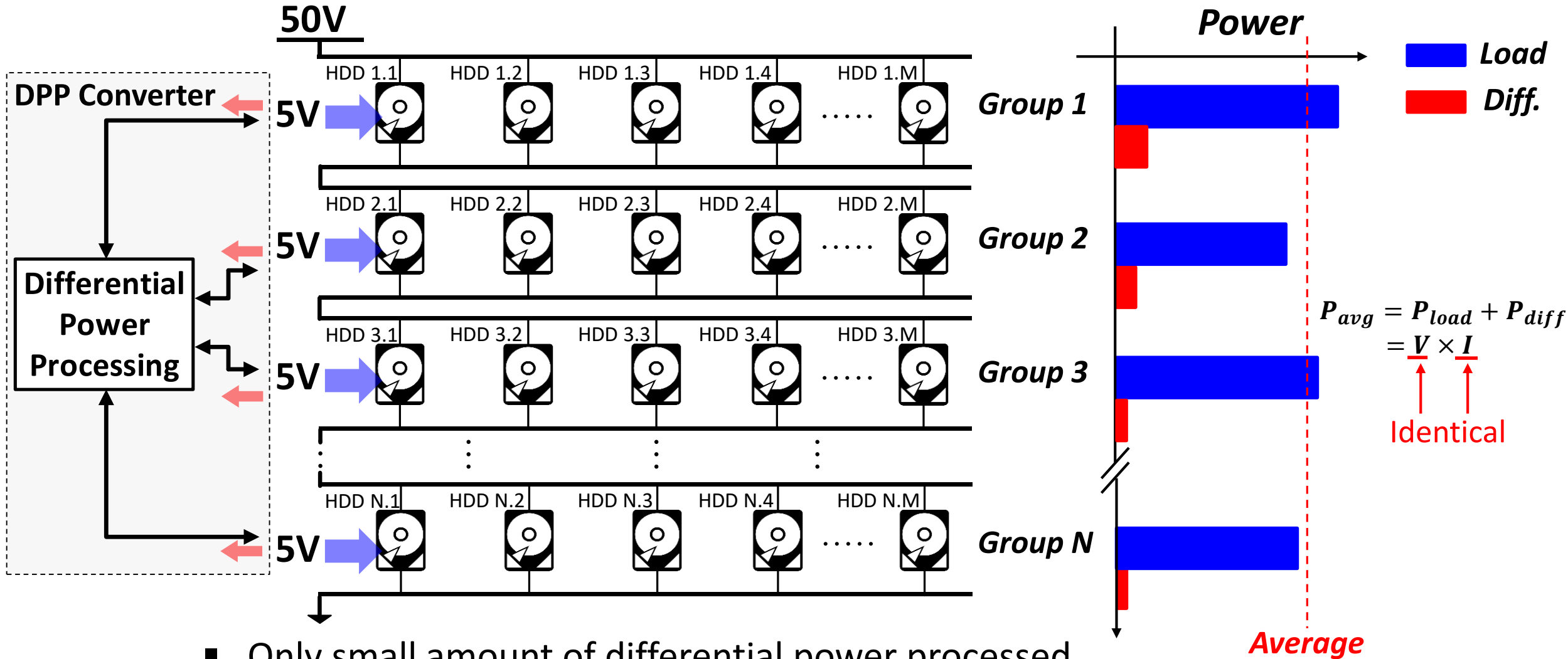
➤ Conventional Voltage Step Down Architecture



- All load power flows through the step-down converter.

Differential Power Processing for HDD Array

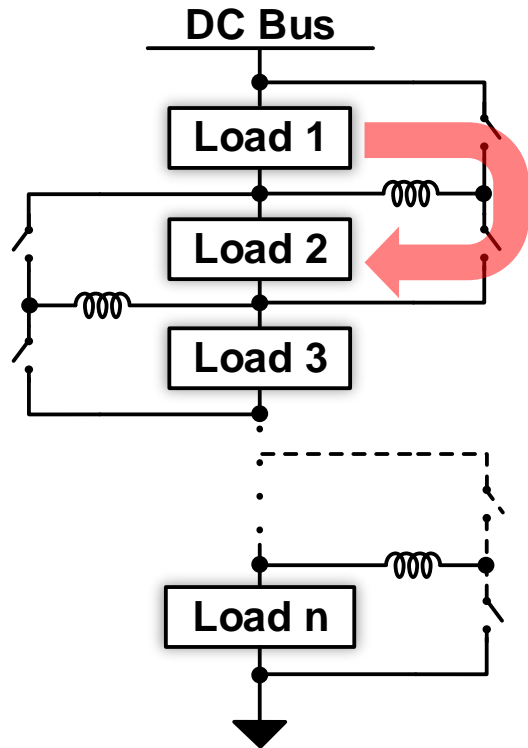
➤ Series-Stacked Power Architecture



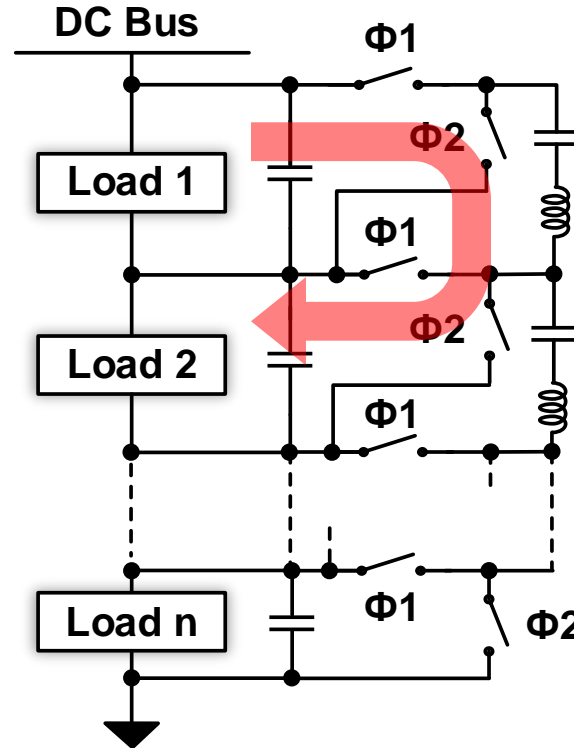
- Only small amount of differential power processed by the differential power processing (DPP) converter.

DPP Converter Topology

- **Ladder DPP^[3]**



- **Switched Capacitor DPP^[4]**



- **Dc-Coupled DPP^[5]**

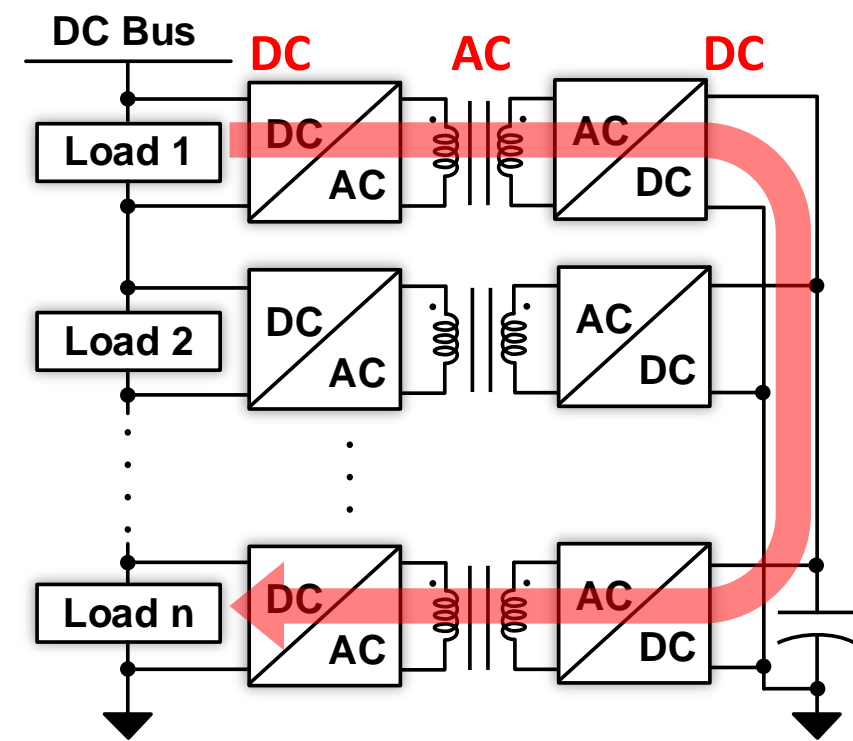
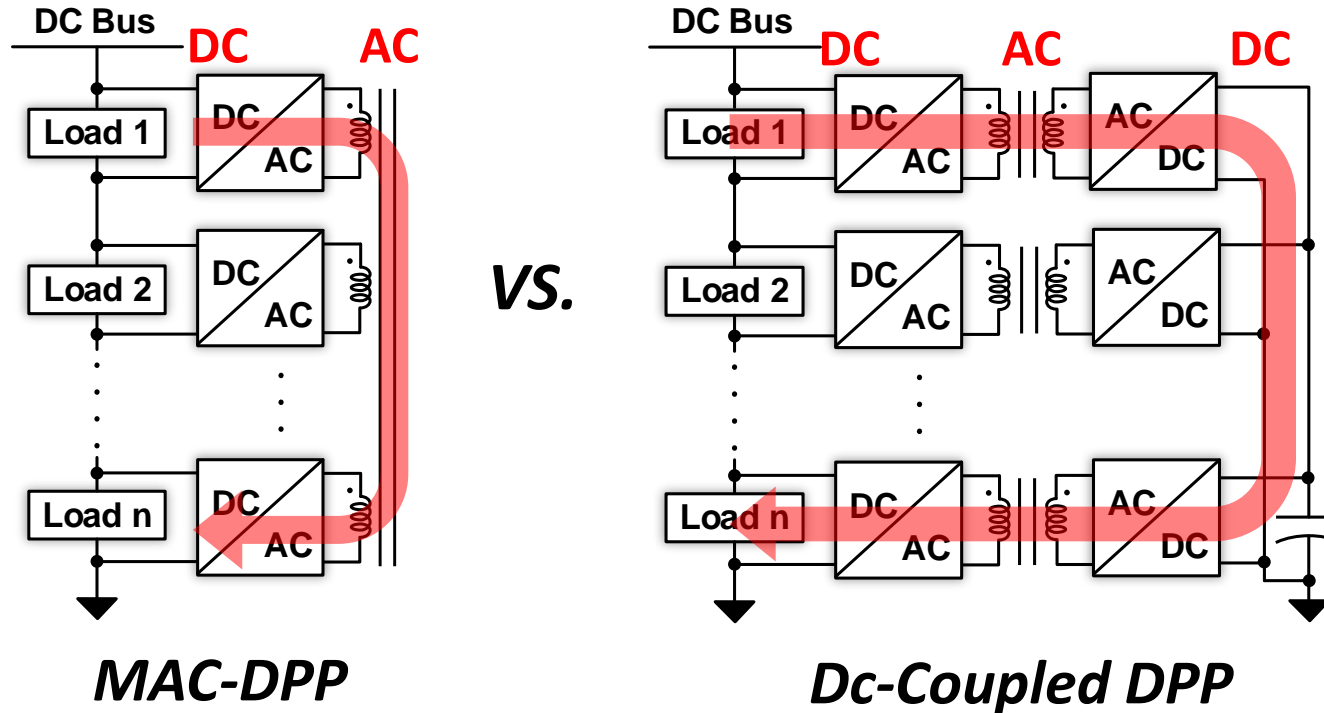


Fig. 5: Three Existing DPP Topologies

- **Ladder DPP & Switched Capacitor DPP:** DPP only between two neighboring ports
- **Dc-Coupled DPP:** Multiple magnetics; Two dc-ac-dc conversion stages

Multiport Ac-Coupled (MAC) DPP Converter

➤ MAC-DPP Compared with Dc-Coupled DPP



Advantages

- Higher power density
- Higher conversion efficiency
- Lower cost

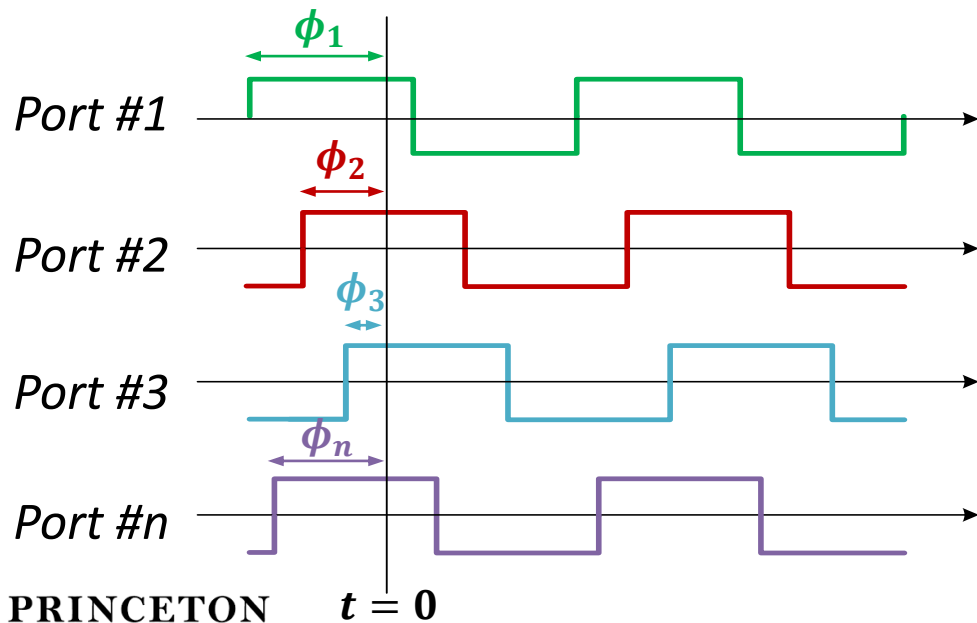
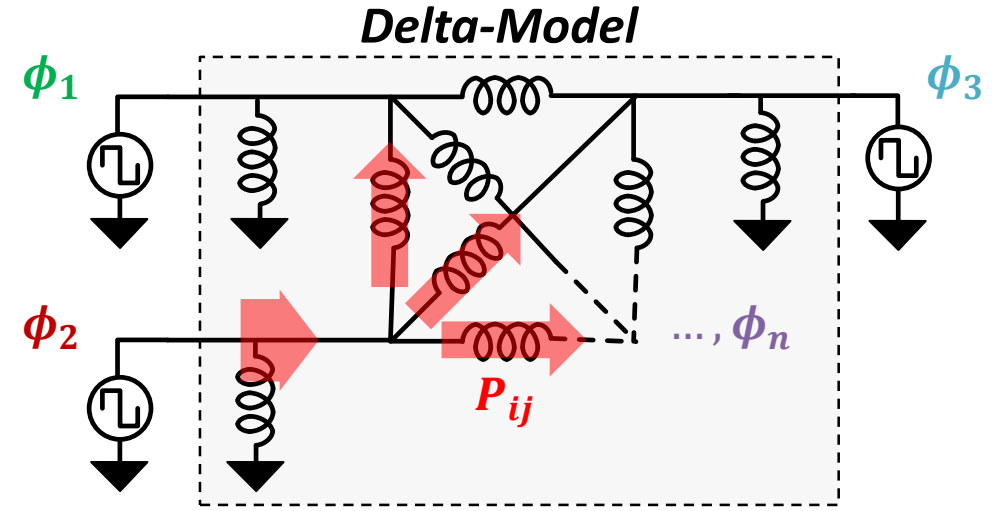
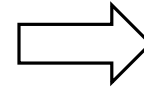
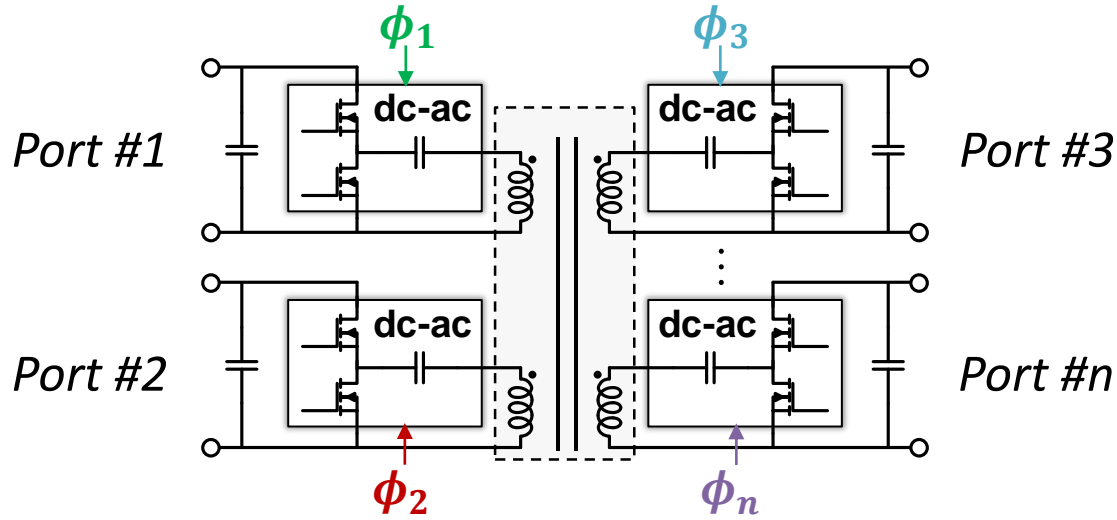
Challenges

- Closely-coupled power flow
- Modeling and control

Number of Devices	MAC-DPP	Dc-Coupled DPP	Benefits
Dc-ac units	N	2N	Lower cost
Transformers	1	N	Higher power density
Dc-ac-dc conversion stages ^[6]	1	2	50% loss reduction

Power Flow Modulation

➤ Multi-port Phase-Shift Modulation



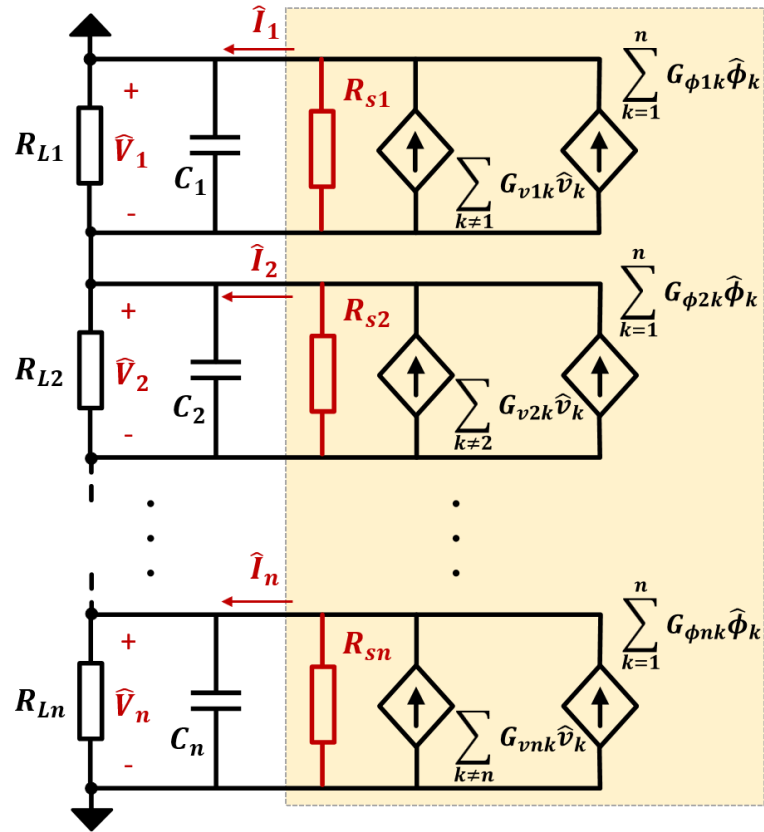
- All ports transferring power simultaneously.

- Total input power flow at *Port #i*:

$$P_i = \sum_{k \neq i} \frac{V_i V_k}{2\pi f L_{ik}} \phi_{ik} \left(1 - \frac{|\phi_{ik}|}{\pi} \right)$$

- Closely-coupled power flow
- Modulating phase-shifts $\{\phi_1, \dots, \phi_n\}$

Small Signal Model



▪ **Step 1: Large Signal Current**

$$I_i = \frac{P_i}{V_i} = \sum_{j \neq i} \frac{V_j}{2\pi f L_{ij}} \phi_{ij} \left(\frac{|\phi_{ij}|}{\pi} - 1 \right)$$

$\frac{\partial I_i}{\partial V_j}$
 $\frac{\partial I_i}{\partial \phi_j}$

▪ **Step 2: Small Signal Current Modeling**

$$\begin{bmatrix} \hat{I}_1 \\ \hat{I}_2 \\ \vdots \\ \hat{I}_n \end{bmatrix} = \begin{bmatrix} 0 & G_{v12} & \cdots & G_{v1n} \\ G_{v21} & 0 & \cdots & G_{v2n} \\ \vdots & \vdots & \ddots & \vdots \\ G_{vn1} & G_{vn2} & \cdots & 0 \end{bmatrix} \begin{bmatrix} dV_1 \\ dV_2 \\ \vdots \\ dV_n \end{bmatrix} + \begin{bmatrix} G_{\phi11} & G_{\phi12} & \cdots & G_{\phi1n} \\ G_{\phi21} & G_{\phi22} & \cdots & G_{\phi2n} \\ \vdots & \vdots & \ddots & \vdots \\ G_{\phi n1} & G_{\phi n2} & \cdots & G_{\phi nn} \end{bmatrix} \begin{bmatrix} \hat{\phi}_1 \\ \hat{\phi}_2 \\ \vdots \\ \hat{\phi}_n \end{bmatrix}$$

$\Downarrow G_v$

$\Downarrow G_\phi$

$$G_{vij} = \frac{\phi_{ij}}{2\pi f L_{ij}} \left(\frac{|\phi_{ij}|}{\pi} - 1 \right) \quad G_{\phi ij} = \begin{cases} \frac{V_j}{2\pi f L_{ij}} \left(1 - \frac{2|\phi_{ij}|}{\pi} \right), j \neq i \\ \sum_{j \neq i} \frac{V_j}{2\pi f L_{ij}} \left(\frac{2|\phi_{ij}|}{\pi} - 1 \right), j = i \end{cases}$$

▪ **Step 3: Considering the load structure**

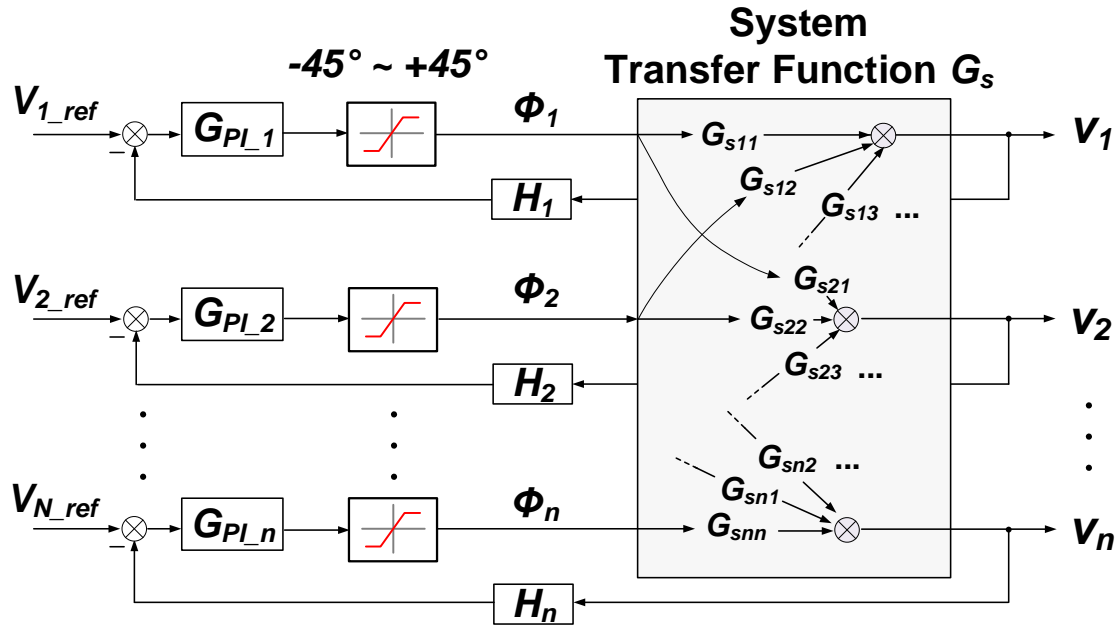
$$\begin{bmatrix} \hat{V}_1 \\ \hat{V}_2 \\ \vdots \\ \hat{V}_n \end{bmatrix} = \begin{bmatrix} -Z_1 \parallel \sum_{k \neq 1} Z_k & \frac{Z_1 Z_2}{\sum_{k=1}^n Z_k} & \cdots & \frac{Z_1 Z_n}{\sum_{k=1}^n Z_k} \\ \frac{Z_2 Z_1}{\sum_{k=1}^n Z_k} & -Z_2 \parallel \sum_{k \neq 2} Z_k & \cdots & \frac{Z_2 Z_n}{\sum_{k=1}^n Z_k} \\ \vdots & \vdots & \ddots & \vdots \\ \frac{Z_n Z_1}{\sum_{k=1}^n Z_k} & \frac{Z_n Z_2}{\sum_{k=1}^n Z_k} & \cdots & -Z_n \parallel \sum_{k \neq n} Z_k \end{bmatrix} \times \begin{bmatrix} \hat{I}_1 \\ \hat{I}_2 \\ \vdots \\ \hat{I}_n \end{bmatrix} \Rightarrow G_z$$

▪ **Step 4. Obtaining System Transfer Function:** $\hat{V} = (I - G_z G_v)^{-1} G_z G_\phi \times \hat{\phi}$

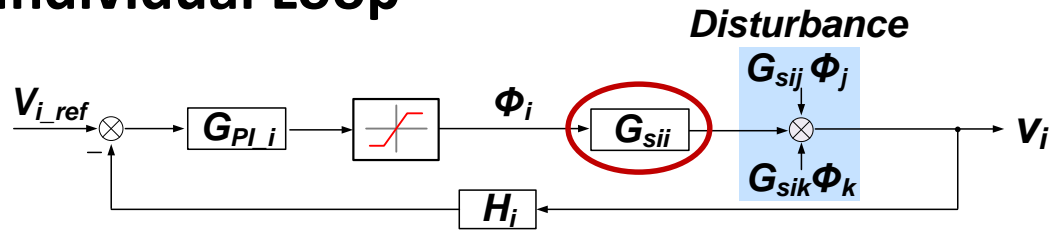
P. Wang, Y. Chen, Y. Elasser and M. Chen, "Small Signal Model for Very-Large-Scale Multi-Active-Bridge Differential Power Processing (MAB-DPP) Architecture," 2019 20th Workshop on Control and Modeling for Power Electronics (COMPEL), Toronto, ON, Canada, 2019, pp. 1-8.

Closed-Loop Voltage Regulation

➤ Distributed Phase-Shift (DPS) Control [7]

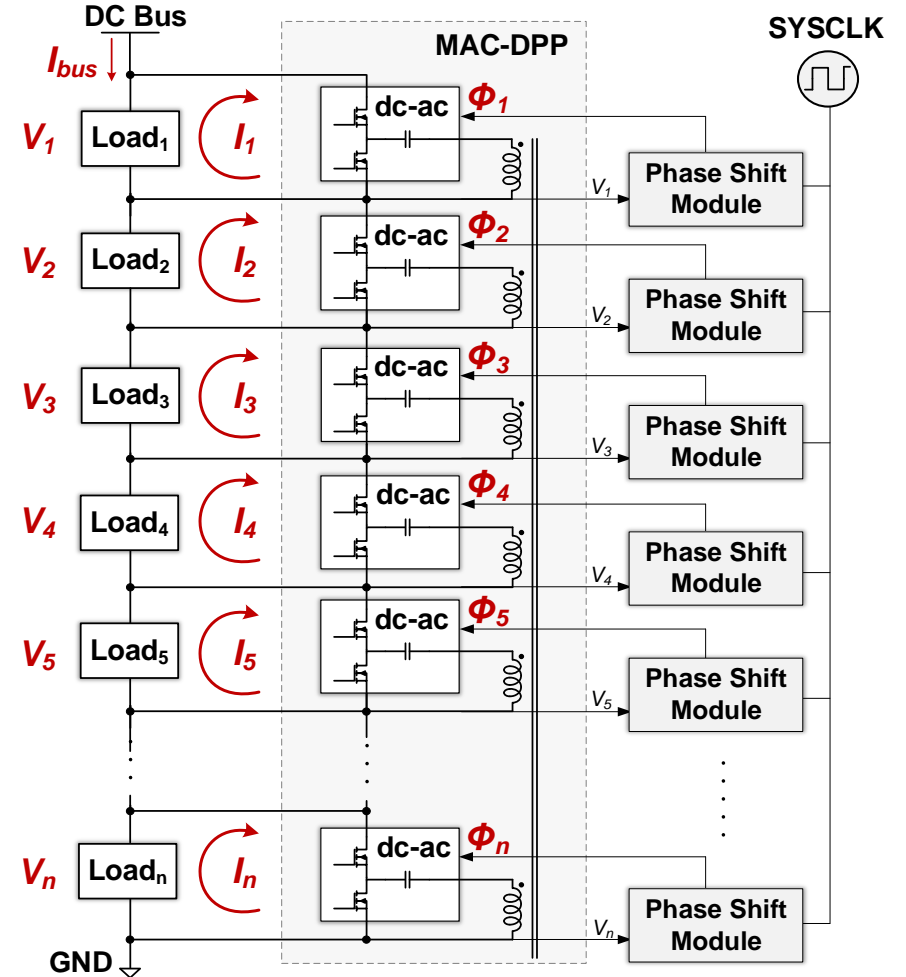


■ Individual Loop



- Design PI parameters based on G_{sii}

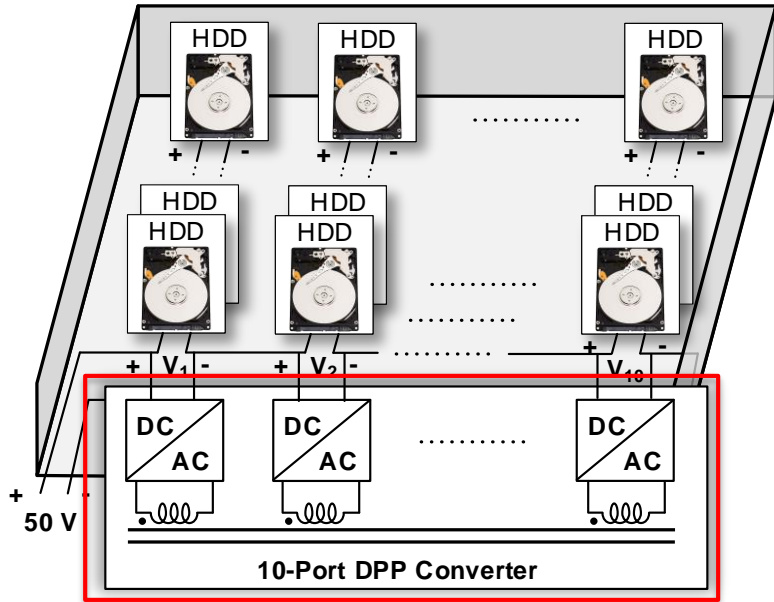
■ System Implementation



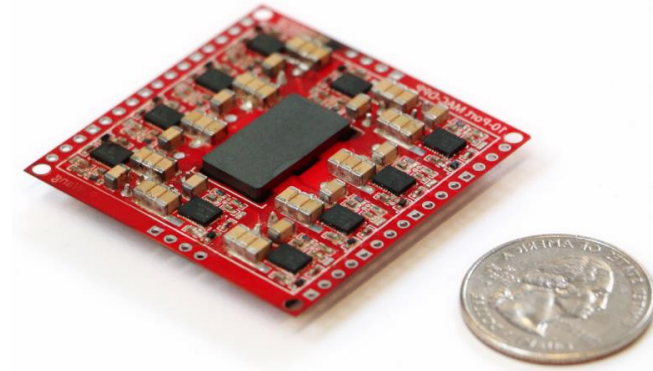
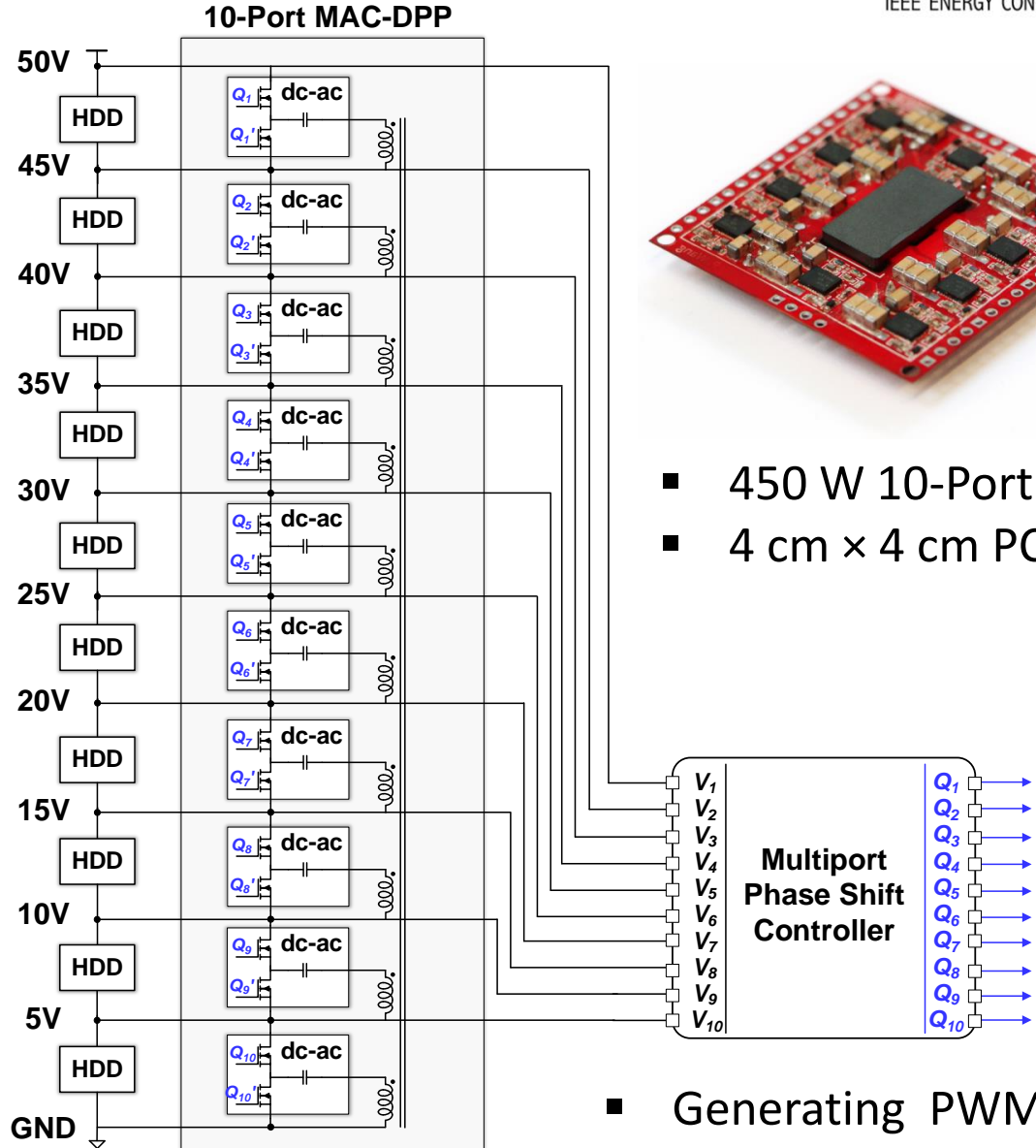
- Enable fully-modular building block

MAC-DPP for Data Storage Server

➤ 50-HDD Data Storage Server



- 10 series-stacked voltage domains (5 × 2.5-inch HDDs at each domain)
- 450 W 10-port MAC-DPP converter
- Ultra-high efficiency and power density
- Hot-swapping capability



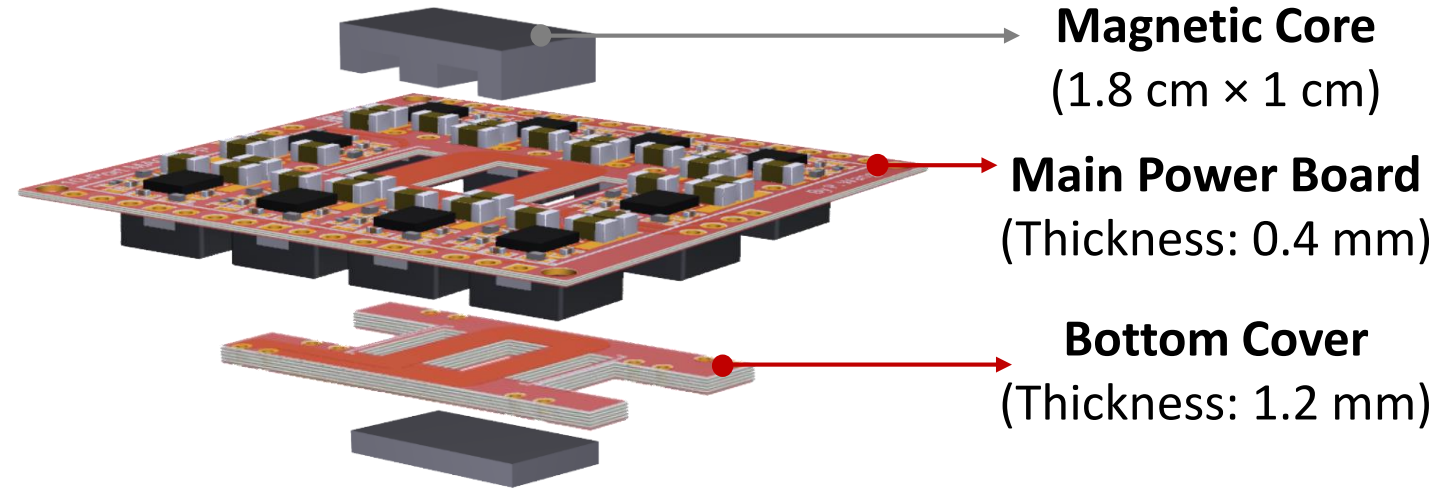
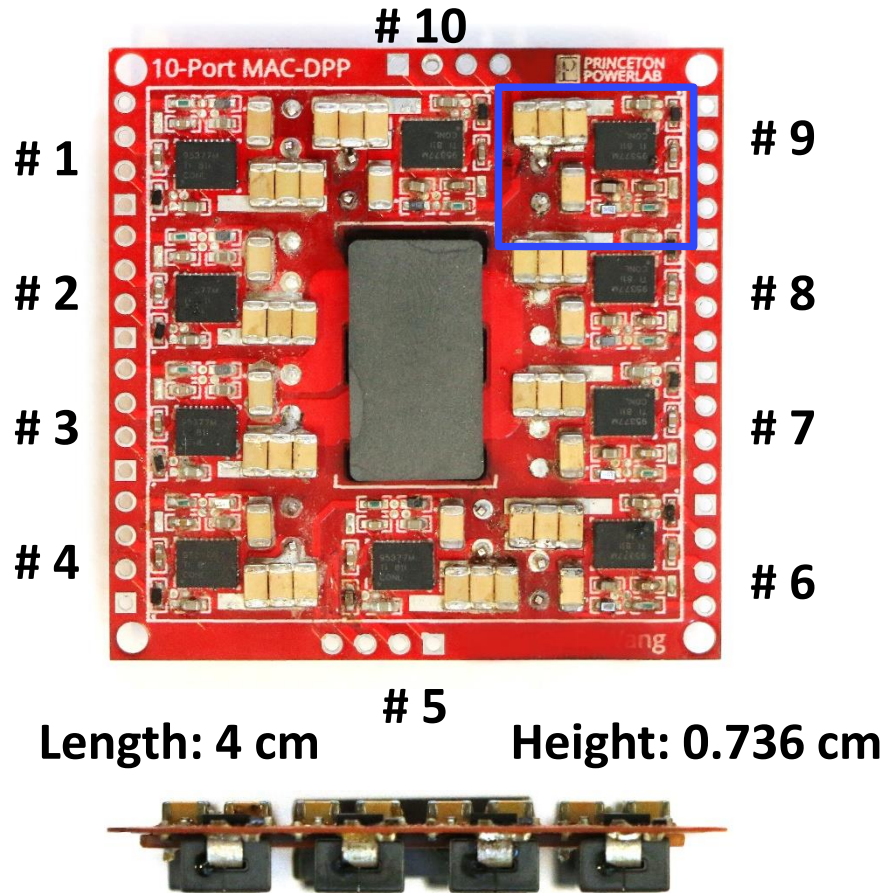
- 450 W 10-Port MAC-DPP
- 4 cm × 4 cm PCB area

- Generating PWMs with different phase-shifts

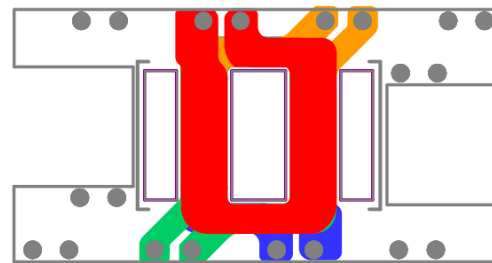
450W 10-Port MAC-DPP Prototype

➤ **Highly-Modular & Ultra-Compact**

➤ **Stacked PCB Planar Magnetics**



▪ **Main Power Board:**



Four Windings

▪ **Bottom Cover:**



Six Windings

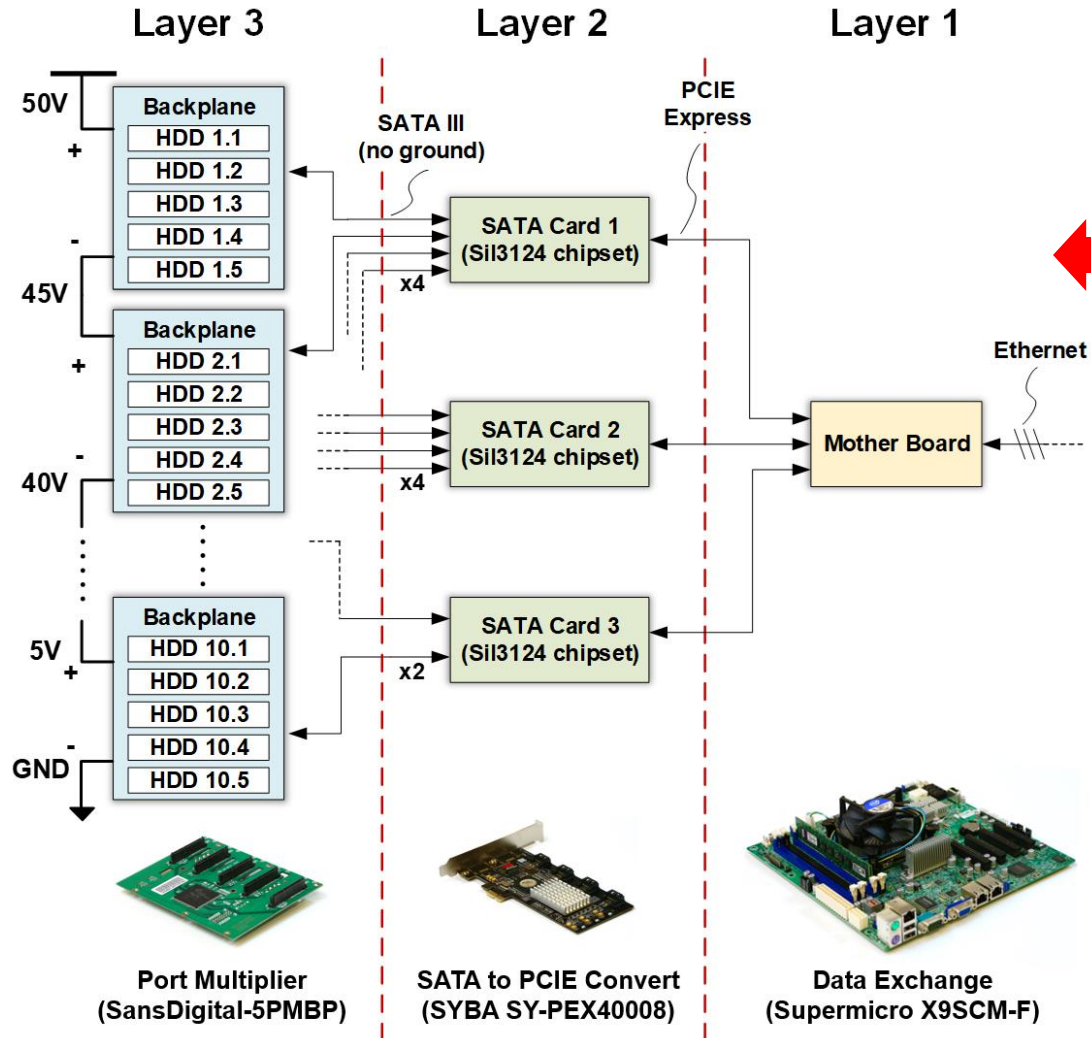
Two-PCB vertical-stacked magnetics design
10x magnetics size reduction

▪ **Volume:** $(1.57 \text{ in})^2 \times 0.29 \text{ in} = 0.71 \text{ in}^3$

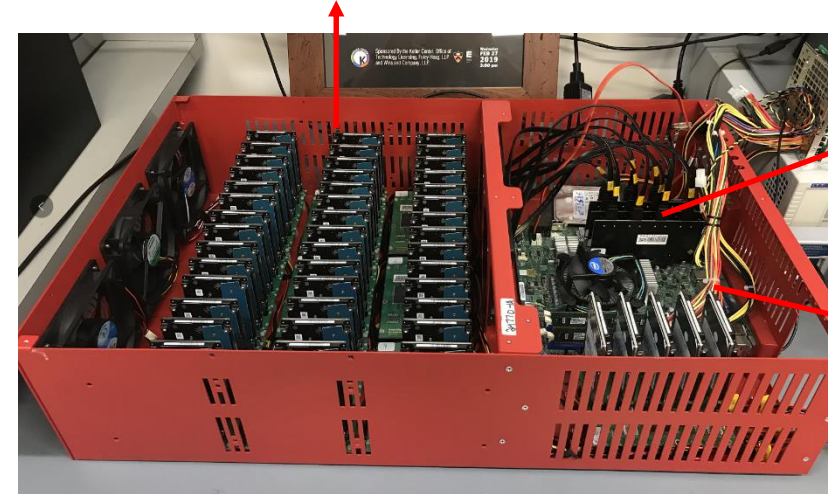
▪ **Power Density:** $\frac{450\text{W}}{0.71\text{in}^3} = 633\text{W/in}^3$

Communication Structure

➤ Three-Layer Communication Link



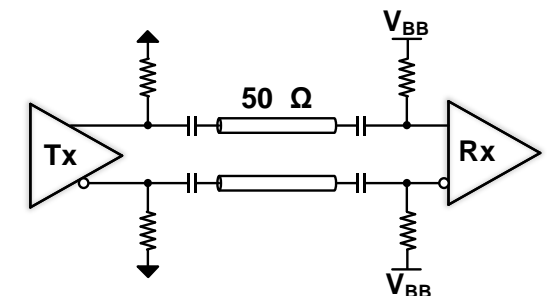
HDD Array with Backplanes



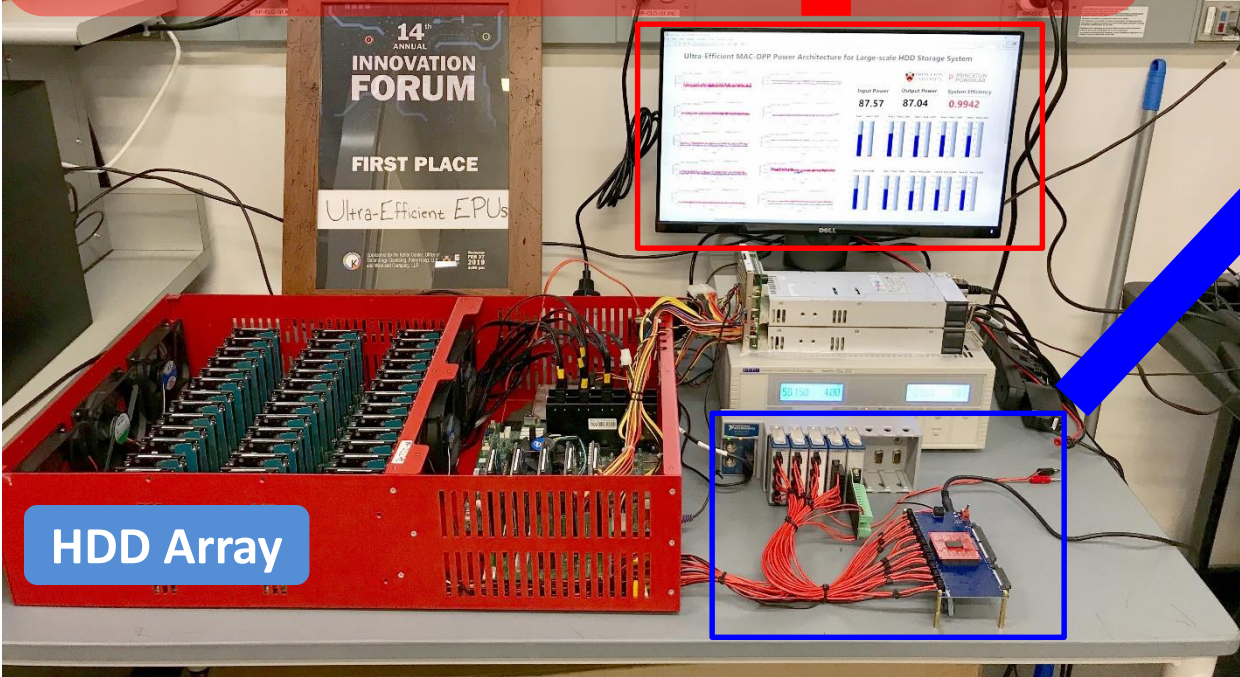
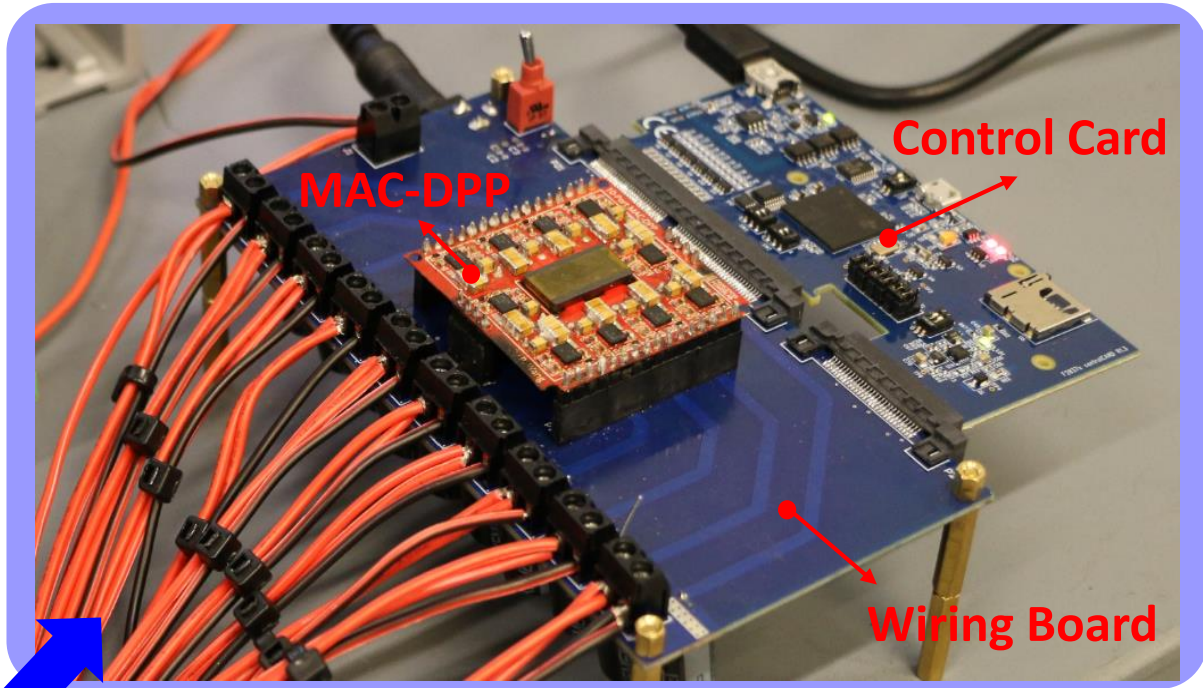
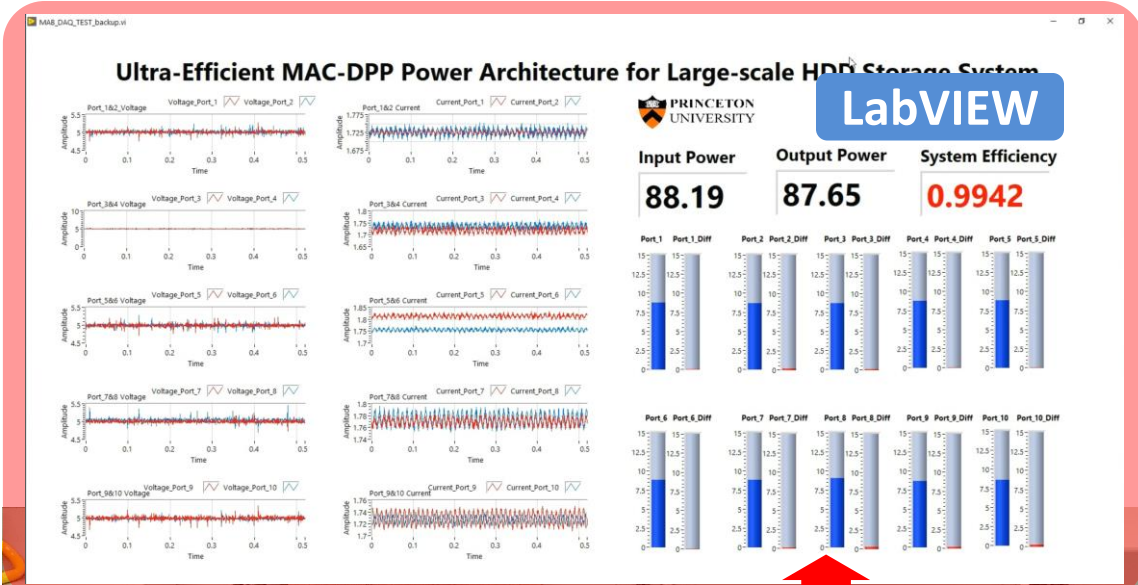
SATA Cards

Mother Board

- Five HDDs parallel on one voltage domain
- Standard SATA differential signal with blocking capacitors across different voltage domains
- Tested full reading/writing of HDDs at different voltage domains.



HDD Testbench with DAQ Measurement System

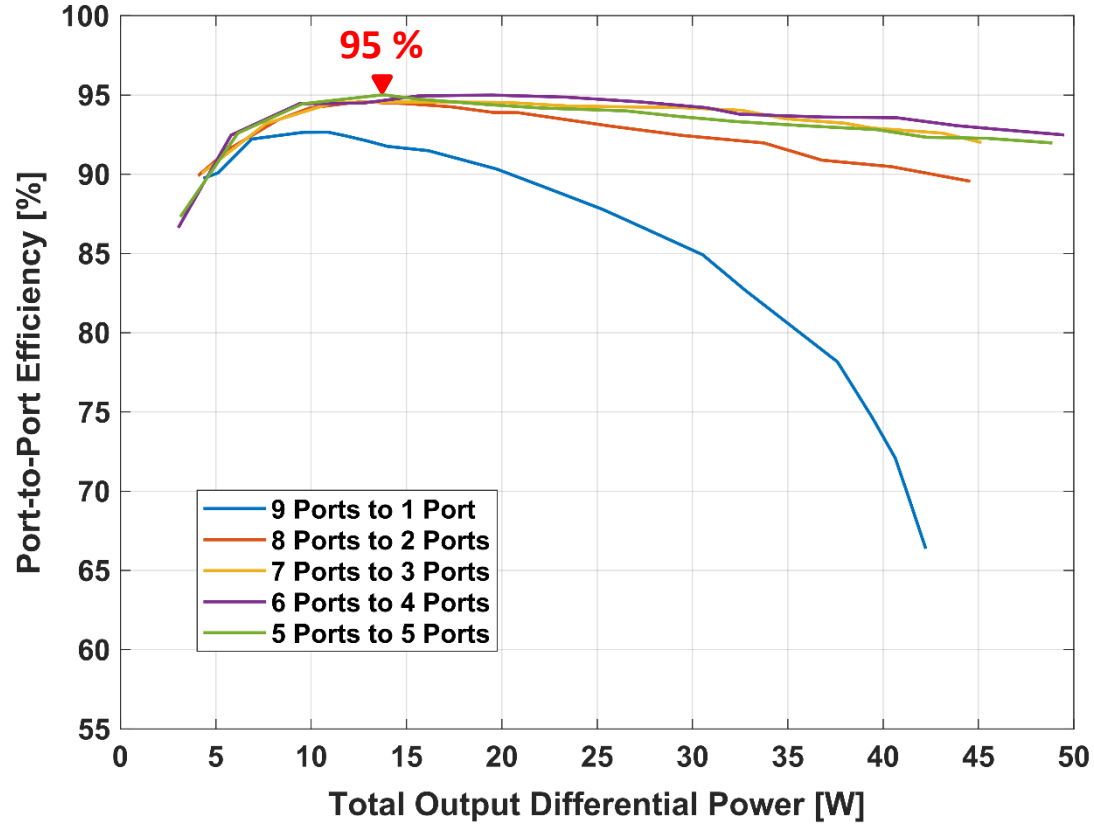


- Tested with Backblaze 50-HDD server
- Power monitoring system with LabVIEW
- Tested full reading/writing, hot-swapping capability of HDDs
- HDD server system efficiency: over 99.4%

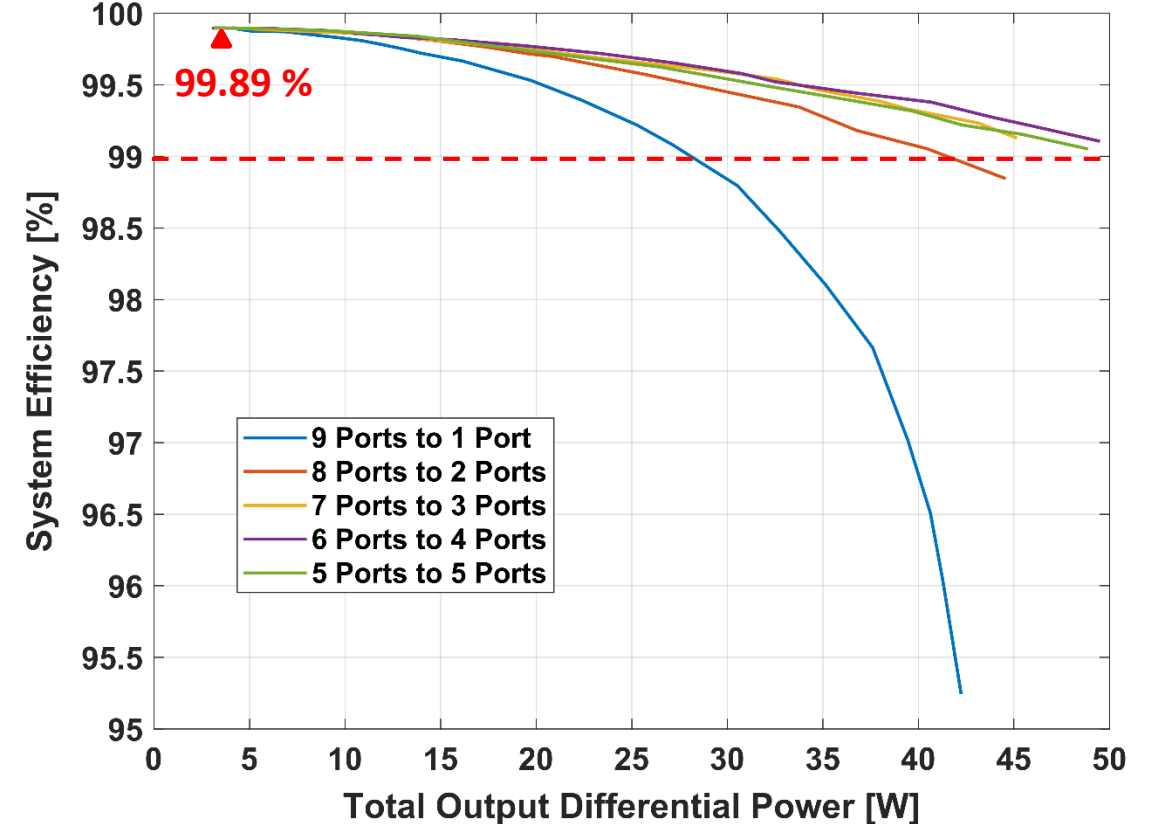
--- Collaborated with Jing Yuan

Efficiency Measurement

Port-to-Port Conversion Efficiency



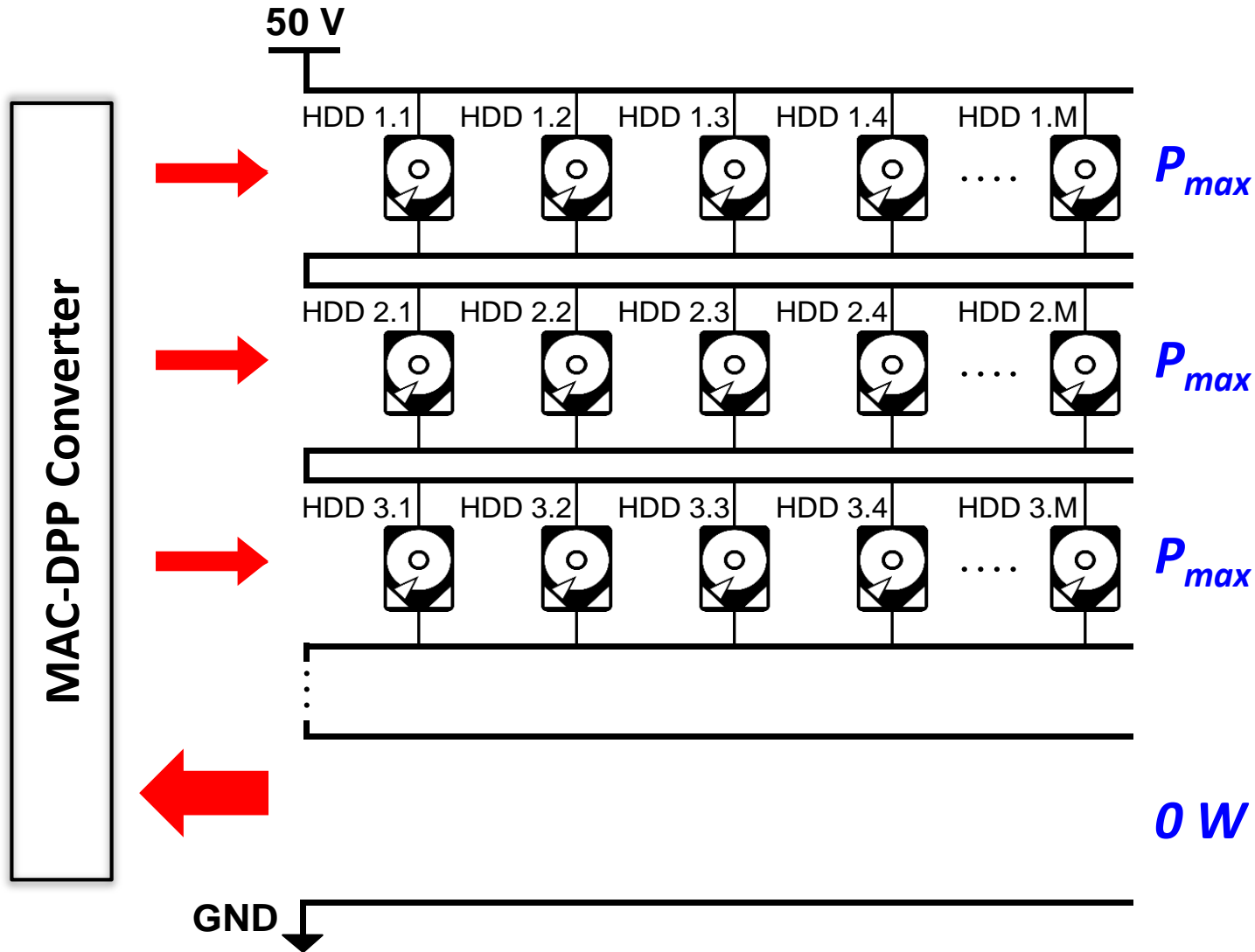
System Conversion Efficiency



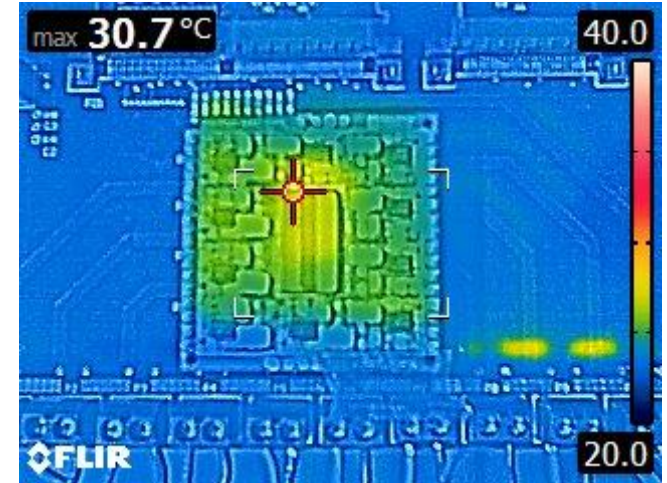
- Achieved 95% peak port-to-port efficiency when delivering 14 W from 5 Ports to 5 Ports
- **Over 99.8% peak system efficiency with 450 W load power**

Hot-Swapping Thermal Image

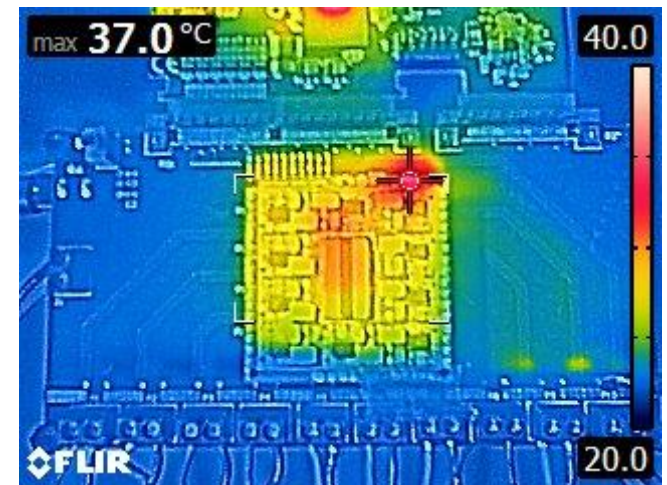
➤ Worst-Case Hot-Swapping Scenario



■ Normal Operation



■ Worst-Case Hot-Swapping



Hot-Swapping Transient Response



Fig. 25: Transient response when removing all 5 HDDs from one voltage domain (Port #3) at HDD server.

- Worst hot-swapping scenario
- Smooth voltage transient with all other HDDs working normally

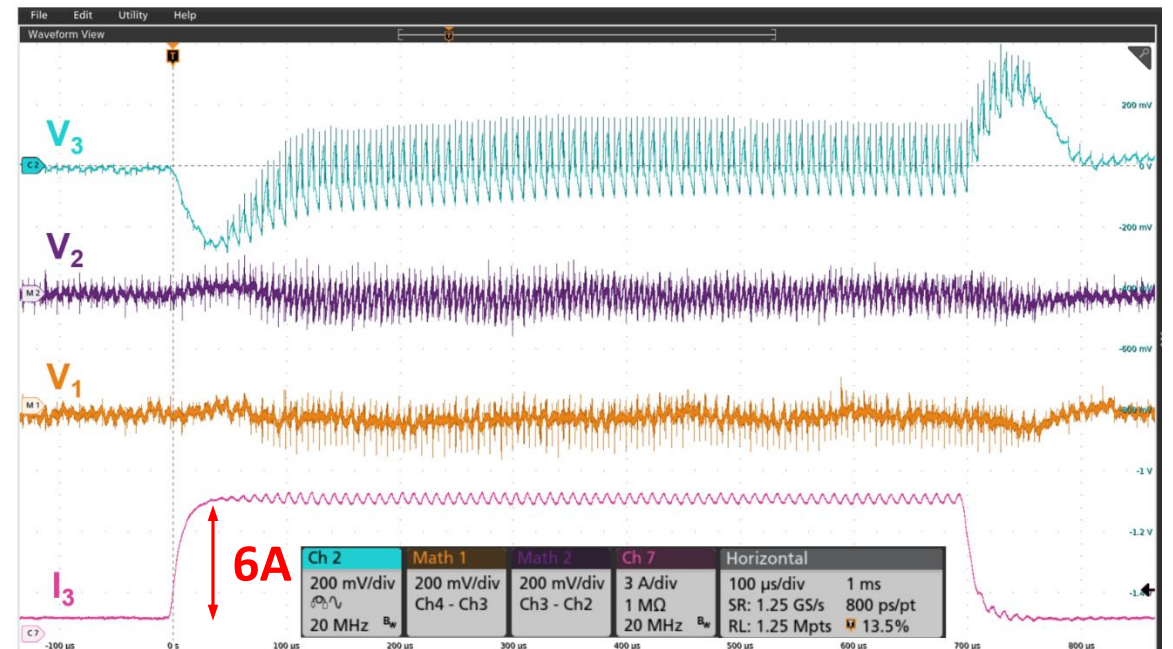
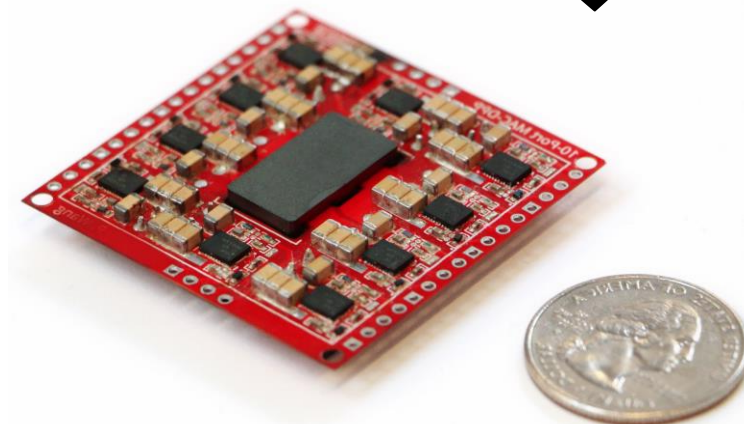
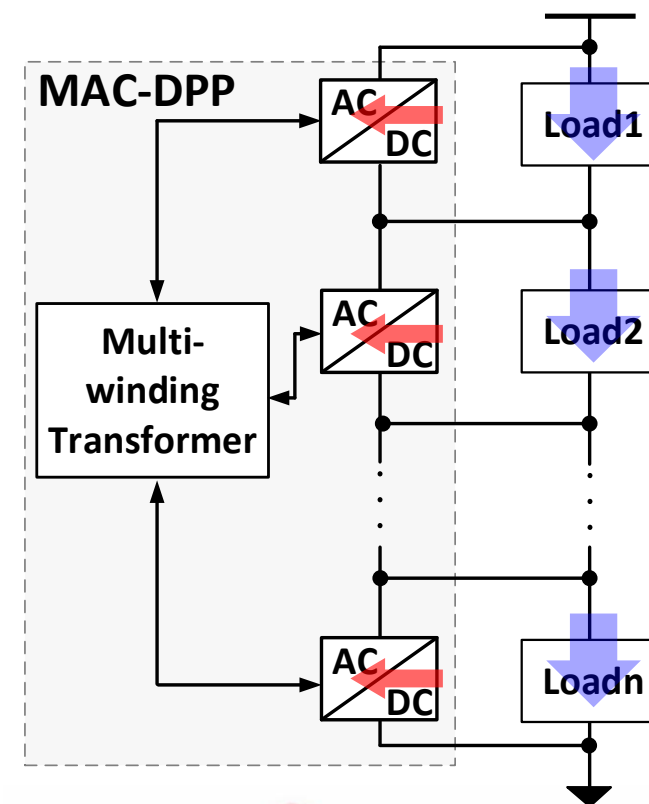


Fig. 26: Transient response of 30 W (6 A) step load change at Port #3.

- Extreme case considering inrush current of HDD motors
- Settling time less than 100 μs
- Overshoot less than 250mV

Summary

- Proposed an ultra-efficient highly-compact MAC-DPP topology for series-stacked modular loads in data centers
- N times magnetics core area reduction; Single dc-ac-dc conversion stage
- Proposed distributed phase-shift control, enabling fully-modular building block
- Designed a 10-port MAC-DPP prototype
- 50-HDD storage server with DAQ measurement system
- **Power rating: Over 450 W**
- **Power density: over 630 W/in³**
- **HDD Server System efficiency: Over 99.4%**
- Maintained normal reading/writing operation at worst hot-swapping scenario



Reference

- [1] A. Shehabi, S. Smith, D. Sartor, R. Brown, M. Herrlin, J. Koomey, E. Masanet, N. Horner, I. Azevedo, and W. Lintner, "United States Data Center Energy Usage Report," 2016.
- [2] S. Jiang, S. Saggini, C. Nan, X. Li, C. Chung and M. Yazdani, "Switched Tank Converters," *IEEE Transactions on Power Electronics*, vol. 34, no. 6, pp. 5048-5062, June 2019.
- [3] G. L. Brainard, "Non-dissipative battery charger equalizer," U.S. Patent 5479083, Dec. 26, 1995
- [4] J. T. Stauth, M. D. Seeman and K. Kesarwani, "Resonant Switched-Capacitor Converters for Sub-module Distributed Photovoltaic Power Management," *IEEE Transactions on Power Electronics*, vol. 28, no. 3, pp. 1189-1198, March 2013.
- [5] E. Candan, P. S. Shenoy and R. C. N. Pilawa-Podgurski, "A Series-Stacked Power Delivery Architecture with Isolated Differential Power Conversion for Data Centers," *IEEE Transactions on Power Electronics*, vol. 31, no. 5, pp. 3690-3703, May 2016.
- [6] P. Wang and M. Chen, "Towards Power FPGA: Architecture, Modeling and Control of Multiport Power Converters," *2018 IEEE 19th Workshop on Control and Modeling for Power Electronics (COMPEL)*, Padua, 2018, pp. 1-8.
- [7] P. Wang, Y. Chen, Y. Elasser and M. Chen, "Small Signal Model for Very-Large-Scale Multi-Active-Bridge Differential Power Processing (MAB-DPP) Architecture," *2019 IEEE 20th Workshop on Control and Modeling for Power Electronics (COMPEL)*, Toronto, ON, 2019, pp. 1-8.