Analysis and Design of Series Voltage Compensator for Differential Power Processing

Ping Wang, *Student Member, IEEE* and Minjie Chen, *Senior Member, IEEE*

***Abstract*—Differential power processing (DPP) has been proved effective in many applications. This paper explores a series voltage compensator (SVC) architecture for voltage regulation of differential power processing (DPP) systems. An SVC is connected in series between the input dc bus and the DPP system to compensate for the voltage difference. It only processes a fraction of the overall power. The inclusion of an SVC changes the power flow of the DPP system and changes the loss distribution. We theoretically investigated the SVC power rating and the additional power conversion stress that SVC brings to the DPP converter, and identified the operating conditions in which an SVC is attractive or not compared to a conventional DPP pre-regulation converter that has to process the full power. Our analysis provides insights into system design and control strategy of SVC-DPP topologies. To validate the principles of SVC, a buck SVC is designed and applied to a 10-port DPP converter. The buck SVC can efficiently convert an input voltage ranging from 50 V to 65 V into a regulated 50 V for the DPP system. The size of the SVC is only 20% of the DPP converter, and the peak efficiency of the SVC-DPP system achieves 98.8%.**

***Index Terms*—differential power processing, voltage regulation, partial power processing, battery management systems, photovoltaic systems, data center power management**

I. Introduction

Differential power processing (DPP) is a promising power delivery solution for a wide range of applications. DPP systems were initially developed for series battery systems as active equalization circuits [2]–[8]. Similar circuits were later applied to photovoltaic (PV) systems in order to manage current mismatch and achieve maximum power point tracking (MPPT) for series-connected PV cells [9]–[15]. Recently, DPP architecture has also been utilized to reduce power conversion stages for many emerging dc systems such as servers and telecom loads in data centers [16], [17] and multi-processor systems [18]. In a DPP system, power converters only process a small fraction of the total power, yielding greatly improved system efficiency and reduced size [19].

One challenge for DPP system design is to regulate the stacked string voltage. In DPP systems where the series loads are directly connected to the input dc bus, the stacked DPP string voltage is fixed to the input dc bus voltage. The tightly-coupled load voltage and bus voltage might deteriorate system performance. In PV systems, for example, the voltage to achieve MPPT for each PV string varies due to illuminance difference. Directly connecting multiple PV strings to the dc bus forces different PV strings to share the same string voltage, lowering the overall power generation. In other cases such as servers in data centers, the dc bus voltage in a server rack may change between 48 V to 54 V, whereas the IT equipment needs precisely regulated voltage (e.g., 24 V, 12 V, or 5 V) to function properly. An input regulation stage that decouples the series domain voltage from the dc bus voltage is needed and is the main focus of this paper.

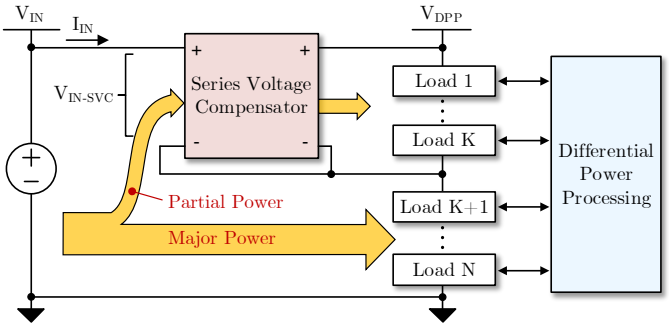


Fig. 1. A series voltage compensator (SVC) leveraging the partial power processing concept for voltage regulation of DPP systems. SVC only processes a fraction of total power. Major power is directly delivered to the DPP loads.

The most straightforward way of implementing an input voltage regulator is to design a standalone front-end dc-dc converter. In this case, however, the front-stage dc-dc converter processes the full load power, reducing the benefits gained from differential power processing and limiting the overall system efficiency and power density that can be achieved. An alternative way is to regulate the DPP string voltage through partial power processing. The partial power processing concept was initially found in PV applications [20]–[22]. Similar topologies such as sigma converter [23] and composite converter [24] were proposed later. These topologies can be generally classified into two categories: input-parallel-output-series (IPOS) structure and input-series-output-parallel structure (ISOP) [25], [26]. Usually, in partial power converters, major power is directly delivered to the loads. The direct power has no impact on the size or losses of power converters [27]–[29]. Some partial power converters might deliver the majority of power through a high-efficiency fixed-ratio dc-dc conversion stage to minimize the cost of size or losses. Consequently, only a fraction of power (i.e., partial power) is processed by the voltage regulation stage, contributing to power rating reduction and efficiency improvement [30], [31].

Leveraging the partial power processing concept, a vari-

The authors are with the Department of Electrical Engineering and Andlinger Center for Energy and the Environment at Princeton University, Princeton, NJ 08540, USA. Corresponding author: Minjie Chen.

This paper is an extension of a published conference paper, "Series Voltage Compensator for Differential Power Processing" in IEEE ECCE 2020 [1].

This work was jointly supported by the NSF CAREER award (#1847365), and the DOE ARPA-E CIRCUITS Program (DE-AR0000906).

ety of series voltage compensators (SVCs) for voltage pre-regulation in DPP systems are investigated and compared in this paper. Fig. 1 shows the general architecture of an SVC. Different from a standalone voltage pre-regulator, the SVC converter is in effect connected in series with the DPP loads, compensating for the voltage difference between the input dc bus and stacked DPP loads. The negative terminals of the input and output ports of SVC are tied to the middle of the stacked loads, leading to a decreased voltage rating. Therefore, SVC only processes a fraction of the overall system power and delivers it to the top few voltage domains. A majority of the power is directly delivered to the DPP loads. The topologies presented in [32]–[34] are a subset of the SVC family investigated in this paper. We generalize these topologies and perform a systematic analysis on the power rating and the additional power conversion stress that SVC brings to DPP converters. To validate the theoretical analysis, a buck SVC topology was designed and tested with a 10-port ac-coupled DPP converter which drives a 10×60 LED array. The prototype SVC also provides soft-start and fault protection functions to the system. It can regulate the DPP string voltage at 50 V when the input dc bus voltage ranges from 50 V to 65 V. The peak system efficiency is 98.8%.

The remainder of this paper is structured as follows. Section II introduces the working principles of SVC and analyzes the additional power conversion stress it brings to the system. Section III analyzes several SVC circuits and compares their component stress and voltage regulation ranges. Section IV presents the design of a buck SVC and a 10-port DPP converter, including the converter power ratings and control strategy for voltage regulation. Experimental results are provided in Section V. Finally, Section VI concludes this paper.

II. Power Processing Analysis of SVC

As shown in Fig. 1, an SVC converter is a modified dc-dc converter with unique input/output terminal configurations to take advantage of partial power processing. The input and output negative terminals of the SVC converter are connected to the middle of the stacked loads. In this way, the SVC current rating is the same as the overall system, but its voltage rating is only a portion of the system voltage rating. Therefore, the SVC converter processes a fraction of the total system power and can have much lower power loss and component size compared to a standalone dc-dc regulator. Although the SVC converter only processes a portion of the system power, it may increase the power conversion stress of the DPP converters. As indicated in Fig. 2, the SVC only delivers power to the top few voltage domains, creating additional power imbalance which needs to be handled by the DPP converter.

The main purpose of this paper is to identify the operating conditions in which an SVC is attractive or not compared to a conventional DPP pre-regulation converter that has to process the full power as shown in Fig. 3. Both the SVC power conversion stress and the additional stress introduced by the SVC to the DPP are considered in this comparison. The operation boundaries for SVC to achieve lower overall system stress than a traditional DPP pre-regulation converter

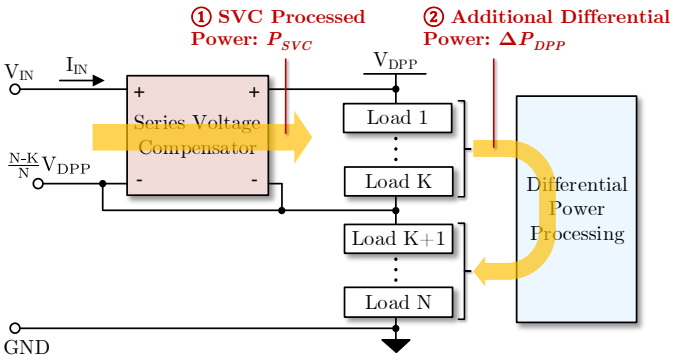


Fig. 2. The SVC incurred power processing consists of: (1) SVC processed power P_{SVC}; (2) additional differential power in DPP converters ΔP_{DPP}.

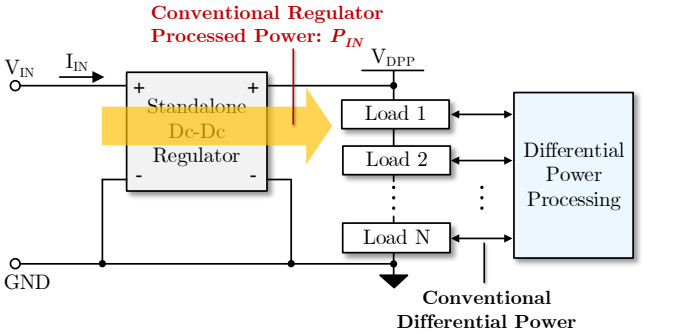


Fig. 3. Conventional voltage pre-regulator for DPP system. In contrast, the standalone dc-dc regulator needs to process total system input power P_{IN}.

are derived. To the best of the authors' knowledge, this is the first systematic analysis of the impact of SVC on DPP.

A. SVC Processed Power

Fig. 2 labels the voltage and current ratings of an SVC. Assume the DPP system comprises N series voltage domains, and the negative terminals of the input and output ports of the SVC are tied to the negative terminal of the K^{th} domain with voltage as $\frac{N-K}{N}V_{DPP}$, the power processed by the SVC is

$$P_{SVC} = \left(V_{IN} - \frac{N-K}{N}V_{DPP}\right) I_{IN}. \quad (1)$$

To quantify the benefits of partial power processing, the SVC processed power is normalized to the total system input power and is denoted as ρ_{SVC}:

$$\rho_{SVC} = \frac{\left(V_{IN} - \frac{N-K}{N}V_{DPP}\right) I_{IN}}{V_{IN} I_{IN}} = 1 - (1 - K_s)M_v. \quad (2)$$

Here, $M_v = \frac{V_{DPP}}{V_{IN}}$ is the voltage regulation ratio; $K_s = \frac{K}{N}$ is the ratio of the SVC-tied voltage domain to the overall number of voltage domains. The SVC converters discussed herein are non-inverting converters and their input or output polarity does not flip during the operation. Thus, the input voltage (V_{IN}) should be larger than the negative terminal voltage of the K^{th} domain ($\frac{N-K}{N}V_{DPP}$). As a result, the feasible range for M_v is: $M_v < \frac{1}{1-K_s}$.

Fig. 4 plots the normalized SVC power as a function of the voltage regulation ratio with different values of K_s. If

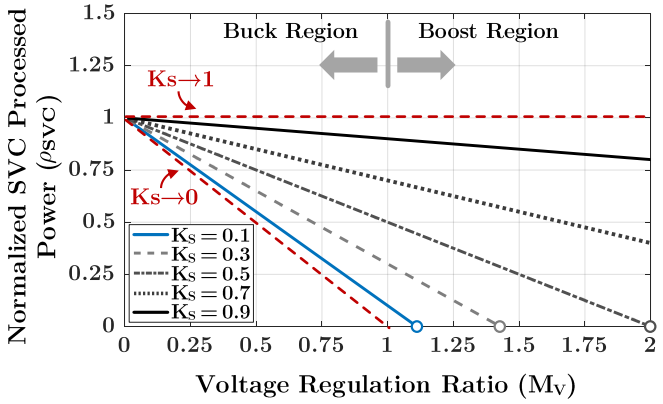


Fig. 4. Normalized SVC processed power ρ_{SVC} as a function of voltage regulation ratio M_v. $K_s = \frac{K}{N}$ is the ratio of SVC-tied voltage domain to the overall number of voltage domains. If $K = 1$ and N is very large, $K_s \to 0$ and $\rho_{SVC} = 0$ at $M_v = 1$. When $K_s \to 1$, SVC behaves like a standalone dc-dc regulator and ρ_{SVC} is a constant one. Each curve is plotted only within its feasible range: $M_v < \frac{1}{1-K_s}$.

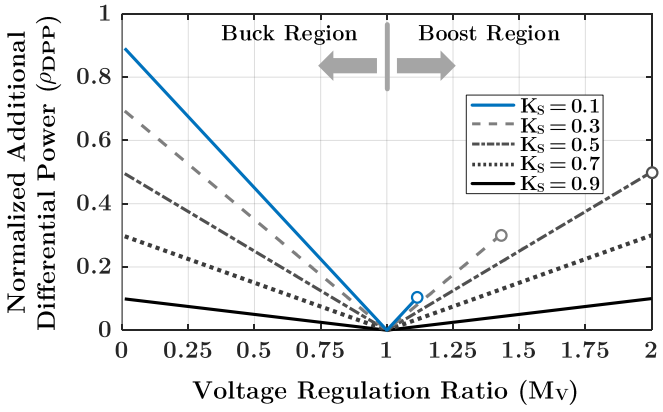


Fig. 5. Normalized additional DPP processed power ρ_{DPP} as a function of the voltage regulation ratio M_v.

$K = 1$ and N is very large, $K_s \to 0$ and $\rho_{SVC} = 0$ at $M_v = 1$, indicating that the SVC is not processing power. When $K_s \to 1$, the output of SVC is almost directly attached to the entire DPP series voltage domains. In this case, the SVC becomes a conventional standalone dc-dc regulator, and ρ_{SVC} becomes one, as shown in Fig. 4. ρ_{SVC} will increase as M_v decreases in both buck region ($M_v < 1$) and boost region ($1 < M_v < \frac{1}{1-K_s}$), but it will be always less than one, indicating that the SVC processed power is always less than the total load power. As K_s increases, the voltage regulation range in the boost region will be larger, but the SVC voltage rating will also increase, resulting in a higher ρ_{SVC}.

B. Additional Differential Power

In DPP systems, power converters work to balance the differential power among the series domains. SVC that only delivers power to the top few voltage domains will cause power imbalance among the series domains and bring additional power conversion stress to the DPP system. DPP converters need to cope with both the inherent power mismatch

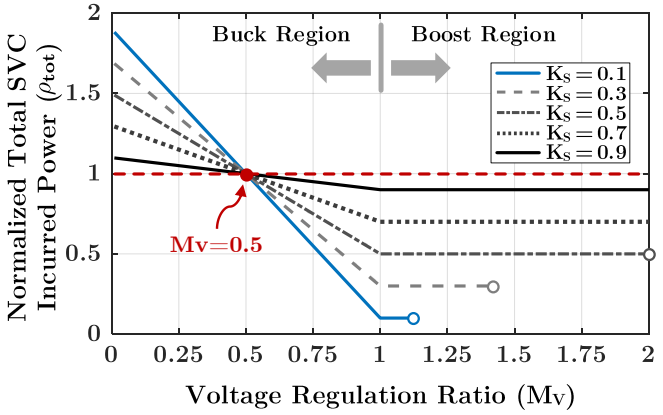


Fig. 6. Normalized total SVC incurred power processing $\rho_{tot} = \rho_{SVC} + \rho_{DPP}$ as a function of the voltage regulation ratio M_v.

TABLE I
SVC INCURRED POWER PROCESSING IN BUCK AND BOOST REGION

	Buck Operation Region ($M_v < 1$)	Boost Operation Region ($1 < M_v < \frac{1}{1-K_s}$)
ρ_{SVC}	$1-(1-K_s)M_v$	$1-(1-K_s)M_v$
ρ_{DPP}	$(1-K_s)(1-M_v)$	$(1-K_s)(M_v-1)$
ρ_{tot}	$(2-K_s)-(2-2K_s)M_v$	K_s

of the series domains and the power imbalance caused by SVC. This subsection quantitatively analyzes the additional differential power in a fully-coupled DPP architecture [37], where there is a direct power flow path between any two voltage domains. The analytical framework can be further extended to other DPP architectures (e.g., ladder DPP [5], [12]–[14]) with indirect power delivery paths.

Differential power flow in DPP systems is determined by power distribution across series voltage domains, which is dynamic and unpredictable [37], [38]. For a well-designed DPP system, however, load powers of different voltage domains are expected to be close by average [17]. Thus, we analyze the average increased differential power caused by SVC by assuming a uniform load power across all series domains. In this case, the average summed load power of top K voltage domains is $\frac{K}{N}P_{IN}$, and the power that SVC delivered to the top K domains is $\rho_{SVC}P_{IN}$. If SVC operates in buck region, $\rho_{SVC} > \frac{K}{N}$, thus the DPP converter needs to deliver the differential power $\left(\rho_{SVC} - \frac{K}{N}\right)P_{IN}$ from the top K domains to the lower $N-K$ domains. When SVC is working in boost region, $\rho_{SVC} < \frac{K}{N}$, the DPP converter needs to deliver the differential power $\left(\frac{K}{N} - \rho_{SVC}\right)P_{IN}$ in an opposite way. For both buck and boost regions, the average additional differential power that an SVC brings to the system is

$$\Delta P_{DPP} = \left|\rho_{SVC} - \frac{K}{N}\right| \times V_{IN}I_{IN}. \quad (3)$$

Similarly, we normalize the additional differential power to the total input power:

$$\rho_{DPP} = \frac{\left|\rho_{SVC} - \frac{K}{N}\right| V_{IN}I_{IN}}{V_{IN}I_{IN}} = (1-K_s)\left|1-M_v\right|. \quad (4)$$

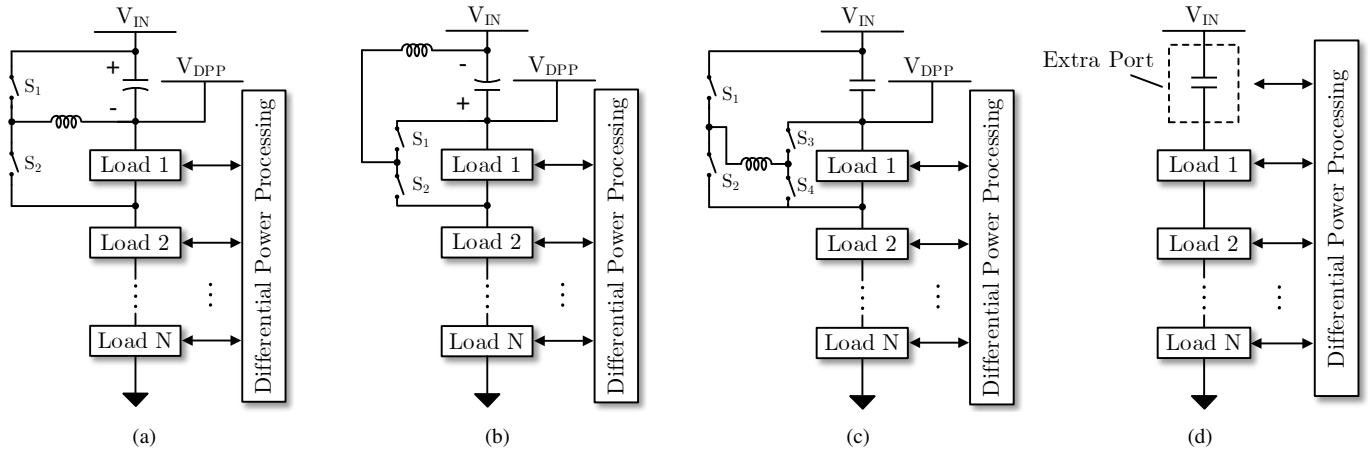


Fig. 7. Several circuit implementations of SVC: (a) buck SVC; (b) boost SVC; (c) buck-boost SVC; (d) extra DPP port [33], [34]. The negative terminal of the input and output ports of the SVC is connected to the negative terminal of the first voltage domain to achieve the maximum benefits.

Fig. 5 plots the relationship between the normalized additional differential power and the voltage regulation ratio M_v. In both buck and boost region, ρ_{DPP} increases as M_v deviates one (i.e., gap between V_{IN} and V_{DPP} becomes larger). ρ_{DPP} becomes zero if $M_v = 1$ (i.e., V_{IN} equals V_{DPP}). Different from ρ_{SVC}, ρ_{DPP} will be lower as K_s increases. As $K_s \to 1$, the SVC behaves more like a standalone dc-dc regulator, and the additional power stress reduces.

A normalized total SVC incurred power processing ρ_{tot} ($\rho_{tot} = \rho_{SVC} + \rho_{DPP}$) is used as a performance metric for evaluating the performance of an SVC. A lower ρ_{tot} indicates a lower total power stress and better performance. If $\rho_{tot} > 1$, the total SVC incurred power processing will be higher than total input power, and the SVC loses advantages compared to a standalone dc-dc regulator. Fig. 6 plots ρ_{tot} as a function of M_v. ρ_{tot} keeps constant ($\rho_{tot} = K_s$) when SVC operates in boost region. If SVC works in buck region, ρ_{tot} will increase as M_v decreases (i.e., larger difference between V_{IN} and V_{SVC}), and it will be larger than one if $M_v < 0.5$ for any K_s. If the voltage regulation ratio M_v is larger than 0.5 ($V_{in} < 2V_{DPP}$), the overall SVC incurred power processing ($\rho_{SVC}+\rho_{DPP}$) is lower than 1, regardless of how the SVC and DPP are configured (independent from K_s), indicating that a DPP with SVC can offer better performance than a traditional DPP architecture with a standalone, fully rated regulation stage in most operating conditions. Detailed normalized figure-of-merits for SVC in boost and buck regions are summarized in Table I.

III. Circuit Implementations of SVC

SVC can be implemented in many different ways with trade-offs in voltage regulation range, control complexity, efficiency, and component count. Fig. 7 shows several circuit implementations of SVC. One can either implement the SVC as an individual partial power converter (Figs. 7a-7c), or merge the SVC into the DPP converter as one extra element (Fig. 7d). Fig. 7a shows a buck SVC which applies to the circumstances where the input voltage is higher than the string voltage of DPP systems. In the case where the input voltage is lower, SVC can be implemented as a boost converter as shown in Fig. 7b. The buck SVC and boost SVC have a very low component count, but they can only regulate the input voltage towards one direction (either up or down).

Fig. 7c is a non-inverting buck-boost SVC that can regulate the input voltage in both directions. It requires more components and more sophisticated control, but it offers a wider regulation range. Fig. 7d shows an SVC topology implemented as an extra port of the DPP converter, where the extra DPP port compensates for the gap between dc bus voltage and stacked string voltage. Input string current is bypassed through the DPP converter. It can either step up or step down the input voltage depending on the designed polarity of the extra port. Voltage regulation of the extra port can be merged with the master controller of the DPP converter. For an extra-port SVC of a fully-coupled DPP converter, the total SVC incurred power processing is exactly the additional differential power. The normalized total SVC incurred power for an extra-port SVC is:

$$\rho_{tot} = \rho_{DPP} = \frac{|V_{IN} - V_{DPP}| \times I_{IN}}{V_{IN} I_{IN}} = |1 - M_v| . \quad (5)$$

To compare different SVC topologies, the component load factor (CLF) that includes the impacts of component count and stress is used as an evaluation metric [35], [36]:

$$CLF = \frac{V^* I^*}{P_{tot}}. \quad (6)$$

V^* is the maximum blocking voltage of switches or the ac average voltage of inductors; I^* is the root-mean-square (RMS) current value of switches and inductors; P_{tot} is the total load power. A lower CLF indicates lower component stress or better utilization of the components. In buck SVC or boost SVC (Figs. 7a-7b), the upper and lower switches (S_1&S_2) are controlled by two complementary gate signals. As for buck-boost converter (Fig. 7c), different control methods exist with trade-offs in driving circuit complexity, inductor size, switch utilization, and converter efficiency [39], [40]. Discussion of buck-boost SVC in this paper is based on the assumption that two switches in each half-bridge are controlled by complementary signals, and the two half-bridges are switching

TABLE II
COMPARISON OF DIFFERENT SVC TOPOLOGIES AND STANDALONE DC-DC REGULATORS

Topologies	Transistor CLF	Inductor CLF	Duty Ratio (D)
Buck SVC	$\frac{(\sqrt{D}+\sqrt{1-D})K_s}{(D-D^2)K_s+D^2}$	$\frac{(1-D)K_s}{(1-D)K_s+D}$	$\frac{M_vK_s}{M_vK_s+1-M_v}$
Boost SVC	$\frac{(\sqrt{D}+\sqrt{1-D})K_s}{1-(1-D)K_s}$	$\frac{(D-D^2)K_s}{1-(1-D)K_s}$	$\frac{M_vK_s+1-M_v}{M_vK_s}$
Buck-Boost SVC	$\frac{(\sqrt{D}+\sqrt{1-D})K_s}{(D-2D^2)K_s+D^2}$	$\frac{(1-D)K_s}{(1-2D)K_s+D}$	$\frac{M_vK_s}{2M_vK_s+1-M_v}$
Buck	$\frac{\sqrt{D}+\sqrt{1-D}}{D}$	$1-D$	M_v
Boost	$\frac{\sqrt{D}+\sqrt{1-D}}{D}$	$1-D$	$\frac{1}{M_v}$
Buck-Boost	$\frac{\sqrt{D}+\sqrt{1-D}}{D(1-D)}$	1	$\frac{M_v}{1+M_v}$

oppositely (i.e., S_1&S_4 or S_2&S_3 are in phase). Define D as the duty ratio of S_1 in the three SVC topologies. The CLF of switches and inductors are calculated and compared across the buck, boost, and buck-boost SVCs. The current ripple is ignored when calculating the current RMS value; power loss is not considered so that $P_{tot} = V_{IN}I_{IN}$. In a buck SVC, the negative terminal of the input and output ports are connected to the negative terminal of the K^{th} domain with voltage as $(1-K_s)V_{DPP}$. To keep the volt-second balancing of the inductor, the duty cycle of buck SVC should satisfy:

$$D \times \underbrace{[V_{IN}-(1-K_s)V_{DPP}]}_{\text{SVC Input Voltage}} = \underbrace{K_sV_{DPP}}_{\text{SVC Output Voltage}} . \quad (7)$$

As a result, the duty ratio of the buck SVC is:

$$D = \frac{M_vK_s}{M_vK_s+1-M_v} \quad (8)$$

In a buck SVC, the blocking voltage of each switch is the SVC input voltage which can be reorganized as $\frac{K_sV_{IN}}{(1-D)K_s+D}$, and the RMS currents of S_1 and S_2 are $\frac{\sqrt{D}}{D}I_{IN}$ and $\frac{\sqrt{1-D}}{D}I_{IN}$ respectively, so the transistor CLF of buck SVC is:

$$\begin{aligned}\text{Transistor CLF} &= \frac{\frac{K_sV_{IN}}{(1-D)K_s+D}\times\left(\frac{\sqrt{D}}{D}I_{IN}+\frac{\sqrt{1-D}}{D}I_{IN}\right)}{V_{IN}I_{IN}} \\ &= \frac{(\sqrt{D}+\sqrt{1-D})K_s}{(D-D^2)K_s+D^2}.\end{aligned} \quad (9)$$

The average voltage of the inductor is $\frac{D(1-D)K_sV_{IN}}{(1-D)K_s+D}$, and the RMS inductor current is $\frac{I_{IN}}{D}$, so the inductor CLF of buck SVC is:

$$\text{Inductor CLF} = \frac{\frac{D(1-D)K_sV_{IN}}{(1-D)K_s+D}\times\frac{I_{IN}}{D}}{V_{IN}I_{IN}} = \frac{(1-D)K_s}{(1-D)K_s+D}. \quad (10)$$

The component load factors and required duty ratios for other SVC topologies are derived and summarized in Table II. Fig. 8 plots the switch and inductor CLFs of the three SVC topologies when $K_s = 0.5$. While the buck-boost SVC has a wider regulation range than the buck SVC and the boost SVC, its switch and inductor CLFs are higher in the full regulation range, as shown in Fig. 8.

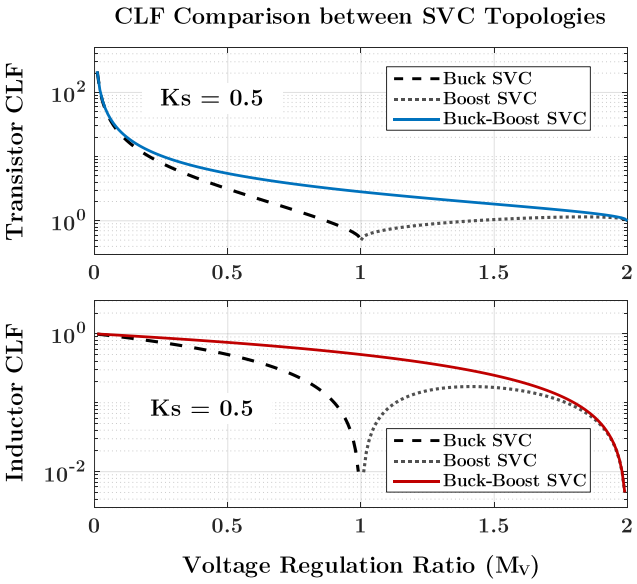


Fig. 8. Transistor and inductor CLFs of different SVC topologies when $K_s = 0.5$, plotted as a function of the voltage regulation ratio M_v.

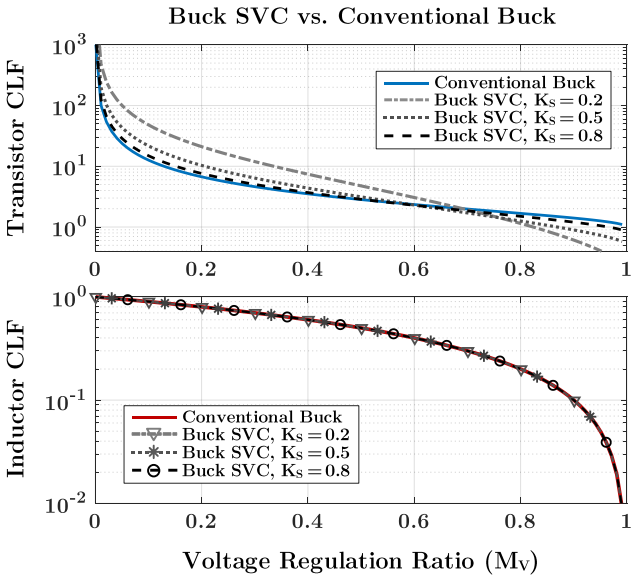


Fig. 9. Transistor and inductor CLF comparison between buck SVC and conventional buck.

In Table II, the CLF and D of the three topologies when implemented as conventional buck, boost, and buck-boost converters are also calculated for comparison. These conventional dc-dc converters compared here are performing the same voltage pre-regulation task as the SVC for the DPP system. Figs. 9–11 plot the switch and inductor CLFs of the three SVC topologies with different K_s values and plot the CLFs of their conventional counterparts as references. As indicated by the figures, for all the three SVC topologies, their CLFs become closer to their counterparts as K_s increases from $0 \rightarrow 1$. If $K_s = 1$, the SVC becomes a standalone dc-dc regulator, processing full power. For the buck SVC, its inductor CLF is always the same as the conventional buck

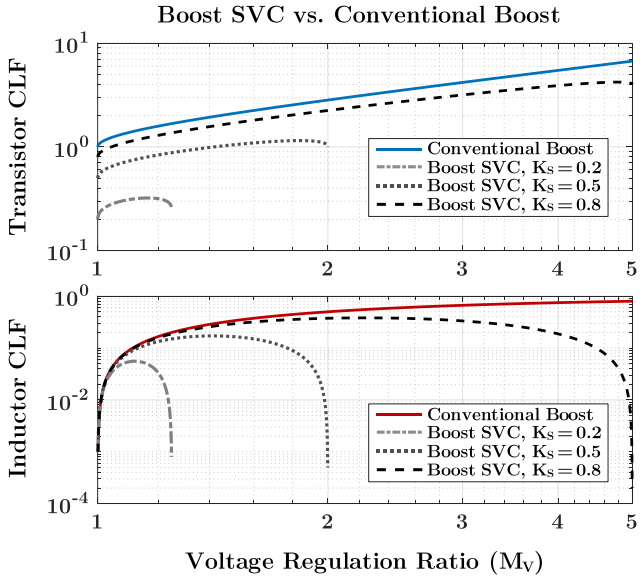


Fig. 10. Transistor and inductor CLF comparison between boost SVC and conventional boost. For each K_s, CLFs of boost SVC are plotted only within the feasible range: $M_v < \frac{1}{1-K_s}$.

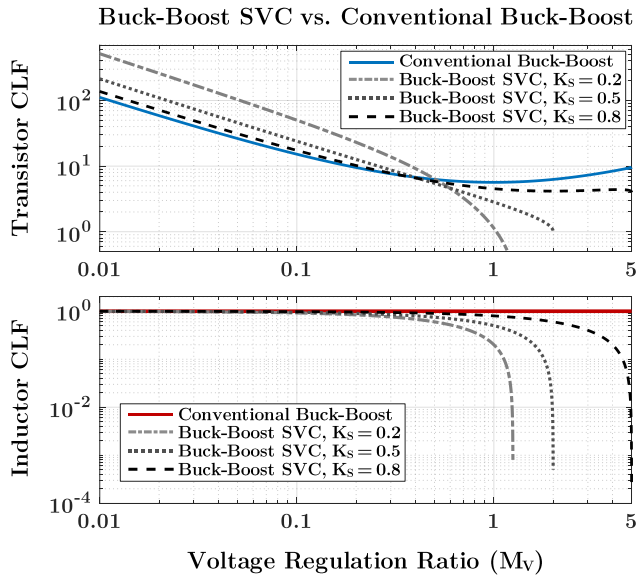


Fig. 11. Transistor and inductor CLF comparison between buck-boost SVC and conventional buck-boost. For each K_s, CLFs of buck-boost SVC are plotted only within the feasible range: $M_v < \frac{1}{1-K_s}$.

converter, but its switch CLF might be higher when M_v is low. For the boost SVC, both its transistor and inductor CLFs are lower than the conventional boost converter in the full regulation range, implying that its component stress is always less than its conventional counterpart. As for the buck-boost SVC, its inductor CLF is always less than the conventional buck-boost converter, but its transistor CLF might be higher if M_v is low, similar to the buck SVC. Regulation ratio (M_v) at the crossing point when transistor CLF of the buck SVC or buck-boost SVC is equal to its conventional counterpart is plotted in Fig. 12. To maintain the advantage in terms of component stress, a buck SVC or buck-boost SVC is suggested

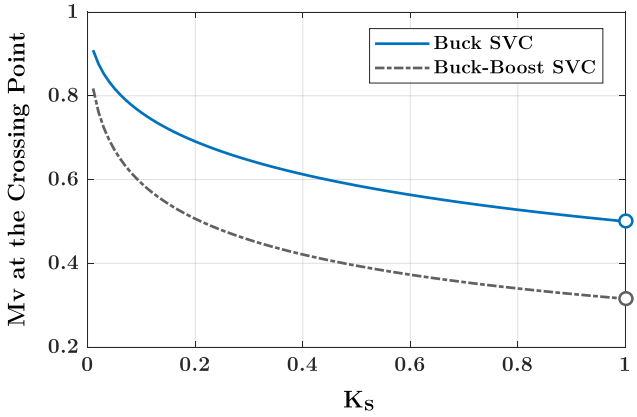


Fig. 12. Regulation ratio (M_v) at the crossing point where transistor CLFs of the SVC topology and its conventional counterpart are equal. The crossing point M_v value is not continuous at $K_s = 1$, where the transistor CLF curves of the SVC and conventional converter will overlap instead of crossing.

to operate in the condition when M_v is larger than the crossing point so that the SVC has lower transistor CLF. One can adjust the number of series domains in the DPP, or change the configuration of SVC to achieve this goal.

IV. A Buck SVC for a 10-Port DPP Converter

To validate the SVC concept, a buck SVC is built and tested with a 10-port ac-coupled DPP converter. The details of the DPP converter are introduced in [16]. Here we focus on the impacts of SVC on the DPP operation. Fig. 13 shows the circuit topology of the buck SVC and the 10-port DPP converter. Ten voltage domains are connected in series and fully-coupled by a multi-winding transformer through half-bridge circuits. The DPP converter functions to balance the differential power among series loads, making the dc bus voltage (V_{DPP}) evenly distributed into ten series-stacked voltage domains. The buck SVC is attached to the first voltage domain with the negative terminals of its input and output ports connected to the negative terminal of the first domain and its switch node linked to the DPP dc bus through a filter inductor. By controlling the duty ratio of the buck SVC, the DPP dc bus voltage can be regulated. Besides input voltage regulation and partial power processing, the buck SVC offers the following additional advantages for DPP system operation:

- *Soft Start*: In a DPP architecture, multiple voltage domains are connected in series to the input side. If the input voltage has a high slew rate at startup, a small power unbalance might cause significant voltage overshoot at some of the series voltage domains, leading to severe damage to the loads in that voltage domain. By adjusting the duty ratio, the buck SVC can control the voltage difference between the input bus and the load, limiting the load voltage slew rate during startup or input transient.
- *Fault Protection*: In fault conditions, the buck SVC can provide fast protection by disabling the upper arm switch and detaching the DPP loads from the input dc bus as shown in Fig. 13.

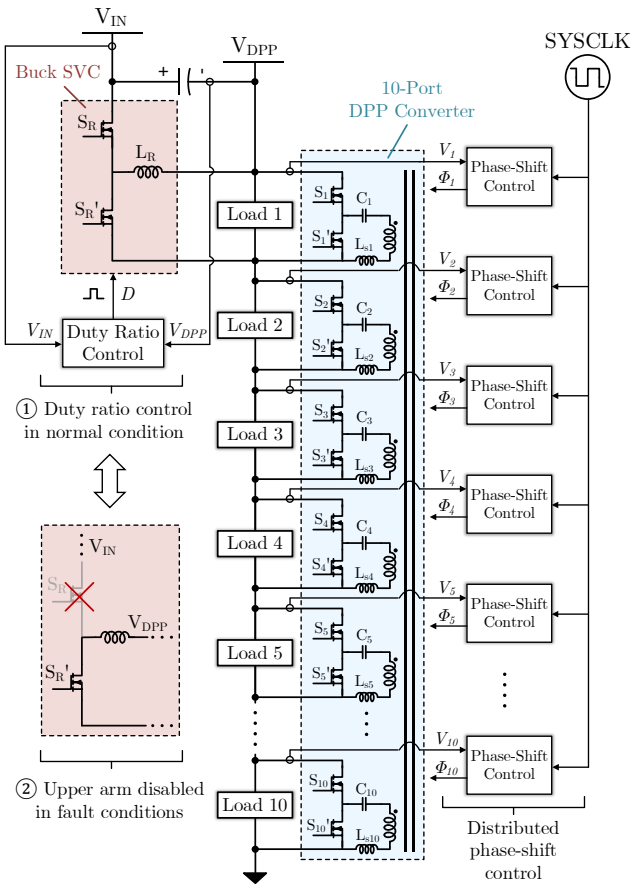


Fig. 13. Circuit topology of a buck SVC attached to a 10-port DPP converter.

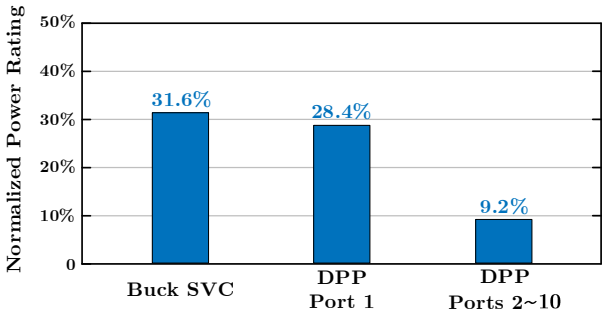


Fig. 14. Normalized power rating of the buck SVC and the 10-port DPP converter. Power ratings are normalized to the maximum system power.

A. Power Rating Design

As indicated in Section II, voltage regulation ratio of the buck SVC needs to follow $M_v > 0.5$, to maintain the total SVC incurred power processing lower than full load power. In addition, to keep the buck SVC component stress lower than a standalone buck converter, M_v should be larger than the crossing point in Fig. 12, which is $M_v > 0.76$ for $K_s = 0.1$ in this design. Considering both the two requirements, the buck SVC is designed to operate in the regulation range of $0.76 < M_v < 1$. Based on the regulation range, we design the power ratings for the buck SVC and the DPP converter. Note that the buck SVC may still function when operating out of this range, but the power rating design for other feasible regulation ranges can follow the discussions below.

Power ratings of the buck SVC and the DPP converter should be designed for their maximum processed power in all operating scenarios. Assume load power of each voltage domain ($P_{load,i}$) is within the range of $[0, P_{\max}]$. The power processed by the buck SVC is

$$P_{SVC} = \rho_{SVC} \times P_{IN} = (1 - 0.9M_v) \times \sum_{i=1}^{10} P_{load,i}. \quad (11)$$

According to (11), the buck SVC processed power reaches maximum when all voltage domains consume $P_{\max}$, and the voltage regulation ratio $M_v = 0.76$. The maximum value is $3.16P_{\max}$, so the buck SVC power rating should be larger than 31.6% of the maximum system load power (i.e., $10P_{\max}$).

In Fig. 13, the buck SVC processed power is only delivered to the first voltage domain, so the power rating requirement for the first DPP port is different from that of the other nine ports. In the first voltage domain, the differential power processed by the DPP converter is

$$P_{DPP,1} = P_{SVC} - P_{load,1} = \rho_{SVC} \sum_{i=1}^{10} P_{load,i} - P_{load,1}. \quad (12)$$

Here, $\rho_{SVC} \in [0.1, 0.316]$ for $M_v \in [0.76, 1]$. Therefore, the maximum differential power processed for the first domain is reached when the first domain consumes zero power and each of the other nine domains consumes $P_{\max}$ at the regulation ratio of $M_v = 0.76$ (i.e., $\rho_{SVC} = 0.316$). The maximum value is $2.84P_{\max}$, so the power rating for DPP port #1 should be larger than 28.4% of the maximum system load power.

As for voltage domains 2∼10, differential power processed by the DPP converter for each voltage domain is

$$\begin{aligned} P_{DPP,m(m\geq 2)} &= \frac{P_{IN} - P_{SVC}}{9} - P_{load,m} \\ &= \frac{1 - \rho_{SVC}}{9} \sum_{i=1}^{10} P_{load,i} - P_{load,m}. \end{aligned} \quad (13)$$

Different from the first voltage domain, the maximum differential power processed by the m^{th} ($m \geq 2$) voltage domain is reached when the m^{th} domain consumes $P_{\max}$ and each of the other nine domains consumes zero power at $M_v = 0.76$. The maximum value is $0.92P_{\max}$, so the power rating for DPP ports #2∼#10 should be larger than 9.2% of the maximum system load power. Fig. 14 shows the normalized power rating requirements for the buck SVC and the 10-port DPP converter. As shown in the figure, the buck SVC can have a significantly reduced power rating compared to the maximum system power. Fig. 14 also indicates that the SVC processed power delivered to the first voltage domain brings additional differential power conversion stress to the DPP converter and increases the power rating requirement for the first DPP port.

B. Control Strategy

In the SVC-DPP architecture, SVC output capacitor and DPP system input capacitor decouple the dynamics of the

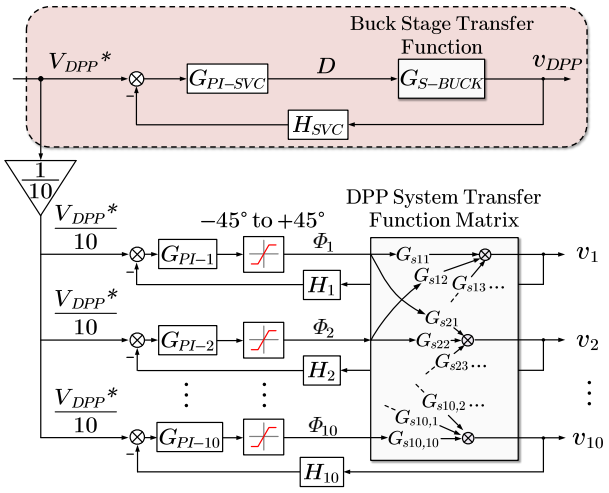


Fig. 15. Block diagram of an example control strategy which enables precise DPP string voltage regulation and rapid differential power balancing.

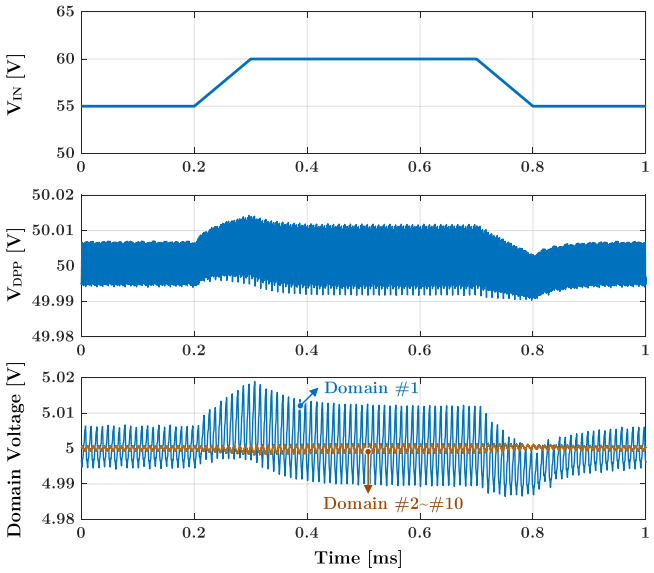


Fig. 16. Simulated waveforms of the regulated DPP string voltage and regulated domain voltages as input bus voltage ramps up and down between 55 V and 60 V. The buck SVC is switching at 500 kHz and the DPP converter is switching at 100 kHz. Inductance values of L_R and L_s as labeled in Fig. 13 are 1.5 μH and 100 nH respectively.

SVC stage and the DPP system, so the buck SVC and the DPP converter can be controlled separately. Existing voltage regulation methods for a buck converter can be easily applied to the buck SVC. Fig. 15 shows one way of implementing the closed-loop control for the buck SVC. The DPP string voltage (V_{DPP}) is regulated by controlling the duty ratio (D) of the buck stage. According to Table II, the regulated DPP string voltage can be formulated as a function of V_{IN} and D:

$$V_{DPP} = \frac{10D}{9D+1} \times V_{IN}. \tag{14}$$

Eq. (14) indicates that the DPP string voltage monotonically increases as the duty ratio increases. Therefore, a PI feedback loop can be applied to regulate the DPP string voltage. The feedback loop adjusts the duty ratio based on the sampled DPP string voltage as shown in Fig. 15. The 10-port DPP converter works as a ten-active-bridge converter, and the power flows among all the ports are controlled by phase-shift modulation. To balance the voltage of series domains, a distributed phase-shift control strategy is applied, where an individual feedback loop is implemented in each domain to control the phase-shift based on the locally measured voltage [41]. The reference DPP string voltage is divided by 10 as the reference voltage for each domain. As shown in Fig. 13, the distributed phase-shift control strategy for the DPP converter can be implemented as multiple phase-shift modules synchronized to a central clock.

A SPICE simulation platform is built to validate the control strategy for the buck SVC and the 10-port DPP converter. In the simulation, the nominal stacked string voltage of the ten series voltage domains is 50 V (5 V for each domain), and the load current of each domain is 5 A. The input dc voltage range is 50 V to 65 V. The buck SVC needs to compensate for the difference between the input dc bus and the nominal DPP string voltage. Fig. 16 shows the simulated voltage waveforms when the input dc bus voltage ramps up and down between 55 V and 60 V. Both the DPP string voltage and voltage of each domain can be regulated with less than 5% voltage ripple at nominal voltages and with a small overshoot during the transient. Since the SVC power is directly delivered to the first voltage domain, domain #1 needs to process higher differential power and has a larger voltage ripple than other domains.

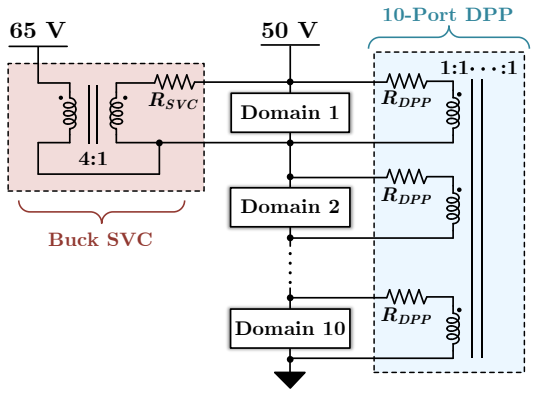


Fig. 17. Equivalent circuit model for Monte Carlo simulation of an SVC-DPP system. Power losses of the buck SVC and the DPP converter are captured by effective output resistance, R_{SVC} and R_{DPP} respectively.

C. Probabilistic Load Distribution and System Efficiency

In the SVC-DPP architecture, power conversion stress and generated power loss are dependent on the load power distribution across series voltage domains. In practical applications, however, load power of each voltage domain might randomly change with time, resulting in unpredictable power distributions. This subsection presents a numerical method of analyzing the performance of the SVC-DPP system with probabilistic load distribution based on Monte Carlo simulations.

Fig. 17 shows the equivalent circuit model of a buck SVC and a fully-coupled 10-port DPP converter. The buck SVC can be modeled as an ideal transformer with an output resistance

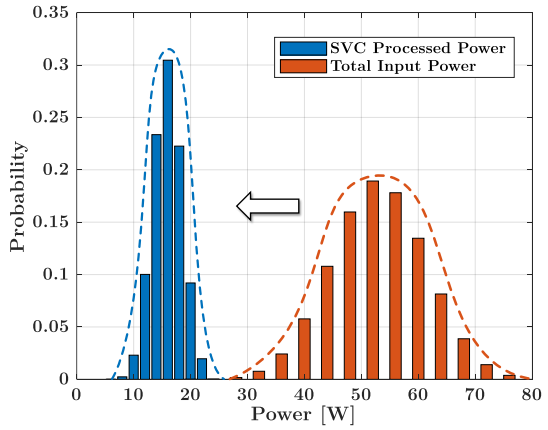


Fig. 18. Probabilistic distribution of the SVC power and total input power.

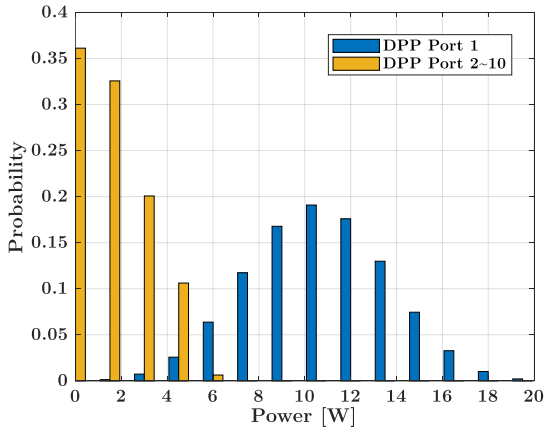


Fig. 19. Probability distribution of the differential power processed by each DPP port. Differential power flow at each port is bidirectional, so its absolute value is plotted here.

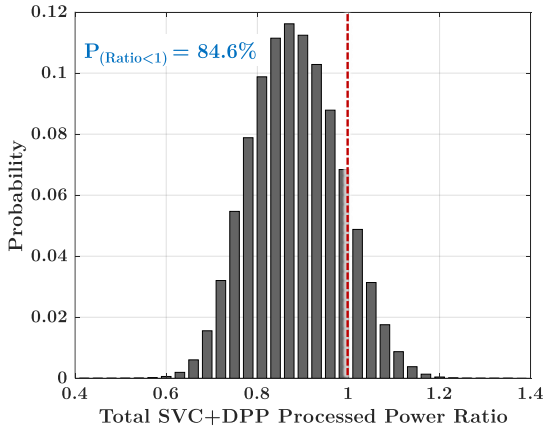


Fig. 20. Probability distribution of the normalized total processed power by SVC and DPP converters $\left(\text{i.e., } \frac{\text{Total SVC + DPP Processed Power}}{\text{Total Load Power}}\right)$. In this Monte Carlo simulation, there is an 84.6% chance that the summed SVC and DPP processed power is lower than total load power.

R_{SVC} capturing the power loss. The 10-port DPP converter can be modeled as a 10-winding transformer of uniform turns ratios and with a R_{DPP} capturing the loss generated at each port. For a symmetric design, R_{DPP} is identical for all the ports. A Monte Carlo simulation of 10,000 iterations is performed based on the circuit model. In the simulation,

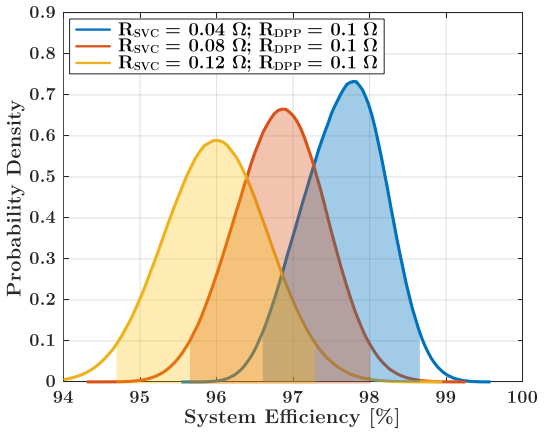


Fig. 21. Probability density distribution of the system efficiency when $R_{DPP} = 0.1\ \Omega$ and $R_{SVC} = 0.04\ \Omega$, $0.08\ \Omega$, and $0.12\ \Omega$ respectively. 95% confidence intervals of the three distributions are marked as shaded areas.

TABLE III
MEAN VALUE AND CONFIDENCE INTERVAL OF THE SYSTEM EFFICIENCY

SVC Output Resistance*	Mean Value	95% Confidence Interval
$R_{SVC} = 0.04\ \Omega$	97.7%	[96.6%, 98.6%]
$R_{SVC} = 0.08\ \Omega$	96.8%	[95.7%, 98.0%]
$R_{SVC} = 0.12\ \Omega$	96.0%	[94.7%, 97.3%]

* $R_{DPP} = 0.1\ \Omega$ in all the three cases.

the buck SVC regulates the 65 V input voltage into 50 V DPP string voltage. The load power of each voltage domain follows a uniform distribution changing between 1 W∼10 W. In every iteration, the total input power, SVC processed power, and the differential power processed at each voltage domain are recorded. Their statistical distributions are plotted in Figs. 18 and 19. In Fig. 18, the overall distribution of the SVC processed power is much lower than that of the total input power, validating that the SVC has a significantly reduced power conversion stress compared to a traditional standalone dc-dc regulator. Fig. 19 plots the distribution of the differential power processed by each DPP port. In general, the differential power processed by DPP port #1 is higher than others, consistent with the conclusions in Section IV-A. Fig. 20 shows the distribution of the normalized total SVC and DPP processed power (normalized to the total load power) in this Monte Carlo simulation, where load power in each domain is uniformly distributed between 1 W∼10 W. In contrast, a conventional buck converter that directly steps down 65 V to 5 V will need to process the total load power. Although the buck SVC increases power stress of the DPP converter, the buck SVC + DPP converter still processes less power than that of conventional buck in most of cases. In a well-designed DPP system where load power has less power variation, the advantage of the SVC + DPP architecture will be more distinct.

To explore the system efficiency (i.e., $\frac{\text{Total Load Power}}{\text{Total Input Power}}$) of the SVC-DPP architecture, we calculate the power loss based on (11) – (13) as well as the modeled output resistance and record the system efficiency in each simulation iteration. Fig. 21 plots the statistical distributions of the system efficiency when

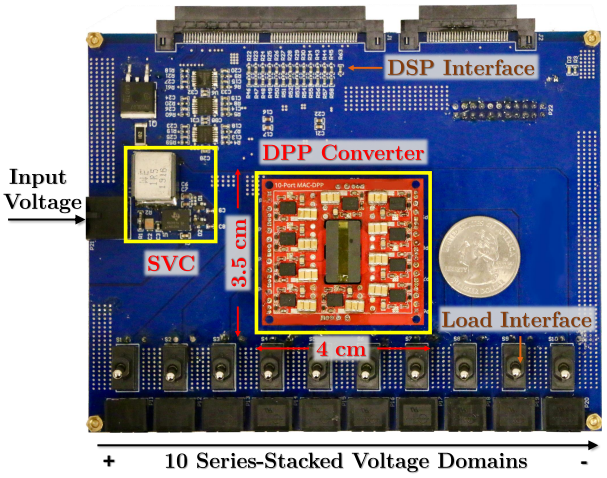


Fig. 22. Prototype of the buck SVC and the 10-port DPP converter in comparison with a US quarter.

TABLE IV
BILL-OF-MATERIAL OF THE PROTOTYPE

Component & Symbol	Description
SVC Half-Bridge Switch, S_R	DrMOS, LMG5200MOFT
SVC Series Inductor, L_R	WE-HCM Shielded, 1.5μH
SVC Switching Frequency, f_{sw}	500 kHz
DPP Half-Bridge Switch, $S_1 \sim S_{10}$	DrMOS, CSD95377Q4M
DPP Blocking Capacitor, $C_1 \sim C_{10}$	Murata X5R, 100 μF $\times$ 3
DPP Series Inductor, $L_{s1} \sim L_{s10}$	Coilcraft SLC7649, 100 nH
DPP Switching Frequency, f_{sw}	100 kHz
DPP Transformer Core	Ferroxcube, ELP18-3C95
DPP Transformer Winding	2 oz single turn per winding

$R_{DPP} = 0.1\ \Omega$ and R_{SVC} increases from 0.04 Ω to 0.12 Ω. Average system efficiencies and 95 % confidence intervals of the three cases are listed in Table III. As shown in the table, after R_{SVC} increases by three times, system efficiency still has over 95% probability to be higher than 94.7%, and its mean value only drops by 1.7%. Performance analysis of SVC-DPP systems with various load probabilistic distributions (e.g., Gaussian, Poisson, Bernoulli, etc.) and other output resistance values can follow the analyzing method presented here.

V. EXPERIMENTAL RESULTS

To experimentally validate the analysis, a buck SVC and a 10-port ac-coupled DPP converter as depicted in Fig. 13 are built and tested. Fig. 22 shows the picture of the buck SVC and DPP converter prototype in comparison with a U.S. quarter. The prototype is designed to support ten series voltage domains with 50 V overall string voltage, and each domain can supply 5-V loads, such as hard disk drives or LEDs, etc. The buck SVC operates to regulate 50 V$\sim$65 V input voltage into 50 V for the DPP system. In this input range, according to (2), the buck SVC only processes 10%$\sim$31% of the overall load power. Board area of the buck SVC is about 1/4 of the DPP converter and is comparable to a U.S. quarter, as shown in Fig. 22. Table IV lists the key component values and parameters of the prototype. Detailed component volume breakdown of the prototype is plotted in Fig. 23. Fig. 24 shows

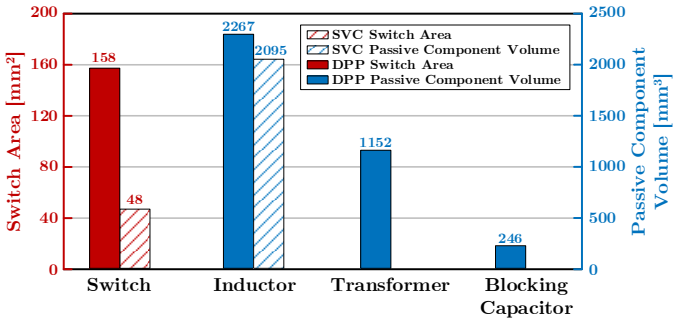


Fig. 23. Component volume breakdown of buck SVC and DPP converter.

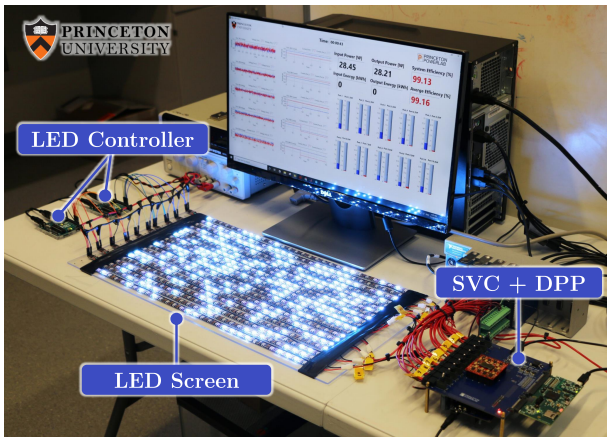


Fig. 24. Picture of an example application. The SVC-DPP is powering a 600-LED screen.

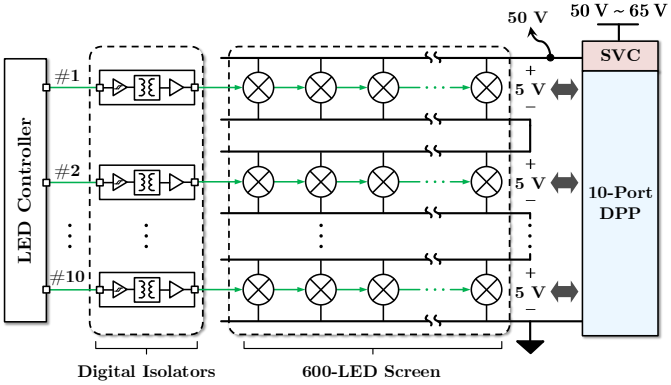


Fig. 25. Power and signal configuration of the LED screen. LEDs in each voltage domain are controlled by one serial signal delivered from LED controller through a digital isolator.

an example application, where the SVC-DPP architecture is powering a 10$\times$60 LED array. The 600 LEDs are evenly divided into ten groups, and LEDs in each group are connected in parallel in one 5-V voltage domain. DPP converter is operated to balance power difference among different LED groups and maintain stable 5 V for each voltage domain. Fig. 25 shows the power and signal configuration of the SVC-DPP system with programmable LED arrays.

Fig. 26 shows the measured steady-state voltage and current waveforms. Here, the input dc bus voltage is 55 V. The buck SVC can effectively compensate for the difference between

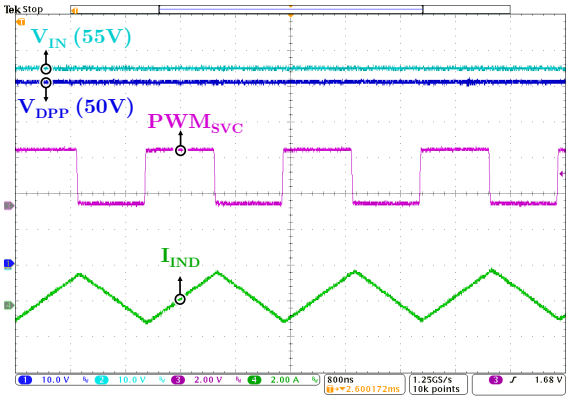


Fig. 26. Measured waveforms of input dc bus voltage, regulated DPP string voltage, and the gate driving signal and inductor current of the buck SVC.

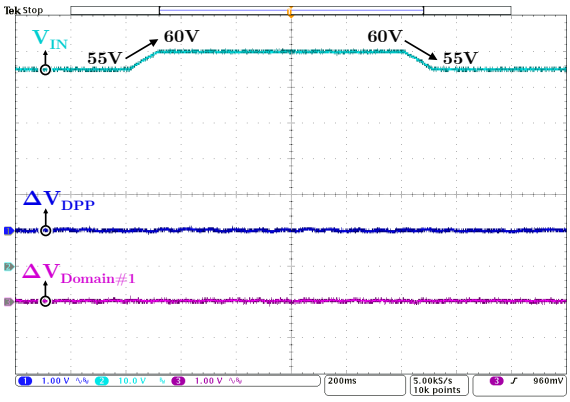


Fig. 27. Measured waveforms of DPP string voltage and the voltage of domain #1 when input voltage ramps up and down between 55 V and 60 V. Input dc bus voltage is measured in dc coupling; DPP string voltage and the voltage of domain #1 are measured in ac coupling.

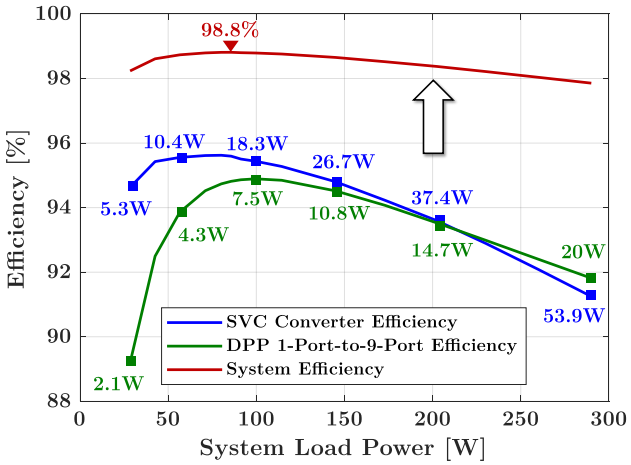


Fig. 28. Measured SVC converter efficiency, 1-port-to-9-port DPP converter efficiency (as defined in [16]) and the system efficiency when SVC converting 55 V input dc bus voltage into 50 V DPP string voltage. The SVC processed power and the DPP processed differential power are labeled along the curves. In this case, the maximum SVC processed power is 53.9 W when the hot spot temperature reaches 90 °C under 110 CFM airflow. Efficiency results are measured with electronic load.

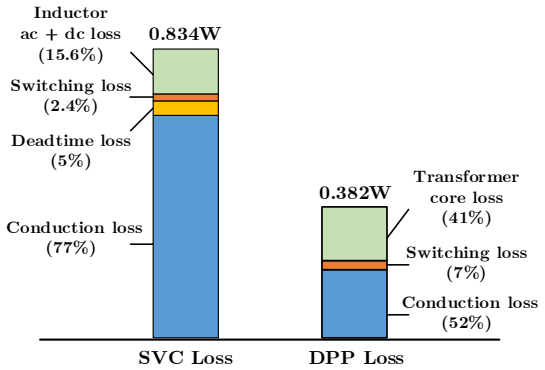


Fig. 29. Power loss breakdown of SVC and DPP converter at 100 W system load power. The labeled conduction loss for SVC converter covers all resistive paths except for inductor winding wire, whose loss is included in inductor ac and dc loss. For DPP converter, the labeled conduction loss covers all resistive paths. Based on the manufacturer's core loss calculation tool (Coilcraft Inductor Analyzer), the DPP inductor (Coilcraft SLC7649S-100nH) core loss at this operating point is negligible and is not included in the graph.

the input voltage and the DPP string voltage, converting 55 V into 50 V for the DPP system. The duty ratio of the buck SVC is 50%, consistent with (14). Fig. 27 shows the regulated DPP string voltage and the voltage of domain #1 during the input voltage ramping transient. Both the DPP string voltage and the voltage of domain #1 maintain stable during the transient, validating the SVC and DPP control strategy.

In SVC-DPP architecture, the DPP converter needs to cope with both the inherent power mismatch of the series loads and the power imbalance caused by SVC. The system efficiency is defined as the total load power divided by the input power. We first only consider the power imbalance caused by SVC by assuming identical load power across series voltage domains. In this case, the system efficiency describes the average performance of the SVC-DPP system with matched average domain load powers. The best-case and worst-case load distributions are discussed later, and the corresponded system efficiencies are plotted to show the upper and lower efficiency limits of the SVC-DPP system.

Figs. 28–30 show the efficiency curves and power loss breakdown in the case of identical domain load powers. Fig. 28 plots the measured SVC converter efficiency, DPP converter efficiency, and the system efficiency when SVC is converting 55 V input voltage into 50 V DPP string voltage. Losses of control and auxiliary circuits are not included here. In the figure, the SVC processed power and the DPP processed differential power are labeled along the curves, and both of them are only a small portion of the total load power, leading to significantly improved system efficiency. As shown in Fig. 28, the maximum SVC processed power at 55 V input voltage is 53.9 W, indicating over 290 W system power according to (2). In Fig. 28, the peak converter efficiency of the buck SVC and DPP converter (measured in the 1-port-to-9-port power delivery case) is around 95%, but the efficiency of the full SVC-DPP system can be much higher, achieving 98.8% peak efficiency at around 80 W load power while losing less than 1 W. Detailed power loss breakdown when SVC converting 55 V to 50 V for the DPP system with 100 W load power is plotted in Fig. 29. In this case, the majority power loss

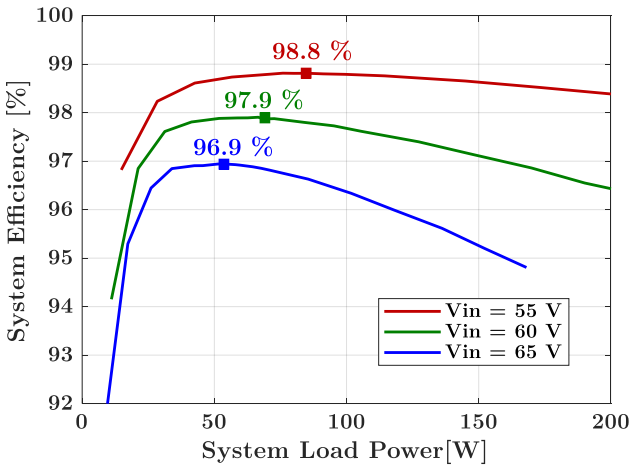


Fig. 30. System efficiency when converting input dc bus voltage from 55 V, 60 V, 65 V into 50 V for DPP system with identical domain load powers. The peak system efficiencies are 98.8%, 97.9%, and 96.9%, respectively.

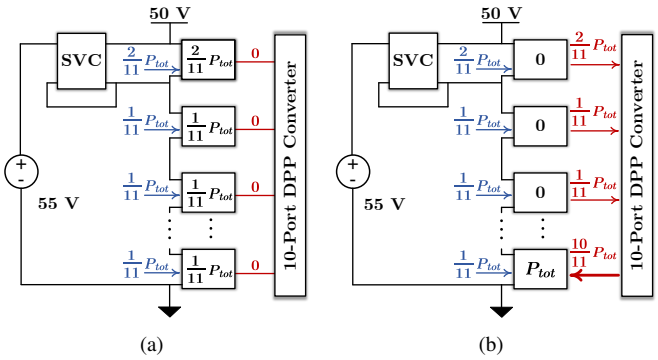


Fig. 31. Load distributions of: (a) best-case system efficiency; (b) worst-case system efficiency. The buck SVC is converting 55 V input voltage into 50 V DPP string voltage.

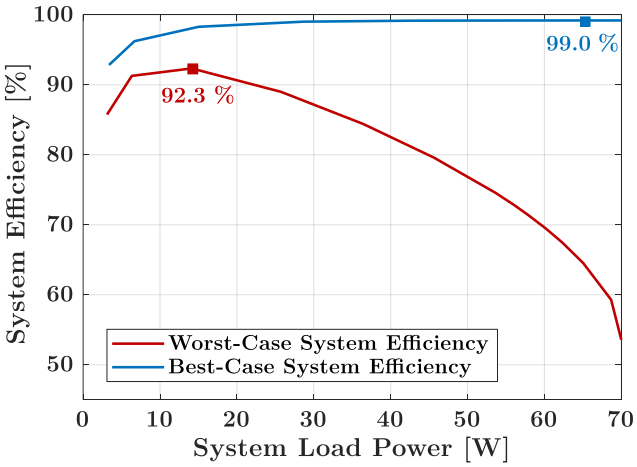


Fig. 32. System efficiency in the best-case and the worst-case load distributions. The buck SVC is converting 55 V input voltage into 50 V DPP string voltage.

of the system is the conduction loss. Fig. 30 plots the system efficiency of different input voltages in the case of identical domain load powers. When the input voltage increases, the voltage regulation ratio M_v decreases. As indicated by Figs. 4 and 5, the power processed by the buck SVC and the DPP converter will increase as M_v decreases, yielding higher loss and lower system efficiency.

To examine the best-case and worst-case load distributions for the system efficiency, both the inherent power mismatch of series loads and power imbalance caused by SVC need to be considered. As indicated by (2), the SVC processed power ratio (ρ_{SVC}) only depends on M_v and K_s. Therefore, in a specific SVC-DPP system (i.e., when M_v and K_s are fixed), SVC processed power and its generated power loss will be determined by the total load power regardless of load distribution. The impacts of load distributions on the total power loss and system efficiency lie in the differential power processing. Fig. 31 shows the load distribution for the best-case and worst-case system efficiencies when SVC is regulating 55 V input voltage to 50 V DPP string voltage. Denote the total load power as P_{tot}, then the SVC processed power is fixed as $\frac{2}{11}P_{tot}$, which is directly delivered to the first voltage domain. In the best-case load distribution, domain #1 consumes $\frac{2}{11}P_{tot}$, and each one of domain #2∼#10 consumes $\frac{1}{11}P_{tot}$, as shown in Fig. 31a. In this case, power of each domain is balanced, so the DPP converter doesn't need to deliver differential power and total power loss is minimized. It is noticeable in Fig. 31a that the best-case load distribution of an SVC-DPP system is different from a conventional DPP system due to the power imbalance caused by SVC. In the worst-case load distribution, domain #1 consumes zero power and one of domain #2∼#10 consumes P_{tot}. Fig. 31b shows one example of the worst-case load distribution, where the total processed differential power and generated power loss are maximal. Fig 32 plots the system efficiency in the best-case and worst-case load distributions. System efficiency curve of any other load distribution will be located in the between. As shown in the figure, the peak system efficiency in the best case reaches 99% and even the worst-case system efficiency can reach 92.3%. In a well-designed DPP system, however, the worst-case load distribution rarely happens.

In summary, the SVC leverages the partial power processing concept and only compensates for the voltage difference between the input voltage and the DPP string voltage. The DPP converter only processes the differential power among the series-stacked voltage domains and inherits natural voltage step-down. An SVC may induce additional power conversion stress to the DPP, and the system should be jointly optimized to achieve optimal performance.

VI. Conclusions

This paper presents the analysis and design of the series voltage compensator for differential power processing. Compared to a standalone dc-dc regulator, the SVC only processes a small fraction of the total load power but may introduce additional stress to the DPP system. A theoretical framework is developed to compare the summation of both the SVC processed power and the additional power conversion stress that SVC brings to the DPP converter to a traditional DPP architecture with a standalone pre-regulator. The operating conditions in which the total SVC incurred power processing is

less than total load power are identified. Several SVC topologies are compared based on their component load factors. A buck SVC converter is designed and applied to a 10-port DPP converter. In addition to improved efficiency and reduced size, the SVC also enables soft-start and fault protection of the DPP system. The theoretical analysis is verified by Monte Carlo simulations in SPICE. Experimental results show that the SVC can effectively regulate the DPP bus voltage with minimum impact on the DPP performance.

REFERENCES

[1] P. Wang and M. Chen, "Series Voltage Compensator for Differential Power Processing," in *Proc. IEEE Energy Convers. Cong. Expo.*, Detroit, MI, USA, 2020, pp. 135-142.

[2] S. T. Hung, D. C. Hopkins and C. R. Mosling, "Extension of Battery Life via Charge Equalization Control," *IEEE Trans. Ind. Electron.*, vol. 40, no. 1, pp. 96-104, Feb. 1993.

[3] H. Schmidt and C. Siedle, "The Charge Equalizer-A New System to Extend Battery Lifetime in Photovoltaic Systems, UPS and Electric Vehicles," in *Proc. IEEE Int. Telecom. Energy Conf.*, Paris, France, 1993, pp. 146-151.

[4] N. H. Kutkut, D. M. Divan and D. W. Novotny, "Charge Equalization for Series Connected Battery Strings," *IEEE Trans. Ind. Appl.*, vol. 31, no. 3, pp. 562-568, May-June 1995.

[5] G. L. Brainard, "Non-dissipative Battery Charger Equalizer," U.S. Patent 5479083, Dec. 26, 1995.

[6] C. Pascual and P. T. Krein, "Switched Capacitor System for Automatic Series Battery Equalization," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 1997, pp. 848-854.

[7] M. Evzelman, M. M. Ur Rehman, K. Hathaway, R. Zane, D. Costinett and D. Maksimovic, "Active Balancing System for Electric Vehicles With Incorporated Low-Voltage Bus," *IEEE Trans. Power Electron.*, vol. 31, no. 11, pp. 7887-7895, Nov. 2016.

[8] M. Liu, Y. Chen, Y. Elasser and M. Chen, "Dual Frequency Hierarchical Modular Multilayer Battery Balancer Architecture," *IEEE Trans. Power Electron.*, vol. 36, no. 3, pp. 3099-3110, March 2021.

[9] T. Shimizu, M. Hirakata, T. Kamezawa and H. Watanabe, "Generation Control Circuit for Photovoltaic Modules," *IEEE Trans. Power Electron.*, vol. 16, no. 3, pp. 293-300, May 2001.

[10] C. Olalla, D. Clement, M. Rodriguez and D. Maksimovic, "Architectures and Control of Submodule Integrated DC-DC Converters for Photovoltaic Applications," *IEEE Trans. Power Electron.*, vol. 28, no. 6, pp. 2980-2997, June 2013.

[11] J. T. Stauth, M. D. Seeman, and K. Kesarwani, "Resonant Switched-Capacitor Converters for Sub-Module Distributed Photovoltaic Power Management," *IEEE Trans. Power Electron.*, vol. 28, no. 3, pp. 1189–1198, March 2013.

[12] P. S. Shenoy, K. A. Kim, B. B. Johnson and P. T. Krein, "Differential Power Processing for Increased Energy Production and Reliability of Photovoltaic Systems,"*IEEE Trans. Power Electron.*, vol. 28, no. 6, pp. 2968-2979, June 2013.

[13] S. Qin, S. T. Cady, A. D. Domínguez-García and R. C. N. Pilawa-Podgurski, "A Distributed Approach to Maximum Power Point Tracking for Photovoltaic Submodule Differential Power Processing," *IEEE Trans. Power Electron.*, vol. 30, no. 4, pp. 2024-2040, April 2015.

[14] K. A. Kim, P. S. Shenoy and P. T. Krein, "Converter Rating Analysis for Photovoltaic Differential Power Processing Systems," *IEEE Trans. Power Electron.*, vol. 30, no. 4, pp. 1987-1997, April 2015.

[15] Y. Jeon, H. Lee, K. A. Kim and J. Park, "Least Power Point Tracking Method for Photovoltaic Differential Power Processing Systems," *IEEE Trans. Power Electron.*, vol. 32, no. 3, pp. 1941-1951, March 2017.

[16] P. Wang, Y. Chen, J. Yuan, R. C. N. Pilawa-Podgurski and M. Chen, "Differential Power Processing for Ultra-Efficient Data Storage," *IEEE Trans. Power Electron.*, vol. 36, no. 4, pp. 4269-4286, April 2021.

[17] E. Candan, P. S. Shenoy and R. C. N. Pilawa-Podgurski, "A Series-Stacked Power Delivery Architecture with Isolated Differential Power Conversion for Data Centers," *IEEE Trans. Power Electron.*, vol. 31, no. 5, pp. 3690-3703, May 2016.

[18] A. Stillwell and R. C. N. Pilawa-Podgurski, "A Resonant Switched-Capacitor Converter with GaN Transistors for Series-Stacked Processors with 99.8% Power Delivery Efficiency," in *Proc. IEEE Energy Convers. Cong. Expo.*, 2015, pp. 563–570.

[19] P. S. Shenoy and P. T. Krein, "Differential Power Processing for DC Systems," *IEEE Trans. Power Electron.*, vol. 28, no. 4, pp. 1795-1806, April 2013.

[20] R. M. Button, "An Advanced Photovoltaic Array Regulator Module," in *Proc. Intersociety Energy Convers. Eng. Conf.*, Washington, DC, USA, 1996, pp. 519-524 vol.1.

[21] J. H. R. Enslin and D. B. Snyman, "Combined low-cost, high-efficient inverter, peak power tracker and regulator for PV applications," *IEEE Trans. Power Electron.*, vol. 6, no. 1, pp. 73-82, Jan. 1991.

[22] B. Min, J. Lee, J. Kim, T. Kim, D. Yoo and E. Song, "A New Topology with High Efficiency Throughout All Load Range for Photovoltaic PCS," *IEEE Trans. Ind. Electron.*, vol. 56, no. 11, pp. 4427-4435, Nov. 2009.

[23] M. H. Ahmed, C. Fei, F. C. Lee and Q. Li, "Single-Stage High-Efficiency 48/1 V Sigma Converter With Integrated Magnetics," *IEEE Trans. Ind. Electron.*, vol. 67, no. 1, pp. 192-202, Jan. 2020.

[24] H. Chen, H. Kim, R. Erickson and D. Maksimović, "Electrified Automotive Powertrain Architecture Using Composite DC-DC Converters," *IEEE Trans. Power Electron.*, vol. 32, no. 1, Jan. 2017.

[25] J. Zhao, K. Yeates and Y. Han, "Analysis of High Efficiency DC/DC Converter Processing Partial Input/Output Power," in *Proc. IEEE Workshop Control Model. Power Electron.*, Salt Lake City, 2013.

[26] H. Zhou, J. Zhao and Y. Han, "PV Balancers: Concept, Architectures, and Realization," *IEEE Trans. Power Electron.*, vol. 30, no. 7, pp. 3479-3487, July 2015.

[27] E. Moore and T. Wilson, "Basic considerations for DC to DC conversion networks," *IEEE Trans. Magn.*, vol. 2, no. 3, pp. 620-624, September 1966.

[28] J. A. Cobos, H. Cristóbal, D. Serrano, R. Ramos, J. A. Oliver and P. Alou, "Differential power as a metric to optimize power converters and architectures," in *Proc. IEEE Energy Convers. Cong. Expo.*, 2017, pp. 2168-2175.

[29] C. Li and J. A. Cobos, "Classification of Differential Power Processing Architectures Based on VA Area Modeling," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, to be published.

[30] J. W. Zapata, S. Kouro, G. Carrasco, H. Renaudineau and T. A. Meynard, "Analysis of Partial Power DC–DC Converters for Two-Stage Photovoltaic Systems," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 1, pp. 591-603, March 2019.

[31] C. Li, Y. E. Bouvier, A. Berrios, P. Alou, J. A. Oliver and J. A. Cobos, "Revisiting 'Partial Power Architectures' from the 'Differential Power' Perspective," in *Proc. IEEE Workshop Control Model. Power Electron.*, Toronto, ON, Canada, 2019, pp. 1-8.

[32] F. Xue, R. Yu and A. Huang, "A Family of Ultra-High Efficiency Fractional DC-DC Topologies for High Power Energy Storage Device," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 2, pp. 1420-1427, April 2021.

[33] M. Shousha, T. McRae, A. Prodić, V. Marten and J. Milios, "Design and Implementation of High Power Density Assisting Step-Up Converter with Integrated Battery Balancing Feature," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 5, no. 3, pp. 1068-1077, Sept. 2017.

[34] C. Liu, D. Li, Y. Zheng and B. Lehman, "Modular Differential Power Processing (mDPP)," in *Proc. IEEE Workshop Control Model. Power Electron.*, Stanford, CA, 2017, pp. 1-7.

[35] B. Carsten, "Converter Component Load Factors - A Performance Limitation of Various Topologies," in *Proc. PCI*, Munich, Germany, 1988, pp. 31–49.

[36] M. Kasper, D. Bortis and J. W. Kolar, "Classification and Comparative Evaluation of PV Panel-Integrated DC–DC Converter Concepts," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2511-2526, May 2014.

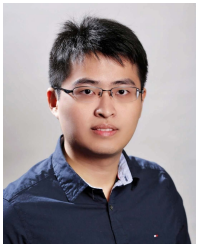
[37] P. Wang, R. C. N. Pilawa-Podgurski, P. T. Krein and M. Chen, "Stochastic Power Loss Analysis of Differential Power Processing," *IEEE Trans. Power Electron.*, vol. 37, no. 1, pp. 81-99, Jan. 2022.

[38] M. Kasper, D. Bortis, and J. W. Kolar, "Unified Power Flow Analysis of String Current Diverters," *Electr. Eng.*, vol. 100, no. 3, pp. 2085-2094, Sep. 2018.

[39] R. W. Erickson and D. Maksimovic, "Section 6.1.2: Cascade Connection of Converters," in *Fundamentals of Power Electronics*. Norwell, MA: Kluwer, 2001.

[40] Y. Lee, A. Khaligh, A. Chakraborty and A. Emadi, "Digital Combination of Buck and Boost Converters to Control a Positive Buck–Boost Converter and Improve the Output Transients," *IEEE Trans. Power Electron.*, vol. 24, no. 5, pp. 1267-1279, May 2009.

[41] P. Wang, Y. Chen, Y. Elasser and M. Chen, "Small Signal Model for Very-Large-Scale Multi-Active-Bridge Differential Power Processing (MAB-DPP) Architecture," in *Proc. IEEE Workshop Control Model. Power Electron.*, Toronto, ON, Canada, 2019, pp. 1-8.



Ping Wang (Student Member, IEEE) received the B.S. degree in electrical engineering from Shanghai Jiao Tong University, Shanghai, China, in 2017, and the M.A. degree in electrical engineering in 2019 from Princeton University, NJ, USA, where he is currently working toward the Ph.D. degree.

His research interests include high-efficiency/ high-density power converters, multiport dc-dc converters, and high-performance power electronics design for data center applications.

Mr. Wang received the Second Place Prize Paper Award of the IEEE Transactions on Power Electronics in 2020, two National Scholarship Awards in 2014 and 2016 at Shanghai Jiao Tong University, the First Place Award of the 2019 IEEE ECCE Best Student Project Demonstration, and the First Place Award from the Innovation Forum of Princeton University in 2019.

Minjie Chen (Senior Member, IEEE) received the B.S. degree from Tsinghua University, Beijing, China, in 2009, and the S.M., E.E., and Ph.D. degrees from Massachusetts Institute of Technology (MIT), Cambridge, MA, USA, in 2012, 2014, and 2015, respectively. He is an Assistant Professor of Electrical and Computer Engineering and Andlinger Center for Energy and the Environment at Princeton University, where he leads the Princeton Power Electronics Research Lab. His research interests include complex power architecture, power magnetics, control, and machine learning methods for high performance power electronics.

Dr. Chen received three IEEE Transactions Prize Paper Awards, a COMPEL Best Paper Award, the NSF CAREER Award, a Dimitris N. Chorafas Award for outstanding MIT Ph.D. Thesis, an Outstanding Reviewer Award from IEEE Transactions on Power Electronics, two ECCE Best Demonstration Awards, multiple APEC Outstanding Presentation Awards, a Siebel Energy Institute Research Award, a C3.ai DTI Research Award, and the First Place Award from the Innovation Forum of Princeton University. He was included in the Princeton Engineering Commendation List for Outstanding Teaching. He holds 6 U.S. patents. He is the Vice Chair of IEEE PELS Technical Committee on Design Methodologies (TC10), Associate Editor of IEEE Transactions on Power Electronics, Associate Editor of IEEE Journal of Emerging and Selected Topics in Power Electronics, Associate Technical Program Committee Chair of IEEE Energy Conversion Congress and Exposition (ECCE) in 2019, Student Activity Chair of IEEE Energy Conversion Congress and Exposition (ECCE) in 2020, and the Technical Program Committee Chair of IEEE International Conference on DC Microgrids (ICDCM) in 2021.