A 3kW Two-Stage Transformerless PV Inverter with Resonant DC Link and ZVS-PWM Operation

Yenan Chen, *Member, IEEE,* Minjie Chen, *Senior Member, IEEE,* and Dehong Xu *Fellow, IEEE*

***Abstract*—Photovoltaic (PV) inverters play important roles in renewable energy integration. Reducing the switching loss is a main challenge in improving the efficiency and power density. This paper presents the design, implementation, and field test of a 3 kW two-stage commercial-ready transformerless PV inverter with resonant dc link and ZVS-PWM operation. The ZVS-PWM operation periodically resonates the dc link voltage of the inverter to zero for ZVS of the inverter switches, which enables higher switching frequency and significantly reduced magnetic component size. A 30 kW distributed PV system comprising ten ZVS-PWM PV inverters was built and tested for more than 100 days to evaluate the long-term performance of the PV inverter. The key figure-of-merits for grid-interface operation, such as efficiency, power density, total harmonic distortion (THD), leakage current, are measured, analyzed, and reported.**

***Index Terms*—photovoltaic, inverter, zero-voltage-switching (ZVS), renewable energy, resonant dc link.**

I. Introduction

DISTRIBUTED PV generation systems contribute more than 36% of the global total solar installation growth between 2012 to 2018 [1]. As the interface between the renewable energy source and the utility grid, PV inverter is a key component of the distributed PV system. PV inverters with power level below 5 kW usually use single-phase dc-ac topology for residential roof-top applications. Transformerless architecture is one of the most popular solutions for single-phase residential-level PV inverters due to its simplicity and higher efficiency compared to a transformer-based solution [2].

The transformerless architecture shown in Fig. 1 usually includes a first dc-dc stage and a second dc-ac stage decoupled by the dc-link bus capacitor. The dc-dc stage is used to boost the voltage and perform maximum-power-point-tracking (MPPT), which can extract more power from PV panels. The peak efficiency of a continuous current mode (CCM) boost converter can be 99% if the PV voltage is close to the dc-link voltage. Some PV inverter manufacturers also use the zero-voltage-transition (ZVT) boost converter [3] to relief the thermal stress of the switching devices. The second dc-ac stage usually determines the overall efficiency and power density of the entire system since it operates across a wider range throughout the day, and perform more sophisticated functions.

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Yenan Chen and Minjie Chen are with the Department of Electrical Engineering and Andlinger Center for Energy and the Environment at Princeton University, Princeton, NJ, 08540, USA. e-mail: {yenanc, minjie}@princeton.edu.

Dehong Xu is with the Department of Electrical Engineering at Zhejiang University, Hangzhou, Zhejiang, 310027, China. e-mail: xdh@cee.zju.edu.cn.

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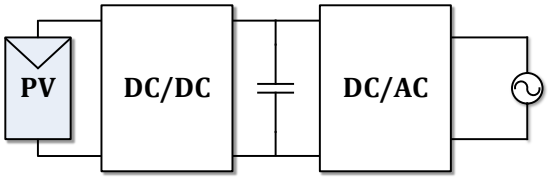

Fig. 1. A two-stage transformerless architecture for single-phase PV inverter including a dc-dc stage and a dc-ac stage. The dc-dc stage performs maximum power point tracking, and the dc-ac stage performs grid interface.

Existing work in the dc-ac grid-interface stage mainly focuses on the common-mode leakage current issue of the non-isolated PV systems. The high frequency common-mode voltage of PV inverter is the source of the leakage current. The parasitic capacitance between PV panels to ground creates a path for the leakage current [4], [5]. One major solution to reduce the leakage current is to create a constant dc common-mode voltage for the PV inverter. In a full-bridge inverter, high frequency common-mode voltage is inevitable with unipolar pulse-width-modulation (PWM). Bipolar PWM can guarantee a constant common-mode voltage but it reduces the efficiency and power quality due to higher current ripple on the ac filter. Many variants of the full-bridge dc-ac topology have been investigated, including [4]–[13]. The common-mode voltage can be clamped at a constant level with extra switching devices. The H5 [6], H6 [7] and HERIC [8] topologies are among the most popular solutions and have been commercialized by numerous PV inverter manufactures. Another solution is to implement common-ground connection between dc input and ac output to bypass the leakage current [14]–[16]. Full-bridge inverters with special common-mode filter design [17], [18] can also reduce the leakage current.

These aforementioned topologies are all hard-switching topologies. Their switching frequencies are usually below 20 kHz. The switching loss of the semiconductor devices limits the overall system efficiency and power density. Resonant techniques have been applied to the dc bus or a single switch [19]–[25] to create soft-switching opportunities. The resonant dc-link inverter is a well-known zero-voltage-switching (ZVS) topology with low additional component count [19]. ZVS-PWM technology have been applied to the full-bridge grid inverter [26], [27] and three-phase dc-ac inverter [28] based on the resonant dc-link concept. The ZVS-PWM technology brings the advantages of reduced switching loss, smaller magnetic components and low total harmonics distortion (THD) with PWM control. The common-mode characteristic of the full-bridge inverter with ZVS-PWM and a common-mode filter

TABLE I
TECHNICAL SPECIFICATIONS OF THE ZVS PV INVERTER

Specifications	Description
Power rating	3 kW
Max. / rated input voltage	450 / 360 V
MPPT range	150 – 450 V
Self power-up voltage	60 V
Nominal ac voltage / range	230 Vac $\pm 15\%$
Nominal ac current (I_{rms})	13A
Ac frequency range	49.5 – 50.2 Hz
Power factor (PF, $\cos\phi$)	0.95 lagging – 0.95 leading
THD	$< 3\%$
Dc current injection	$< 0.5\% I_{rms}$
Self consumption (at night)	<5 W
Max. / Euro Efficiency	98.3% / 98%
Topology	Transformerless
Cooling method	Natural convection

design are presented in [29] for the potential application in PV systems. The safety operation [30], [31], the power quality improvement [32] and control strategy in rectification mode [33] for the ZVS-PWM inverter have been studied.

This paper presents the design, implementation, and field test of a 3 kW two-stage transformerless PV inverter with the ZVS-PWM technology, including the circuit topology, ZVS-PWM control, hardware design, and long-term field test. To the best of the authors' knowledge, it is the first time the resonant dc-link ZVS technology is applied to low-power single-phase PV inverters. The ZVS-PWM technology greatly reduces the switching loss of the dc-ac stage. The following advantages are experimentally verified: 1) higher efficiency; 2) higher switching frequency (100 kHz) for silicon semiconductor devices; 3) smaller size for both differential-mode (DM) filters and common-mode (CM) filters; 4) smaller heat sink to reduce the total weight of the PV inverter. A 30 kW distributed PV system with ten 3 kW ZVS PV inverters was built for the field test. The field test was conducted for 107 days in six months. The efficiency, power quality (THD, power factor), safety and protection functions (leakage current, dc current injection, utility voltage disturbances and frequency disturbances) of the ZVS PV inverter have been rigorously documented. The ZVS PV inverter is ready for commercial adoption in utility interfaced rooftop PV applications.

II. SYSTEM OVERVIEW

Table. I lists the key specifications of the ZVS PV Inverter. The input voltage and MPPT range are the most typical values for a 3 kW PV inverter. Other specifications like ac voltage/frequency range, power factor and THD are the mandatory requirements of certification standards. Fig. 2 shows the topology of the power stage of the 3 kW ZVS PV inverter. It is a two-stage transformerless topology with a two-phase interleaved boost converter and a ZVS dc-ac converter. The CM filters are installed on both the dc input side and ac output side. A flyback converter provides the power for the gate drivers, microcontroller, sensors and relays. The first dc-dc stage is a typical hard-switching boost converter. The interleaved configuration can reduce the current ripple of PV panels. The boost converter will cut in and step up the dc

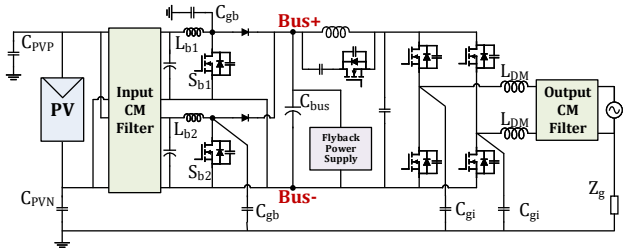

Fig. 2. The circuit schematic of the 3kW ZVS PV inverter with parasitic capacitance to ground.

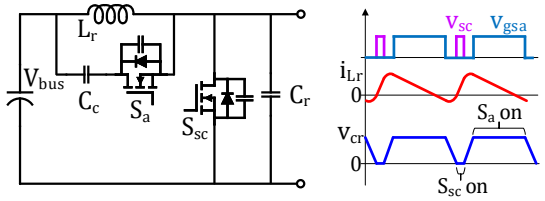

Fig. 3. Basic principle of the resonant dc link with active clamping.

bus voltage of the PV inverter when the PV voltage drops below the rated input voltage. At this time, the boost converter regulates the PV output voltage to realize MPPT while the downstream dc-ac inverter controls the dc bus voltage. The boost switches will be turned off and the MPPT will be performed by the dc-ac stage when the PV voltage is equal to or higher than the rated input voltage. so that the efficiency of the boost stage is not included in the rated overall efficiency. A parallel diode with low forward voltage can bypass the boost inductor and boost diode for lower voltage drop. We focus on the design of the dc-ac stage to improve the efficiency and enhance the grid-interface performance. The ZVS-PWM technology is used in this 3kW residential PV inverter.

A. Principle of ZVS-PWM

As shown in Fig. 2, the ZVS-PWM technology requires additional resonant circuit including the resonant inductor L_r, resonant capacitor C_r, clamping capacitor C_c and active-clamping switch S_a. The resonant capacitor C_r can also act as the snubber capacitor for the inverter. Fig. 3 illustrates the principle of the resonant dc link with active clamping. S_a and S_{sc} are controlled by a pair of complementary gate driver signals (v_{gsa} and v_{sc}). When S_a is on and S_{sc} is off, the voltage of the resonant capacitor is clamped to $V_{dc} + V_{cc}$ where V_{cc} is the voltage of the clamping capacitor. In contrast, the voltage of the resonant capacitor is clamped to zero. The voltage transition of C_r is performed by the resonance between L_r and C_r during the dead-time between v_{gsa} and v_{sc}. ZVS-on can be achieved for both S_a and S_{sc} if the resonant process is completed within the dead-time. The inverter switches realize ZVS-commutation when the dc link voltage of the inverter (same as v_{cr}) is clamped to zero.

It is possible to achieve ZVS for every switching commutation with the resonant dc link mechanism but the loss of the resonant stage will increase. In fact, the resonant dc link stage is only activated during selected switching commutations

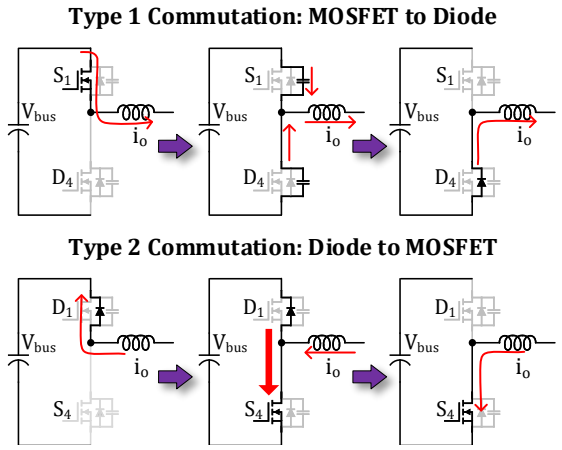

Fig. 4. Two types of switching commutations in hard-switching inverters: Type 1 commutation is from MOSFET to body-diode and Type 2 commutation is from body-diode to MOSFET.

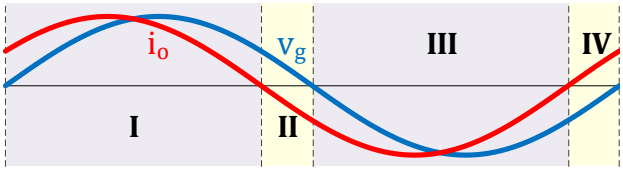

Fig. 5. The output current is leading the grid voltage. The switching action of turning off S_1 then turning on S_4 is Type 1 commutation in Zone I, IV and Type 2 commutation in Zone II, III.

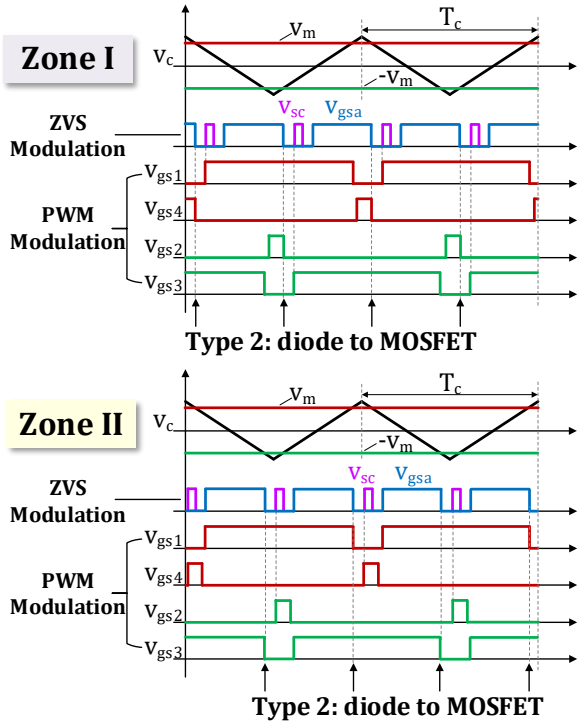

Fig. 6. The control signals of the resonant circuit and the PWM signals of the full-bridge inverter in Zone I and Zone II of the positive half cycle of utility grid.

considering the loss balancing between the inverter stage and the resonant dc link stage. Fig. 4 shows two types of switching commutations in hard-switching inverters: Type 1 commutation is from MOSFET to body-diode and Type 2 commutation is from body-diode to MOSFET. In Type 1 commutation the MOSFET (S_1) is normally quasi-ZVS-off because of the voltage rise delay caused by the nonlinear output capacitance [34]. The complementary MOSFET (S_4) is naturally ZVS-on due to the pre-conducting of its body-diode (D_4). In Type 2 commutation the body-diode (D_1) is forced off with reverse recovery phenomenon, which causes high current spike and high switching loss. Thus, the resonant dc link mechanism is chosen to reduce the switching loss of type 2 commutation.

The commutation types can be different with opposite current direction even if the gate driver signals are the same. In Fig. 5, the output current is leading the grid voltage and one line cycle is divided into four zones. The commutation from S_1 to S_4 is Type 1 with positive output current (Zone I, IV) and Type 2 with negative output current (Zone II, III). The key principle of ZVS-PWM is to identify the type of switching commutations and synchronize the resonant operation to the Type 2 commutations. Fig. 6 shows the control signals of the resonant circuit and the PWM signals of the full-bridge inverter in Zone I and Zone II with output current leading the grid voltage. The inverter switches are controlled by the hybrid unipolar PWM: two inverter phases are controlled by two modulation waves with a 180° phase-shift respectively. The switching actions of S_a and S_{sc} are chosen to synchronize the Type 2 commutations ($S_4 \rightarrow S_1$ and $S_2 \rightarrow S_3$ in Zone I, $S_1 \rightarrow S_4$ and $S_3 \rightarrow S_2$ in Zone II). The switching frequency of S_a is twice of the carrier frequency (f_c).

According to the grid requirements, single-phase residential PV inverters are normally required to operate at unity power factor to maximize the solar energy generation [35]. In inverter mode with unity power factor, Zone II and Zone IV do not exist. The ZVS-PWM control signals for Zone I and Zone III are used. In rectifier mode with unity power factor, only the control signals for Zone II and Zone IV are needed. Detailed analysis and experiment results of the ZVS inverter in these two modes have been published in [27], [33] respectively.

Due to the increasing adoption of PV generation systems, low power single-phase PV inverters are been expected to support the grid with the reactive power capability [36]. This topology is also possible to operate in the reactive power mode which is the combination of inverter mode and rectifier mode. The ZVS-PWM control signals for Zone I - Zone IV are needed and switched in one line cycle. The authors have proposed a ZVS-PWM strategy for three-phase grid inverters with an arbitrary power factor [37]. The results of single-phase ZVS inverter with reactive power capability will be published in the future.

The resonant dc link stage and the inverter stage can be further merged to simplify the circuit and control. S_{sc} in Fig. 3 can be removed and its clamping function can be implemented by simultaneously turning on all the four inverter switches. The circuit topology and the ZVS-PWM block of the ZVS inverter are given in Fig. 7. The ZVS-PWM block is implemented by the microcontroller (TMS32F28069). The

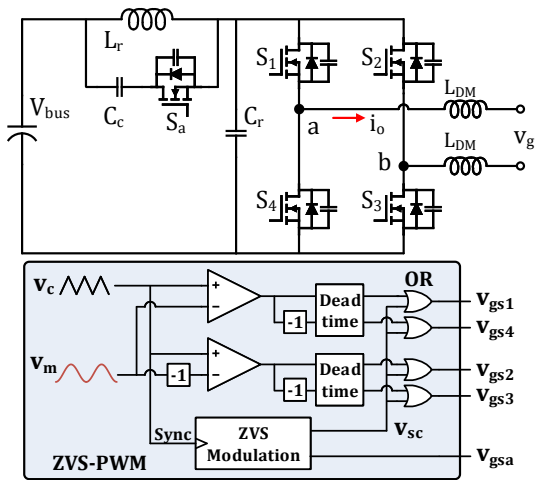

Fig. 7. The circuit topology and the ZVS-PWM block of the ZVS inverter merged with the resonant dc link stage.

control signal v_{sc} is merged to the PWM signals v_{gs1}–v_{gs4} by the "OR" logic gates.

B. Advantages of ZVS PV Inverter

Silicon MOSFET is not applicable for most commercial-level hard-switching PV inverters because of the high reverse current of its body-diode. As the most used device in PV inverters, IGBT has better anti-parallel diode but slower switching speed and higher voltage drop with low current. With ZVS-PWM control, the body-diode of MOSFET is turned off with low di/dt and its reverse recovery current is greatly reduced, enabling MOSFET being used in the ZVS PV inverter without the risk of failure. The ZVS-PWM brings following advantages:

1) ***Higher efficiency***. The commutations from body-diode to MOSFET in the dc-ac stage are completed when the dc link voltage is clamped at zero. Thus, the MOSFET is ZVS-ON without switching loss. The commutations from MOSFET to body-diode do not require extra resonant action of the dc link because they are naturally ZVS-on. The active clamping switch S_a is also ZVS-on. The dc-ac stage only has the turn-off loss of MOSFETs. The total semiconductor loss of the dc-ac stage can be reduced by 50%.
2) ***Smaller magnetic components***. The carrier frequency (f_c) of the ZVS dc-ac stage is 50 kHz and the ripple frequency on the DM filters (L_{DM}) is 100kHz with hybrid unipolar PWM. The inductance of L_{DM} can be reduced by 80% comparing to the hard-switching topologies with switching frequency below 20 kHz. The high switching frequency is also beneficial for the CM filter design. Fig. 8 shows the experimental waveform of the CM voltage ($v_{cm} = (v_a + v_b)/2$) and the DM voltage ($v_{dm} = (v_a - v_b)/2$) of the ZVS dc-ac stage. The CM voltage of the ZVS dc-ac stage is not constant with ZVS-PWM. The spectrum of the high frequency CM voltage mostly distributes at 50 kHz (from the PWM modulation) and 100 kHz (from the ZVS modulation). Similar to the DM inductors, the CM inductors are also smaller than those in a normal low-frequency full-bridge inverter and the leakage current requirement is still fulfilled [29].
3) ***Smaller heat sink***. Unlike the hard-switching PV inverters where most of the power loss is concentrated in the semiconductor devices, the ZVS PV inverter has better heat distribution and less thermal stress. The switching loss of the dc-ac stage is significantly reduced by the ZVS-PWM. Thus smaller heat sink can be used for semiconductor devices. The resonant current causes additional power loss on the resonant inductor. Proper design is needed to minimize the resonant inductor loss. And the heat is easier to be dissipated because of the larger contact surface between the resonant inductor and air.

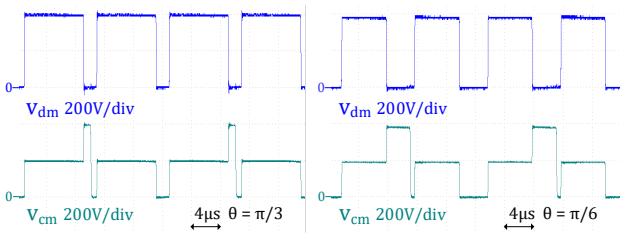

Fig. 8. Experimental waveform of the CM voltage and the DM voltage of the ZVS dc-ac stage at different grid phases with rated input voltage (360 V) and rated ac voltage (230 Vrms) .

C. Design Challenges

The design consideration of the interleaved boost stage in the ZVS PV inverter is the same as many other hard-switching topologies. While the ZVS dc-ac stage brings new technical challenges due to the additional resonant operations. First, the resonant circuit brings extra power loss (mainly contributed by the active-clamping switch and the resonant inductor). As shown in Fig. 7, all the output current flow through the resonant circuit formed by S_a, L_r and C_c. The average current of S_a and C_c in one switching cycle is zero based on the charge balancing requirement of C_c. The average current of L_r is the output current (i_o). The peak current of L_r depends on the energy needed to charge and discharge the resonant capacitor C_r and is always higher than $2i_o$. The resonant parameters should be properly designed to ensure low resonant current for lower additional power loss.

The switches in the dc-ac stage including the active-clamping switch and four inverter switches have higher steady state voltage stress which equals $V_{dc} + V_{cc}$. The voltage of the clamping capacitor V_{cc} can be calculated based on the voltage-second balancing of the resonant inductor:

$$V_{cc} = \frac{(1 - D_a)V_{bus}}{D_a}. \quad (1)$$

Here D_a is the duty-ratio of the active-clamping switch. In order to use standard 600V silicon MOSFET and fulfill the maximum MPPT voltage (450 V), the maximum voltage of semiconductor devices should be designed below 500 V. That is $V_{cc} < 50$ V and $D_a > 0.9$. The PCB layout of the power stage also needs to be optimized since there is less room for the transient voltage spike.

TABLE II
CIRCUIT PARAMETERS OF THE ZVS PV INVERTER

Boost stage	Parameters per phase
Rated power / output voltage	1.5 kW / 360 V
Switching Frequency	50 kHz
Input capacitor	120 μF / 500 V
Boost inductor	533 μH / 30 mΩ Sendust toroid 184-060, 70 turns
Boost MOSFET	FCH47N60F
Boost diode	SCS210AG
Inverter stage	**Parameters**
PWM carrier frequency	50 kHz
Resonant dc link frequency	100 kHz
Bus decoupling capacitor	470 μF $\times$5, 500 V
DM inductor	147 μH / 10 mΩ $\times$2 Sendust toroid 184-060, 32 turns
Resonant inductor	7.2 μH / 10 mΩ PQ32/30, DMR95, 8 turns
Resonant capacitor	1 nF $\times$2, film
Clamping capacitor	10 μF $\times$2, film
MOSFET	FCH041N65F
Input CM inductor	882 μH
Output CM inductor	2.6 mH

The resonant and clamping behavior of the dc link voltage also reduces the available duty-ratio to deliver active power under PWM control. When the dc link voltage is clamped to zero, the DM voltage of the inverter also equals zero. With $D_a > 0.9$, the maximum duty-ratio of PWM control can be 0.9. That is acceptable for the 360 Vdc – 230 Vac conversion. The resonant operations also distort the rising edge and falling edge of the DM voltage and introduce harmonic currents to the output current. A predictive compensation method has been proposed in [32] to reduce the current distortion. All the above design challenges are related to the resonant parameters (L_r and C_r) which need to be carefully selected.

III. DESIGN AND IMPLEMENTATION

A. Hardware Design

The parameters of the ZVS PV inverter are given in Table. II. The minimum input voltage with full power capability is 200 V. The degraded inductance of each boost inductor is 533 μH and the maximum current ripple of the boost inductor is 3.34 A with maximum input current (1500 W / 200 V = 7.5 A). The current ripple decreases with either higher input voltage or lower input current. The boost stage works at CCM mode in the full MPPT range. The bus decoupling capacitor is selected based on the bus voltage ripple:

$$\Delta V_{bus-pp} = \frac{P_{in}}{2\pi f_{line} C_{bus} V_{bus}}. \quad (2)$$

Here f_{line} is the grid frequency, V_{bus} is the dc bus voltage, P_{in} is the dc input power. C_{bus} is chosen as 2.35 mF (five 470 μF electrolytic capacitors in parallel). The maximum bus voltage ripple (peak to peak) is 11.3V with minimum bus voltage (360 V) and rated power (3 kW).

The ripple frequency of DM inductor is 100 kHz and the inductance can be smaller. Based on the industry experience, the current ripple is normally designed to be less than 15% of the peak current for low THD. A sendust toroid core is used

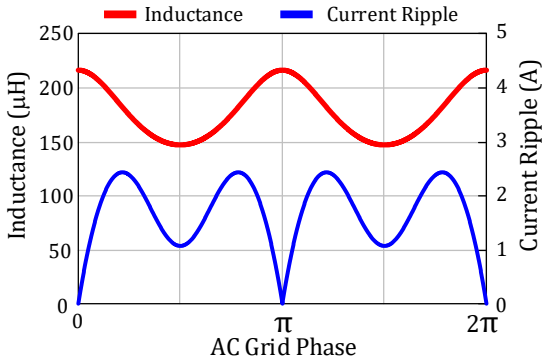

Fig. 9. The inductance and peak-to-peak ripple of one DM inductor vary with ac grid phase. P_o = 3 kW, PF = 1.

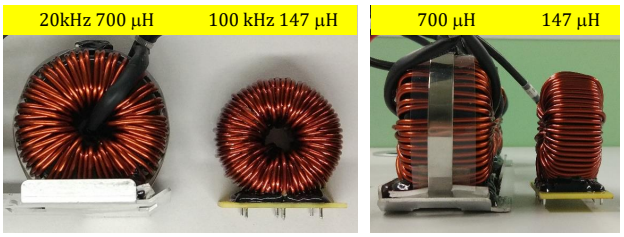

Fig. 10. Photograph of one 100 kHz 147 μH DM inductor used in ZVS PV inverter and one 20 kHz 700 μH DM inductor used in a commercial PV inverter. The inductor size is reduced by 60%.

for each DM inductor with a 32-turn winding. The inductance and peak-to-peak ripple of one DM inductor is calculated and illustrated in Fig. 9. The minimum inductance is 147 μH with peak output current. The maximum current ripple is less than 15% of the peak output current. Fig. 10 is the photograph of one DM inductor used in ZVS PV inverter together with a 20 kHz 700 μH DM inductor used in a commercial PV inverter. The 100 kHz 147 μH DM inductor is smaller and lighter.

The design guideline of resonant parameters has been introduced in [27], [28]. The inductance of the resonant inductor is 7.2 μH. Unlike the boost inductor and the DM inductor, the peak-to-peak ripple percentage of resonant inductor is higher than 200%. As shown in Fig. 3, the current waveform of the resonant inductor is like a triangle wave. With such high ripple current, Litz wire (Φ 0.1 mm $\times$350) is used to reduce the ac winding resistance. The required air gap is 1.5 mm and it is evenly divided into three sections on the center leg of the core.

The resonant capacitors are two 1 nF film capacitors connected in paralleled with each inverter phase. The clamping capacitor is regarded as a constant dc voltage source during the resonant operations so that its capacitance should be much higher than the resonant capacitors. Two 10 μF film capacitors are used as the clamping capacitor but the voltage stress is low ($\leq$ 50 V). The voltage fluctuation of the clamping capacitor is less than 2% in one switching cycle. Fig. 11 shows the 3D drawing of two DM inductors, the resonant inductor and clamping inductor (the resonant capacitors are too small to be shown). Comparing with the 20 kHz DM inductors used in a hard-switching PV inverter, the volume of the ZVS DM inductors is reduced by 67% and the total volume including the

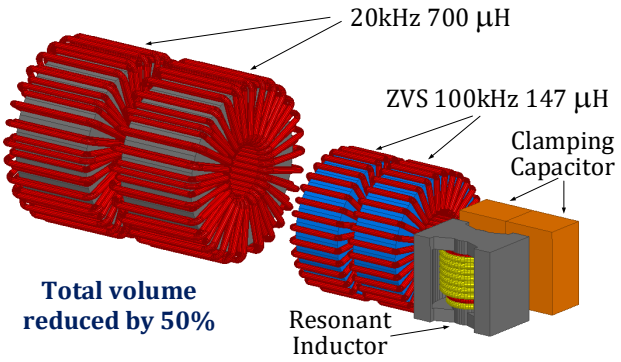

Fig. 11. Comparison of passive components in the dc-ac stage between zero-voltage-switching and hard-switching. The passive component size is reduced by more than 50%.

additional resonant inductor and clamping capacitor is reduced by 50%. Reduced inductor size is a major advantage of high frequency grid-interface inverters.

With the selected resonant parameters, the duty-ratio of the active-clamping switch is higher than 0.9, the voltage of the clamping capacitor is smaller than $0.1V_{bus}$, the positive peak current and negative peak current of the resonant inductor are 40 A and -10 A, which satisfy the need for the target design.

Fig. 12 illustrates the common mode model of the ZVS PV inverter including the boost stage for leakage current analysis. This model is based on the common mode model of a single-stage single-phase inverter [5], [29]. L_{CMI} and L_{CMO} are the input CM inductor and the output CM inductor. C_{CM} is the capacitance of the CM bypass capacitors given in Fig. 13. V_{CMB} and V_{CMI} represent the common mode voltage generated by the boost stage and the inverter stage. The parasitic capacitance (C_{PVN}) of a 3 kW PV panel can be estimated from 150 nF to 450 nF. The stray capacitance (C_{gb} and C_{gi}) between the MOSFETs and the heat sink is from tens to hundreds of picofarads. C_{gb} and C_{gi} can be treat as open-circuit due to their higher impedance when analyzing the leakage current in the parasitic capacitance of the PV panel [5]. Therefore, the leakage current in the common mode path is mainly determined by the inverter stage. The design of the CM filter is also based on the common mode characteristic of the ZVS inverter stage.

The CM filter is modified from the design of a 3kW commercial PV inverter with H6 topology. Even though the H6 topology has constant dc CM voltage, CM filters are still needed to suppress to leakage current caused by the switching transient and fulfill the EMI requirement. Same input CM inductor and output CM inductor are used in the ZVS PV inverter. The inductance is 882 μH and 2.6 mH respectively. As shown in Fig. 13, four CM capacitors ($C_{CM} = 0.68\mu$F) are added to bypass the leakage current of the ZVS PV inverter. The measured leakage current is below 35 mA in both laboratory test and field test.

Fig. 14 shows the top view of the ZVS PV inverter. The chassis is made by 3D printer for fast prototyping. Due to the smaller size and light weight, the boost inductors and the DM inductors can be assembled on the PCB with the power stage.

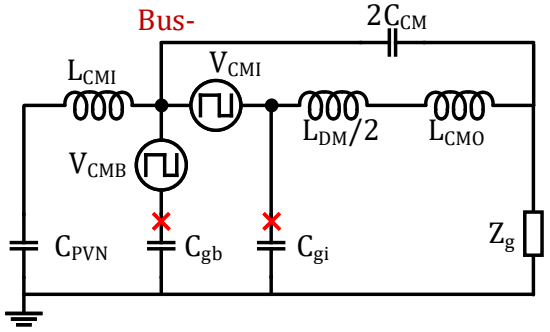

Fig. 12. Common mode model of the ZVS PV inverter for leakage current analysis.

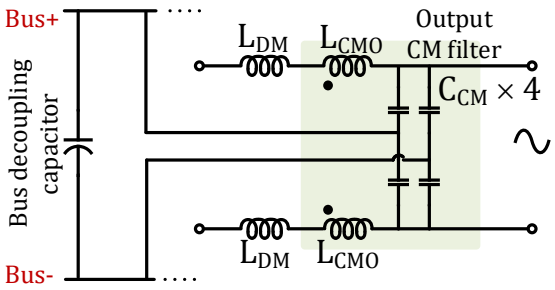

Fig. 13. Schematic of the output CM filter design.

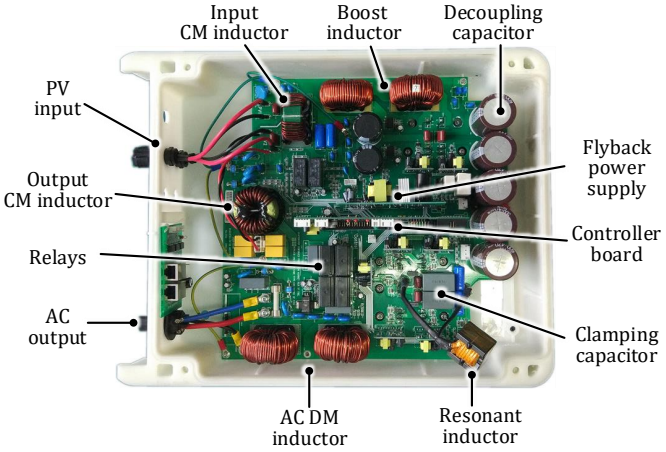

Fig. 14. Top view of ZVS PV inverter. The dimension is 400×315×135 mm including the heat sink attached to the bottom side of the chassis.

While in most traditional PV inverters, those inductors are installed separately with fixtures and extra cables are needed to connect the inductors with the power stage. The on-board assembling of the inductors can reduce the cable loss and save costs for manufacture and maintenance. The dimension is 400×315×135 mm including a 260×200×30 mm aluminum alloy heat sink and the total weight of this ZVS PV inverter is 8 kg. While most commercial PV inverters with similar specifications are usually weighted more than 10 kg.

B. Loss Analysis

The power loss of the major components are calculated with the parameters in Table. II and illustrated in Fig. 15. The PV

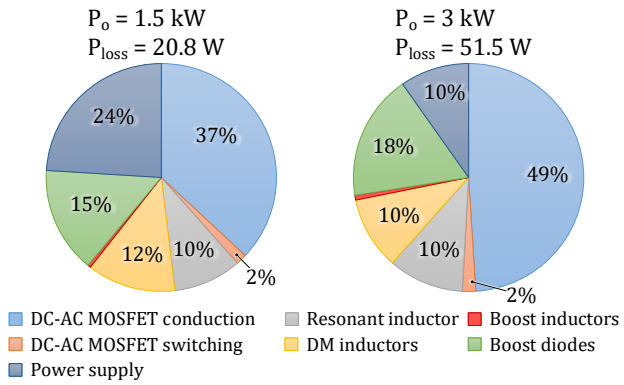

Fig. 15. Loss breakdown of the ZVS PV inverter with rated input voltage (360 V) and rated ac voltage (230 Vrms).

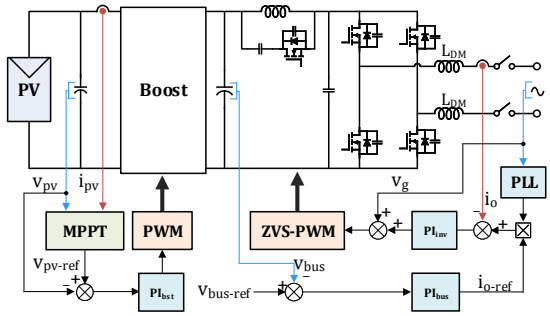

Fig. 16. Control diagram of the ZVS PV inverter with two-stage mode.

voltage is 360 V and the ac RMS voltage is 230 V for loss calculation. The power loss of the boost stage depends on the PV input voltage and the boost stage is bypassed with rated input voltage. Thus, the loss of the boost MOSFET is not included in the loss breakdown. The boost inductors and diodes are considered as wire and only the conduction loss is calculated. The estimated overall efficiency of the ZVS PV inverter is 98.6% with 1.5 kW and 98.3% with 3 kW. The conduction loss of MOSFETs is the largest part of the total loss. The switching loss of MOSFETs (including both inverter switches and the active-clamping switch S_a) is greatly reduced, which only takes 2% of the total power loss at half power and full power. Such low switching loss indicates it is possible to further increase the switching frequency of the dc-ac stage with ZVS-PWM. The thermal stress of MOSFETs is also relieved.

The conduction loss of the boost diodes is not neglectable due to the high forward voltage (1.35 V at 10 A). A typical solution is connecting a bypass diode in parallel with the boost inductor and boost diode. Many cheap diodes with low forward voltage ($<$ 0.8 V at 10 A) are available since there is no requirement for the recovery time and recovery charge in the bypass operation. The power consumption of the flyback power supply is optimized to 5 W by choosing 10 V gate voltage and using PWM control for the relays.

C. Control Implementation

The entire control system of the ZVS PV inverter is implemented in a digital microcontroller (TI TMS320F28069). Fig. 16 shows the control diagram of the ZVS PV inverter when the PV voltage is lower than the rated input voltage and the boost stage is working. The perturb and observe based MPPT algorithm gives the voltage reference of the PV voltage. The boost stage regulates the PV voltage by a PI controller. The bus voltage is controlled by the dc-ac stage. The output of the bus voltage loop is the peak current reference of the inner current loop. The output current is controlled by a PI controller with feedforward of the grid voltage. The control of the boost stage and the dc-ac stage is decoupled. The bus voltage regulation should be faster than the PV power regulation. So that the power fed into the grid can be adjusted quickly to track the PV power fluctuation and the voltage of dc-link capacitor can be stable. The inner current loop also needs to be faster than outer bus voltage loop. The bandwidth of the boost voltage loop, bus voltage loop and output current loop is 5 Hz, 250 Hz and 3.3 kHz respectively with three different PI controllers. The bandwidths of the boost voltage loop and the bus voltage loop can be further optimized to reduce the double-line-frequency harmonic current [38]. This is the classical control architecture for two-stage PV inverter except the ZVS-PWM block. The functional block diagram of the ZVS-PWM block is shown in Fig. 7. The duty-ratios of the complementary ZVS control signals v_{gsa} and v_{sc} are determined by the bus voltage, the instantaneous output current and the resonant parameters. These duty-ratios are pre-calculated and stored in the microcontroller as a look-up table. They are updated in every switching cycle.

The bus voltage reference depends on the grid voltage in the two-stage mode, which is set to be 1.56 times of the ac RMS voltage. The lower limit of the bus voltage reference is 360 V and the upper limit is 450 V. When the PV voltage is higher than the rated input voltage, the controller shut down the the boost stage and the ZVS PV inverter works in single-stage mode. In the single-stage mode, the PV voltage reference from the MPPT block is directly feed to the bus voltage loop as the reference of the bus voltage (the PV voltage equals the bus voltage if ignoring the voltage drop of the boost inductor and boost diode). The outer bus voltage loop and the inner current loop remain the same as the two-stage mode.

The PV panels are always connected to the input side of PV inverter without dc relays. This configuration can guarantee self-start of the flyback power supply. There is no inrush current on the dc bus capacitors since they are always connected to the PV panels. Thus, the ZVS PV inverter does not need soft-start control.

IV. Experimental Results

The laboratory test is conducted with a PV simulator (Chroma 62150H). Fig. 17 shows the waveform of grid voltage v_g, output ac current i_o and resonant current i_{Lr} with rated input voltage (360 V), full load (3 kW) and unity power factor. The THD of the output current is 2% with full load. The dc current injection is below 50 mA which is smaller than 0.5% of the RMS current. The amplitude of the resonant current changes with the double-line frequency and the peak appears with maximum output current. The frequency of the resonant

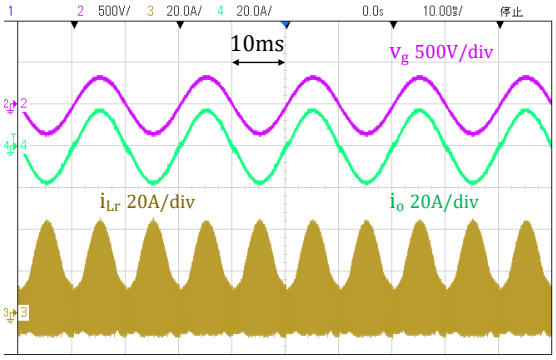

Fig. 17. Measured waveform of grid voltage v_g, output ac current i_o and resonant current i_{Lr} with rated input voltage (360 V) and full load (3 kW), the power factor (PF) equals 1.

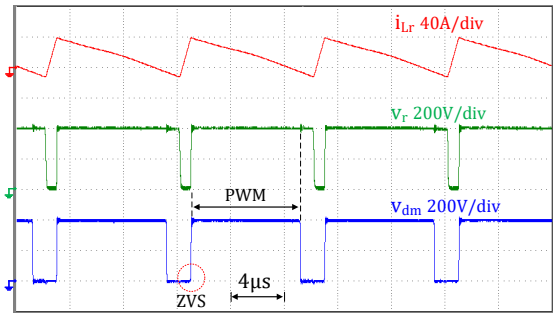

Fig. 18. Measured waveform of resonant current i_{Lr}, resonant dc link voltage v_r and the DM voltage of the inverter v_{dm} in several switching cycles. The commutation from body-diode to MOSFET is synchronized to the zero-clamping state of the dc link for ZVS.

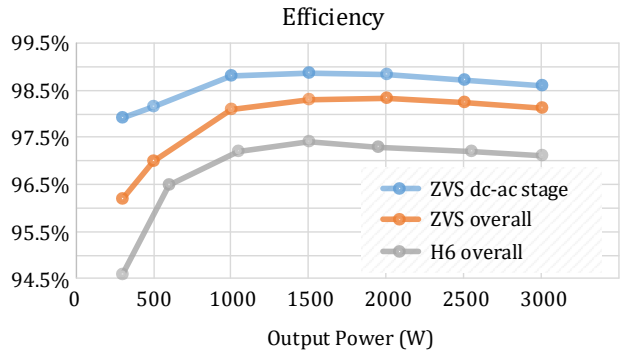

Fig. 19. Measured efficiency of 1) the ZVS dc-ac stage, 2) ZVS PV inverter including the boost inductors, boost diodes and the flyback power supply, 3) H6 hard-switching inverter, all with rated input voltage (360 V) and rated ac voltage (230 Vrms).

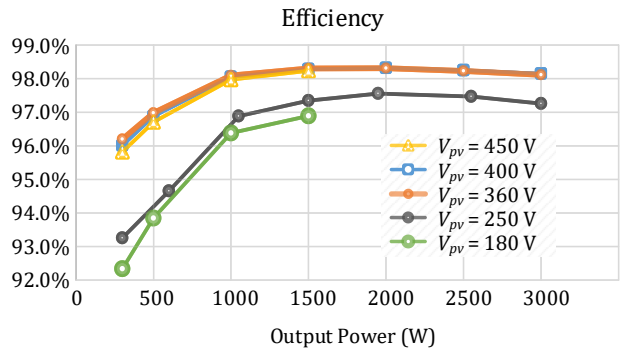

Fig. 20. Overall efficiency of ZVS PV inverter with different input voltages and rated ac voltage (230 Vrms).

current is 100 kHz, which is shown in Fig. 18 along with the resonant dc link voltage v_r and the DM voltage of the inverter v_{dm}. The voltage of the dc link is clamped to zero for a short period in every switching cycle. The commutation from body-diode to MOSFET finishes during this zero-clamping state. The width of the DM voltage is still modulated by PWM. The voltage waveform also shows the voltage stress of MOSFET in the dc-ac stage is slightly higher (400 V) than the dc bus voltage (360 V).

The efficiency of the ZVS PV inverter with rated input voltage (360 V) and rated ac voltage (230 Vrms) is measured and plotted in Fig. 19. The ZVS dc-ac stage has the peak efficiency of 98.8% with half load and a full load efficiency of 98.6%. The overall efficiency of the ZVS PV inverter decreases by 0.5% – 1.7% especially with light load. The reason is the power consumption of the flyback power supply remains the same with light load and takes higher portion of the total power. The weighted CEC efficiency is calculated as 98%. The efficiency of a 3kW commercial H6 PV inverter mentioned in Section III is also measured with the same operation voltages, which is lower than the ZVS PV inverter due to higher switching loss and magnetic loss.

Fig. 20 shows the measured overall efficiency of the ZVS PV inverter with different input voltages and rated ac voltage (230 Vrms). The maximum power is limited to half of the rated power with $V_{pv} = 180$ V and $V_{pv} = 450$ V for the purpose of 1) reducing the current stress for boost diode and boost inductor with low input voltage; 2) reducing the voltage spike for the inverter switches with high input voltage. The overall efficiency is reduced by the boost stage when the input voltage is below the rated value ($V_{pv} = 180$ V and $V_{pv} = 250$ V). When the input voltage is higher than the rated value ($V_{pv} = 400$ V and $V_{pv} = 450$ V), the loss of DM inductor is increased due to larger current ripple, the conduction losses of the auxiliary circuit, the boost inductor and boost diode are lower due to lower input current, the change of other switching loss is minor due to ZVS and the conduction loss of inverter switches also remains the same with the same output current. The overall efficiency turns out to be slightly lower with higher input voltage.

Fig. 21 shows the startup transient of the MPPT operation. The PV inverter normally starts at the open circuit voltage of the PV panels (set as 450V for the PV simulator). When MPPT begins, the PV voltage (equals bus voltage in single-stage mode) is regulated to track the maximum power and the the output current gradually increases. The MPPT step is 5 V and the disturbance cycle is 2s.

Fig. 22 and Fig. 23 show the dynamic response with grid voltage disturbance performed by the grid simulator (Chroma 61860). The ZVS PV inverter works at two-stage mode ($V_{mpp} = 320$ V and $P_{mpp} = 3$ kW controlled by the PV simulator). After the grid voltage steps from 200 Vrms to 250

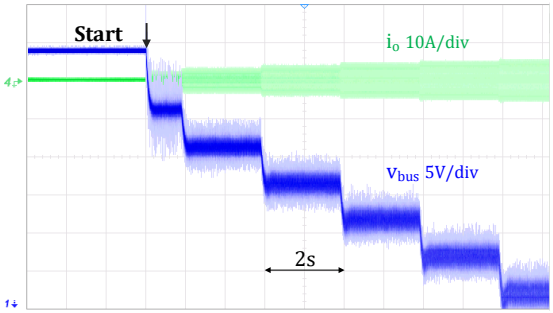

Fig. 21. Start of the MPPT operation. The inverter starts at the open circuit voltage of the PV simulator with single-stage mode.

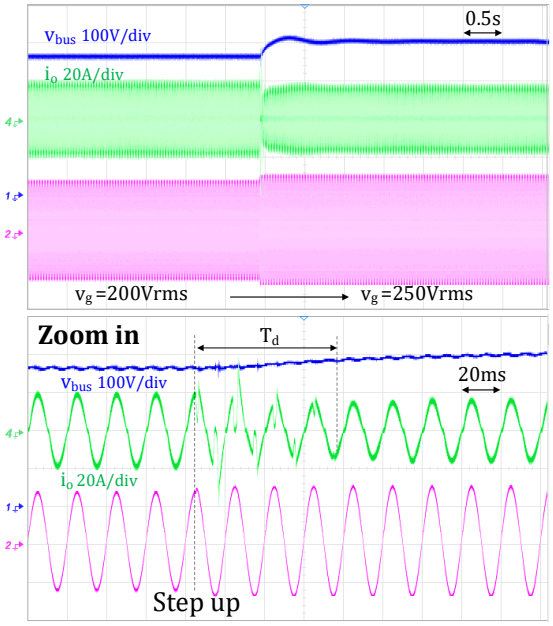

Fig. 22. Dynamic response with grid voltage steps up from 200 Vrms to 250 Vrms.

Vrms (Fig. 22), the bus voltage reference is updated from 360 V to 390 V(250×1.56) and the bus voltage controller ramps up the bus voltage by reducing the grid current reference. There is a delay period before the bus voltage is regulated to a higher level (marked as T_d in Fig. 22). During this delay period the PWM output voltage of the ZVS inverter is lower than the peak grid voltage (353.5 V), resulting reverse bias of the output DM inductors and reduction of grid current amplitude near the peak grid phase angle. This reduces the instantaneous power fed into grid and prevents the bus voltage from dropping. After the delay period the current distortion disappears and the bus voltage continues to rise until it reaches the reference value. In Fig. 23 the grid voltage steps down from 250 Vrms to 200 Vrms. The instantaneous power fed into grid decreases at the beginning of the step-down change. So that the bus voltage increases at first and then is regulated downwards with the bus voltage reference updated from 390 V to 360 V. The PWM output voltage of the inverter bridge is always higher than the peak grid voltage during the step-down response so that the reverse bias of output DM inductor as well as the current distortion do not occur in this case.

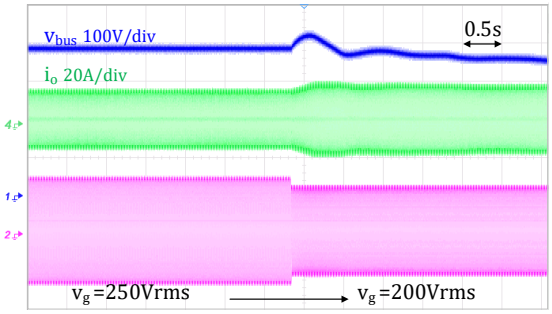

Fig. 23. Dynamic response with grid voltage steps down from 250 Vrms to 200 Vrms.

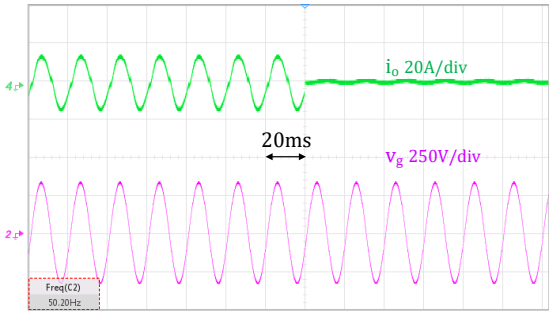

Fig. 24. Protection test with grid frequency $>$ 50.2 Hz.

The controller monitors the grid voltage and frequency and will shut down the inverter If the grid voltage and frequency exceed the normal operation range based on the grid-connection requirement. Fig. 24 shows the inverter is shut down when the grid frequency is higher than 50.2 Hz, which is a typical requirement from the distribution grid.

The experimental results of MPPT, grid voltage disturbance and frequency disturbance verify that the ZVS PV inverter can be controlled with the same high-level control architecture as the typical hard-switching PV inverter. The ZVS-PWM modulator is not affected by the outer control loop and can be updated rapidly to ensure ZVS operation of the dc-ac stage in every switching cycle.

V. Field Test of PV Generation

Ten 3 kW ZVS PV inverters with same parameters in Table. II are built for the field test. The test location is 23°01′N 114°20′E. Each ZVS PV inverter is powered by 12 PV panels connected in series. Table. III lists the parameters of the PV panel with irradiance = 1000 W/m^3 and T = 25°C. The maximum power of each PV string is 3060 W and the open circuit voltage is 455 V. The measured open circuit voltage is between 410 V and 440 V due to different aging status and dust on the surface. The system schematic of the 30 kW PV system is shown in Fig. 25. Ten ZVS PV inverters are distributed into three groups and connected to the three-phase 230V grid respectively. The neutral line is connected to earth through a ground stick near the distribution room. The metal frames of all PV panels and the chassis of all PV inverters are also grounded nearby. Fig. 26 is the photograph of the 30 kW PV panels and the distribution room. The ZVS PV inverters

TABLE III
SPECIFICATIONS OF THE PV PANEL

Open circuit voltage	Short circuit current	MPP voltage	MPP current	MPP power
37.93 V	8.62 A	30.65 V	8.31 A	255 W

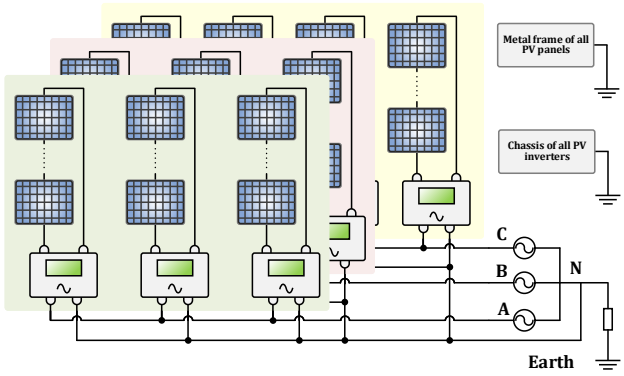

Fig. 25. Schematic of the 30 kW PV system with ten 3 kW ZVS PV inverters.

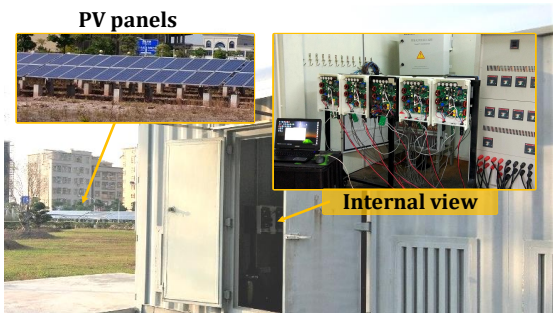

Fig. 26. Photograph of the 30 kW PV panels, the distribution room and its internal view with ten 3 kW ZVS PV inverters.

are installed inside the distribution room. The data of each inverter is automatically collected by a computer.

The leakage current of the ZVS PV inverter is measured during the field test by a residual current transducer (LEM CTSR 0.3-P). Its measuring range is ±500 mA with a sensitivity of 4 V/A. As shown in Fig. 27, the output RMS voltage of the transducer is 68 mV, which equals a leakage current of 17 mA. The leakage current is also tested in the laboratory with PV simulator. External capacitor with capacitance of 450 nF is connected between the negative PV input and the earth to simulate the parasitic capacitance. The RMS leakage current is 34.3 mA with such configuration. The measured results of both field test and laboratory test have shown that the leakage current requirement [39] is fulfilled.

The system operated without malfunctions during the whole test. Fig. 28 shows the operational data of one ZVS PV inverter including the PV voltage, bus voltage and grid voltage from sunrise to sunset. Fig. 29 shows the instantaneous output power of ten ZVS PV inverters on the same day. The data shows the self-start of the inverter with very low PV voltage in the morning, MPPT and bus voltage regulation with the fluctuation of grid voltage. Power difference exists among PV strings. The maximum power of ten ZVS PV inverters was 2 kW and

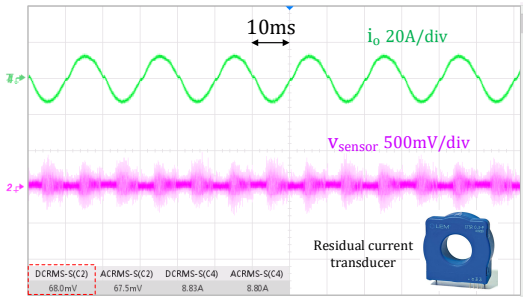

Fig. 27. Measured waveform of the output current and the output voltage of the residual current transducer. The sensitivity of the transducer is 4 V/A.

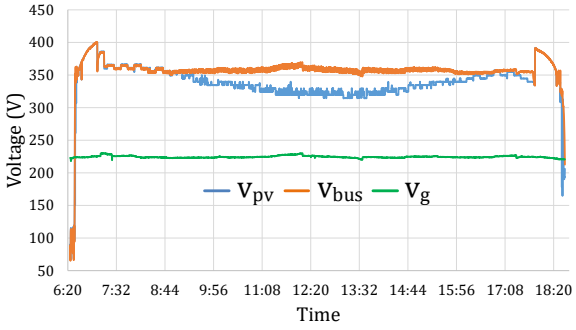

Fig. 28. The operational data of one ZVS PV inverter over a single day.

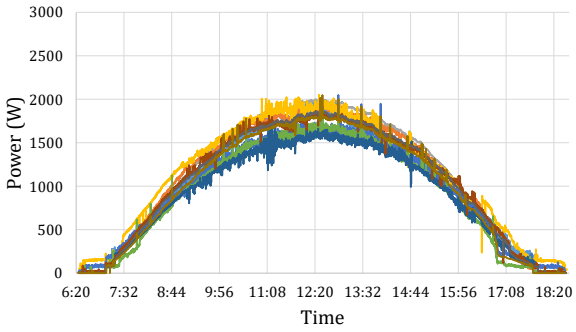

Fig. 29. The output power of ten ZVS PV inverters over a single day (data from 22/03/2017, same date as Fig. 28).

the overall energy generated on that day were between 12.7 kWh–13.5 kWh. The data of field test can help locate the most frequent operational power and voltage for the optimization of the ZVS PV inverter and support the reliability analysis.

The ideal MPP voltage of one PV string is 367.8 V. The field test data shows the MPP voltage is lower than this value and the ZVS PV inverter works in two-stage mode for the most time, especially with higher power. The reason can be explained by the aging of PV panels and the variation of irradiance and temperature. Thus the switching loss of the boost stage is also not neglectable. A modified topology can be used to achieve ZVS for both the boost stage and the dc-ac stage [40]. As shown in Fig. 30, the boost phase is connected in parallel with the dc-ac phases like a three-phase converter. The zero-clamping state of the resonant dc link can create ZVS opportunities for all the three phases. The gate driver

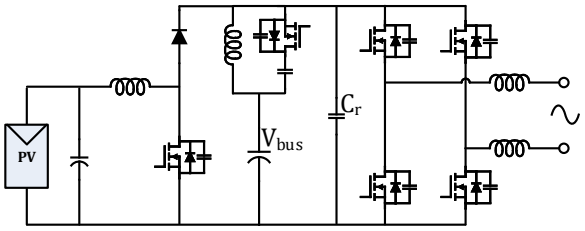

Fig. 30. The ZVS PV inverter with a ZVS boost stage and a ZVS dc-ac stage.

signal of the boost switch needs to be synchronized to the ZVS modulation signals (v_{gsa} and v_{sc}). The switching frequency of the boost stage can be further increased and the size of the boost inductor can be reduced.

VI. Conclusions

In this paper, a 3 kW two-stage PV inverter with ZVS-PWM technology is proposed. The inverter is with high efficiency, small size and light weight by employing the resonant dc link concept and ZVS modulation in the dc-ac stage. The ZVS-PWM technology greatly reduces the switching loss and enables higher switching frequency, smaller magnetic components. A systematic design of the ZVS PV inverter including hardware prototyping and control implementation is presented. The dc-ac stage can achieve the peak efficiency of 98.8%. The overall peak efficiency of the ZVS PV inverter is 98.3%. The test results of THD, dc current injection, leakage current and grid disturbance show that the ZVS PV inverter meet the grid code requirement. A field test with ten ZVS PV inverters has been done to collect data for the future research and verify the reliability.

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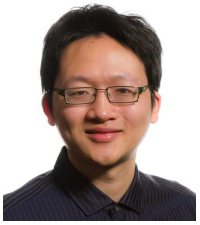
Yenan Chen (Member, IEEE) received his bachelor's degree and Ph.D. degree from Zhejiang University, Hangzhou, China, in 2010 and 2018 respectively, both in Electrical Engineering.

Since 2018, he has been a Postdoctoral Research Associate with the Department of Electrical Engineering, Princeton University, NJ, USA. His research interests include high frequency power converters, advanced power electronics architecture, grid-interface power electronics and renewable energy systems. He holds three issued Chinese patents.

Dr. Chen received the APEC Outstanding Presentation Award in 2019, the First Place Award from the Innovation Forum of Princeton University in 2019, and the Best Paper Award in COMPEL 2020.



Minjie Chen (Senior Member, IEEE) received the B.S. degree from Tsinghua University, Beijing, China, in 2009, and the S.M., E.E., and Ph.D. degrees from Massachusetts Institute of Technology (MIT), Cambridge, MA, USA, in 2012, 2014, and 2015, respectively. He was a Postdoctoral Research Associate at MIT in 2016. Since 2017, he has been with the Department of Electrical Engineering and Andlinger Center for Energy and the Environment at Princeton University, NJ, USA, where he leads the Princeton Power Electronics Research Lab. His research interests include high frequency power electronics, advanced power electronics architectures, power magnetics, machine learning, and the design of high performance power electronics for emerging and important applications.

Dr. Chen was the recipient of two IEEE Power Electronics Society Transactions Prize Paper Awards in 2017 and 2018, a Best Paper Award in COMPEL 2020, the NSF CAREER Award, the Dimitris N. Chorafas Ph.D. Thesis Award from MIT EECS, an Outstanding Reviewer Award from IEEE TRANSACTIONS ON POWER ELECTRONICS, two IEEE ECCE Best Demonstration Awards, multiple IEEE APEC Outstanding Presentation Awards, a Siebel Energy Institute Research Award, and the First Place Award from the Innovation Forum of Princeton University. He was honored by the Princeton Engineering Commendation List for Outstanding Teaching. He is the Associate Editor of IEEE TRANSACTIONS ON POWER ELECTRONICS, Associate Editor of IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN POWER ELECTRONICS, Associate Technical Program Committee Chair of IEEE ECCE 2019, and Technical Program Committee Chair of IEEE International Conference on DC Microgrids in 2021. He holds five issued US patents.

Dehong Xu (Fellow, IEEE) received his B.S., M.S., and Ph.D. degrees from the College of Electrical Engineering, Zhejiang University, Hangzhou, China, in 1983, 1986, and 1989, respectively.

Since 1996, he has been with the College of Electrical Engineering, Zhejiang University, China, as a Full Professor. From June 1995 to May 1996, he was a Visiting Scholar with the University of Tokyo, Tokyo, Japan. From June to December 2000, he was a Visiting Professor with Center for Power Electronics Systems (CPES), Virginia Tech, Blacksburg, VA, USA. From February 2006 to April 2006, he was a Visiting Professor with the ETH, Switzerland. His current research interests include power electronics topologies, modelling and control, and applications for renewable energy and energy efficiency. He has authored or coauthored eight books and more than 270 IEEE journal and conference papers. He holds more than 50 patents.

Dr. Xu is the recipient of seven IEEE journal and conference paper awards. He became an IEEE Fellow in 2013. He was an IEEE PELS Distinguish Lecturer from 2015 to 2017. He received the IEEE PELS R. D. Middlebrook Achievement Award in 2016.