MSP-LEGO: Modular Series-Parallel (MSP) Architecture and LEGO Building Blocks for Non-isolated High Voltage Conversion Ratio Hybrid Dc-Dc Converters

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***Abstract*—This paper presents a *Modular Series-Parallel* architecture and *Linear Extendable Group Operated* (MSP-LEGO) building blocks to achieve high efficiency and high power density in non-isolated high voltage conversion ratio dc-dc applications. Like other hybrid dc-dc solutions, the MSP-LEGO approach merges the strengths of switched-capacitor circuits and switched-inductor circuits, and facilitates series-input parallel-output configuration for balanced distribution of voltage stress and current sharing. The hybrid switched-capacitor-magnetics configuration enables zero-voltage-switching (ZVS) and near zero-current-switching (ZCS). The input voltage and output current of proposed architecture can be linearly extended through series-connected switched-capacitor circuits and parallel-connected switched-inductor circuits. A 100 W, 150 Vdc-to-5 Vdc non-isolated high conversion ratio hybrid dc-dc converter is built and tested. The prototype dc-dc converter achieved 110 W/in^3 power density and 91.5% peak efficiency with automatic voltage balancing and current sharing.**

I. Introduction

Power converters with high voltage conversion ratios are needed in a wide range of applications including point-of-load (PoL) converters and off-line power supplies [1], [2]. Magnetics-based high step-down ratio topologies usually suffer both high voltage stress and high current stress. Increasing the operation frequency can reduce the magnetic component size. However, the hard-switching operation of these converters limits the switching frequency that can be achieved. Tapped-inductor derived topologies are popular solutions [3], but the voltage ringing caused by the leakage inductance of the coupled inductor is a concern. Transformer based topologies usually have low power density and poor light load efficiency [4]. The extended duty ratio multi-phase buck and the multi-phase cascaded buck converters can improve the efficiency and enhance the transient performance [5]. However, under high conversion ratio, many inductors are required which limits the system power density.

Switched-capacitor-based converters are very attractive options for high voltage conversion ratio applications [6], [7]. Switched capacitor based single phase or multiphase topologies achieve high power density and low switching losses because the switches operate at reduced voltages. They can achieve very high power-density and can enable potential on-chip integration. However, switched capacitor circuits have limited voltage regulation capability. The achievable voltage conversion ratios are discrete values. The switches in a typical switched-capacitor circuits are usually hard-switched, leading to switching loss and electromagnetic interference (EMI) concerns. A magnetics-based converter is usually needed as a second stage to regulate the voltage [8].

Hybrid switched-capacitor-magnetic topologies [8]–[20] are promising solutions. [9]–[11] leverage the strengths of coupled inductors and extended duty ratio of buck switches, and offer very low component count. [15], [16] combines Dickson switched capacitor circuit with buck converters to achieve high voltage conversion ratio. However, the currents of the paralleled inductors are not necessarily balanced. Precise capacitance values are needed to guarantee soft-switching and soft-charging. Moreover, existing solutions are usually designed for one specific conversion ratio or output power. They are usually not designed as extendable modules and do not offer good scalability to high voltage or current ratings.

Methodologies to address the above mentioned challenges are needed. The key challenge of designing high performance high voltage conversion ratio power converters is the co-existence of high voltage stress and the high current stress (leading to large effective semiconductor die area). As a result, the principle of the proposed solution is to optimally allocate the voltage and current stresses by series-parallel connecting modular circuit units and enable optimal utilization of active and passive devices. Topologies which can both leverage the high power density of capacitors and the high voltage conversion capability of coupled magnetics are attractive. By connecting a few subcircuit in series on the high voltage side, and connecting a few subcircuit in parallel on the high current side, the voltage stress and current stress can be optimally distributed [8] and reduced.

The remainder of this paper is organized as follows: Section II presents the overview and key principles of the modular series-parallel architecture, including two example building units. The details of circuit topology, operation principles and voltage conversion ratio are presented in Section III. Section IV presents several extended design options of the modular series-parallel architecture. Details about the prototype design and experimental results are provided in Section V. Finally, Section VI concludes this paper.

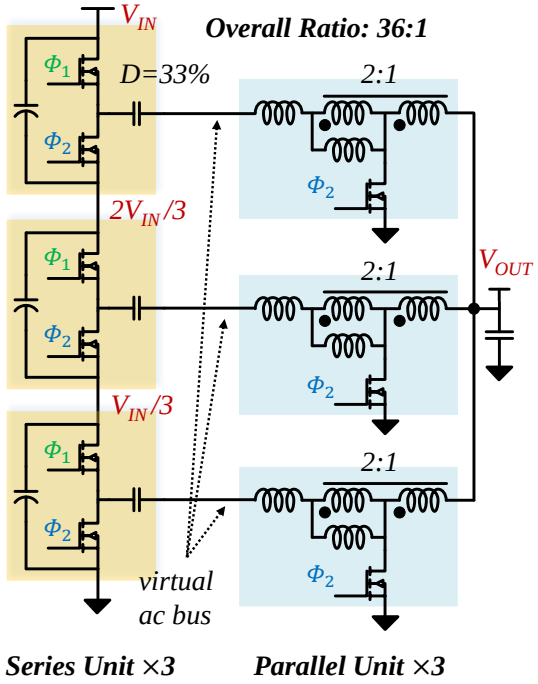


Fig. 1: Block diagram of a MSP-LEGO hybrid converter with a virtual ac bus as the intermediate stage that links the two modular building blocks together.

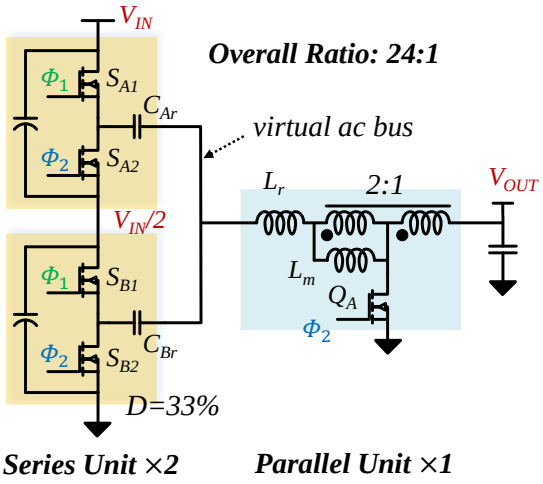


Fig. 2: One example embodiment of the MSP-LEGO architecture with two series units, one parallel unit and one merged virtual ac bus.

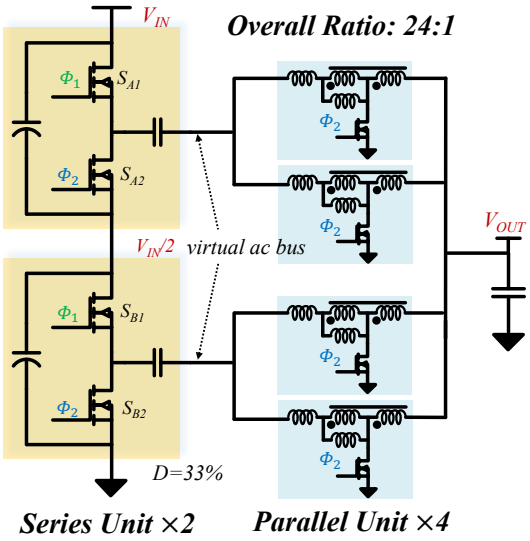


Fig. 3: Another example embodiment of the MSP-LEGO architecture with two series units, four parallel units and two split ac buses.

II. Architecture Overview

Fig. 1 shows an example MSP-LEGO architecture having three series switched-capacitor units and three parallel switched-inductor units as the *linear extendable group operated* (LEGO) build blocks. Each series unit comprises a half-bridge with two switches and two capacitors (namely a switched capacitor building block); each parallel unit comprises a center-tapped inductor and one switch (namely a switched inductor building block). The leakage and magnetizing inductance are both illustrated on the primary side. As a modular architecture, the number of the series unit can be optimally selected to meet the voltage requirements. The number of the parallel units can be optimally selected to meet the current requirements. With modular switched-capacitor and switched-inductor building blocks, the proposed converter can be linearly extended with synchronized control strategy.

Fig. 2 shows another embodiment of the proposed architecture. It comprises two series units and one parallel unit. The two stacked series units perform a 2:1 voltage conversion on the input side. The switch nodes of the half-bridge structure are treated as a merged ac bus that is loaded with one switched-inductor circuit [11]. The tapped inductor is connected to the two series stacked switched capacitor building block through two series resonant capacitors C_{Ar} and C_{Br}. S_{A1} is synchronized with S_{B1} as Φ_1, and S_{A2} is synchronized with S_{B2} as Φ_2. The switches of all the parallel units are synchronized to Φ_2. Φ_1 and Φ_2 are switched in complementary to each other as regular PWM operation. The capacitors C_{Ar} and C_{Br} have equal capacitance and both resonate with the leakage inductance of L_r. They block different dc voltage and carry identical ac current. More specifically, C_{Ar} needs to block an extra $V_{IN}/2$ voltage than C_{Br}. The resonant current through C_{Ar} and C_{Br} enables soft-switching of all the half-bridge switches. The overall voltage conversion ratio of this example embodiment can reach 24:1 with regulated output.

The topology in Fig. 1 has multiple split ac buses, and the topology in Fig. 2 has a single merged ac bus. With multiple split ac buses, these input side capacitors can naturally balance the input voltage with the same power drawn from each series unit. In a merged ac bus design (where all the series units are tied to a single node as illustrated in Fig. 2), C_{Ar} and C_{Br} can be considered as being connected in series to function as one capacitor of the switched capacitor circuit. The switched capacitor mechanism naturally balance the voltage sharing among the many series units. However, in a merged ac bus design, the current sharing among the multiple current paths is sensitive to capacitance value mismatch. Benefiting from the fact that the resonant capacitor blocks dc current, a split ac bus implementation enables automatic current sharing among multiple submodules, which is needed in high current

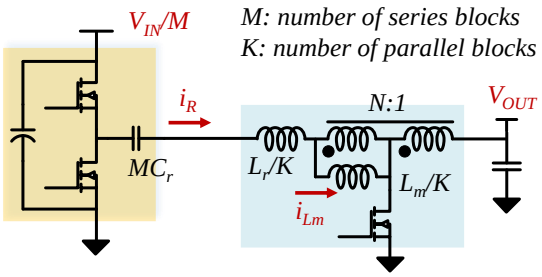


Fig. 4: Analytical model of a MSP-LEGO converter with M series units and K parallel units. V_{IN}/M is the input voltage, MC_r is the series resonant capacitance. L_r/K and L_m/K are the leakage and magnetizing inductances.

applications. However, for the split ac bus structure, the number of the parallel units must be equal to the number of the series units. Fig. 3 shows a hybrid ac bus structure with two series units and four parallel units. Two parallel units are connected in pair to a virtual ac bus created by one series unit.

III. Circuit Topology and Operation Principles

The MSP-LEGO converter can be designed following the design methods of a tapped series capacitor buck converter as described in [10]–[12]. In Fig. 2, the impedance that the parallel unit sees from its input side is the equivalent parallel impedance of all the series units. The impedance the series unit sees from its output side is the equivalent parallel impedance of all the parallel units. An MSP-LEGO architecture with M series units and K parallel units (e.g., in Fig. 2, $M = 2$ and $K = 1$), can be simplified as a lumped circuit model as shown in Fig. 4, where the input voltage reduces to V_{IN}/M, the series resonant capacitance becomes MC_r, the leakage inductance becomes L_r/K, the magnetizing inductance becomes L_m/K, the coupled inductor turns ratio remains $N:1$. Following the derivation in [9]–[11], assuming a large enough C_r, the voltage conversion ratio of an architecture with M series units and K parallel units is:

$$\frac{V_{out}}{V_{in}} = \frac{1}{M}\frac{(N+1)DL_m}{(N+1)^2L_m - N^2L_r}. \quad (1)$$

Here D is the duty ratio of the top switch of the half bridge (i.e., the duty ratio of Φ_1). Appendix I presents a detailed derivation considering the voltage variation of C_r. Fig. 5 compares the voltage conversion ratio of the proposed MSP-LEGO converter against that of a buck converter, a 2:1 tapped inductor buck converter, and a two-stage design with a 2:1 dc transformer. The tapped series capacitor buck converter offers the highest voltage conversion ratio with the same duty ratio. The stacking of the M series units linearly extend the voltage conversion ratio by a factor of M. Benefiting from the hybrid PWM-resonant mechanism, the MSP architecture significantly increase the voltage conversion ratio for a given duty ratio, and offers ZVS opportunities to all switches. The equivalent capacitance MC_r should be sized to resonate with L_r/K at the switching frequency f_{sw}. Note the voltage rating of the series resonant capacitors in different submodules are different. In some applications, the center-tapped switch Q can

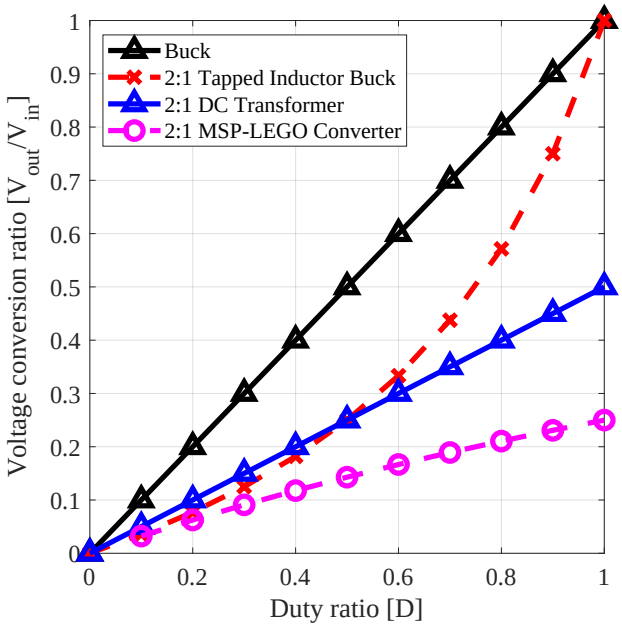


Fig. 5: Duty ratio and voltage conversion ratio of a few example topologies.

be implemented as a diode at the cost of additional forward voltage drop loss.

Similar to a tapped series capacitor circuit, all switches in the proposed MSP-LEGO converter can achieve ZVS, enabling high performance operation of the converter at high frequencies. As shown in Fig. 6, there are two resonant transients during one switching cycle. In Φ_1, C_r resonates with $L_r + L_m$ at frequency ω_1; In Φ_2, C_r resonates with L_r at frequency ω_2. Since L_m is usually much larger than L_r, ω_1 is usually much smaller than ω_2. The waveform of i_r in Φ_1 can be approximated as linear. The key principle to enable ZVS of all switches is to optimize C_r, L_r, L_m and f_{sw} such that: a) at the beginning of Φ_1, the resonant current, $i_r(0)$, is slightly negative; and b) at the end of Φ_2, the resonant current ring back to its initial value at the beginning of Φ_1. One shortcoming of tapped series capacitor buck converter is high output current ripple, which can be partially addressed by interleaving multiple phases (as shown in Fig. 6g).

With different input voltage, a variable on-time (duration time of Φ_1), fixed off-time (duration time of Φ_2) control strategy can be used to enable soft-switching. With higher input voltage, the duration time of Φ_1 is short, leading to higher switching frequencies. With a lower input voltage, the duration time of Φ_1 is long, leading to lower switching frequencies. However, as the output power increases, the resonant current $i_r(0)$ will inevitably exceed zero, and the ZVS turn on of S_1 is lost. One solution is to increase the current ripple of i_r by reducing the leakage inductance and magnetizing inductance.

For a single tapped series capacitor buck converter, the voltage stress of half-bridge switch is the same as input voltage V_{in}. However, with M series units in the MSP architecture, the voltage stress can be reduced to V_{in}/M. Also for the same output current, with K parallel units, the current stress of center-tapped switch is reduced to be $1/K$. As illustrated in

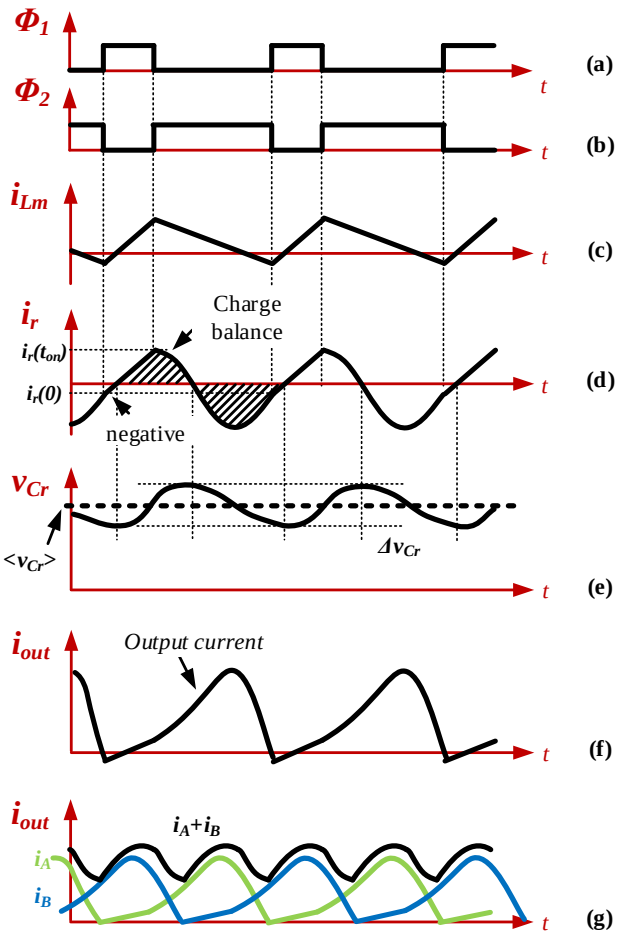


Fig. 6: Key current and voltage waveforms of the MSP-LEGO converter.

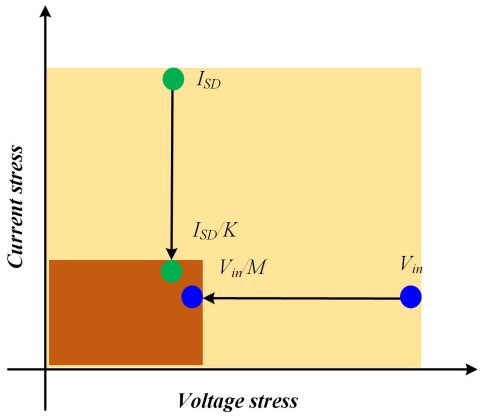


Fig. 7: The proposed MSP-LEGO architecture 1) decouples voltage stress and current stress with the coupled inductor, and 2) linearly allocates the voltage stress and current stress to different switches and building blocks. The effective semiconductor die area (product of voltage rating and current rating) can be significantly reduced by decoupling the voltage stress and current stress.

Fig. 7, both the voltage stress and current stress are optimally allocated by the series-input parallel-output configuration.

The dc blocking voltage of the resonant capacitor C_r in a single tapped series capacitor buck converter is:

$$V_{Cr} = V_{in} \times D - V_{out}. \tag{2}$$

Hence, in the proposed MSP architecture comprising M series units, the DC voltage of resonant capacitor in i unit from bottom to top is $(1 \leq i \leq M)$:

$$V_{Cr_i} = \frac{V_{in}}{M} \times D - V_{out} + \frac{i-1}{M} \times V_{in}. \tag{3}$$

The voltage conversion ratio of the converter shown in Fig. 1 is 36:1 (3:1 from the switched capacitor units, 12:1 from the switched inductor units with 33% duty ratio), which is equivalent to the total voltage conversion ratio of a 3-stage design with a 6:1 switched-capacitor converter, a 3:1 buck converter with 33% duty ratio, and a dc transformer with 2:1 turns ratio. The 6:1 switched-capacitor converter can be implemented as a switched-tank converter (STC) [17], [18]. The MSP-LEGO architecture functions more like a single-stage high conversion ratio design, and inherits the advantages and shortcomings of single-stage architectures. Compared to a merged STC and Buck two-stage solution [8], the MSP-LEGO solution offers lower component count and better soft-switching capability at high frequencies.

IV. Extended Design Options

Fig. 8 shows a few extended design options for the MSP-LEGO architecture with a variety of different building blocks. Fig. 8a is a MSP-LEGO design with half-bridge rectifiers as the modular parallel units. This implementation is also referred to as "switched-tank converter" in [17] with a series L-C resonant tank linking the series units and parallel units. Fig. 8b is a MSP-LEGO design with an isolated half-bridge rectifier as the modular parallel units. This implementation offers galvanic isolation and additional voltage conversion ratio through the transformer turns ratio. The switches in the series-connected units are all soft-switched. Fig. 8c shows a MSP-LEGO design with two isolated parallel units with two split virtual ac buses. The two series stacked switched capacitor unit equally divided the voltage. The dc-blocking capacitors maintain current sharing among multiple parallel units. The series unit can also be modified to other switched capacitor structure. For the aforementioned embodiments, the input voltage of the parallel unit is in ac. The input of parallel unit can also be in dc as the output of the series unit. With switched capacitor circuits as the series units offering dc output, almost all dc-dc converters can be adopted as the parallel unit for the MSP-LEGO architecture.

V. Experimental Results

A 150 Vdc-to-5 Vdc, 20 A, 100 W prototype is built and tested to verify the effectiveness of the proposed MSP-LEGO power conversion architecture. The voltage conversion ratio of this prototype is 30:1. Fig. 9 shows the schematic of the prototype which comprises two 180^o interleaved modules. As illustrated in Fig. 6g, the interleaved configuration significantly reduced the output current ripple. The Bill-of-Material (BoM) the prototype is listed in Table I. The switching frequency is 600 kHz and the duty ratio is 35% (Φ_1). The volume of the passive components can be further reduced by increasing the switching frequency at the cost of higher loss. Low output capacitance is needed for switch Q_1 and Q_2 to reduce the

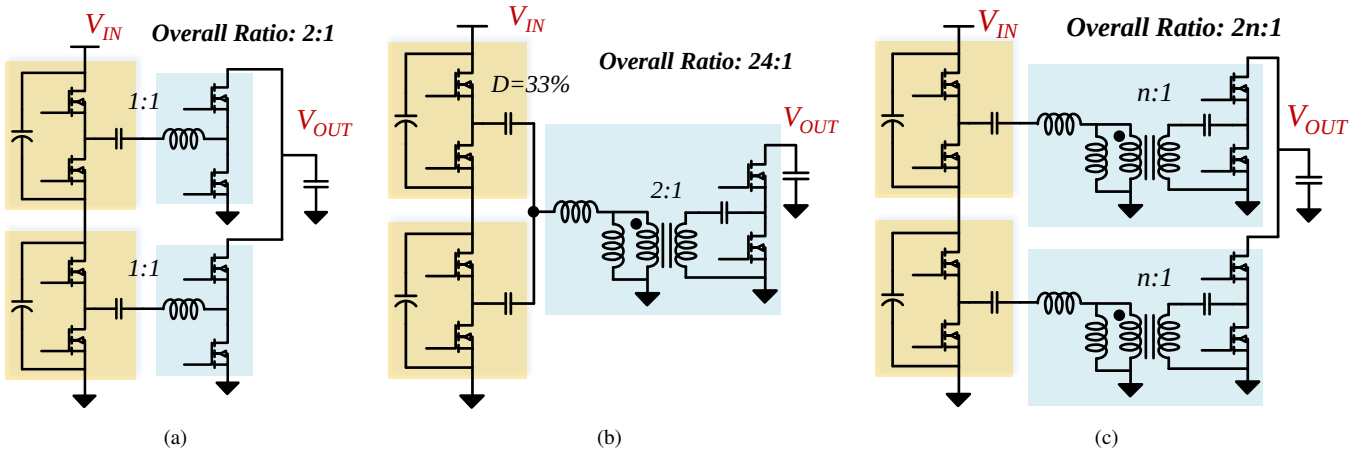


Fig. 8: Example MSP-LEGO implementations with a variety of series-parallel building blocks: (a) half-bridge circuit as the parallel unit (switched-tank converter); (b) isolated half-bridge circuit as the parallel unit; (c) isolated parallel units with split virtual ac bus.

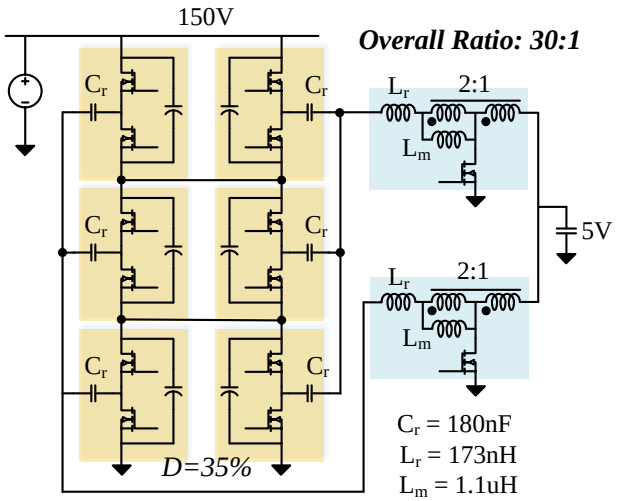


Fig. 9: Schematic of the prototype 30:1 converter comprising two 180^o interleaved modules.

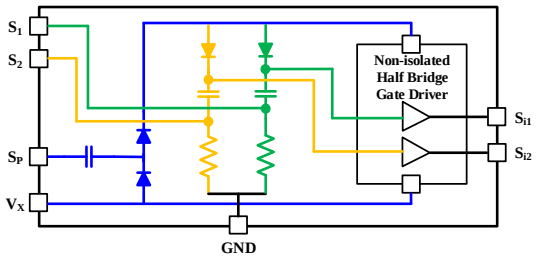


Fig. 10: Modular gate drive implementation of the series unit with non-isolated half bridge gate driver.

TABLE I: Bill of Materials (BOM) of the Prototype Converter.

Device Symbol	Component Description
C_{Ar}, C_{Dr}	C0G Ceramic, 200V, 100 nF+39 nF+2x22 nF
C_{Br}, C_{Er}	C0G Ceramic, 100V, 100 nF+39 nF+2x22 nF
C_{Cr}, C_{Fr}	C0G Ceramic, 50V, 100 nF+39 nF+2x22 nF
L_{r1}, L_{r2}	173 nH
L_{m1}, L_{m2}	1.1 μH
$S_{A1,A2}$–$S_{F1,F2}$	TI LMG5200 integrated GaN half-bridge modules
Q_1, Q_2	2x Vishay SIR890DP silicon MOSFETs
C_A–C_F	2x X5R Ceramic, 50V, 10 μF
C_o	36x X5R Ceramic, 6.3V, 22 μF
Inductor	Ferroxcube ER18, Core material 3F45, turns ratio 2:1, 4-layer PCB

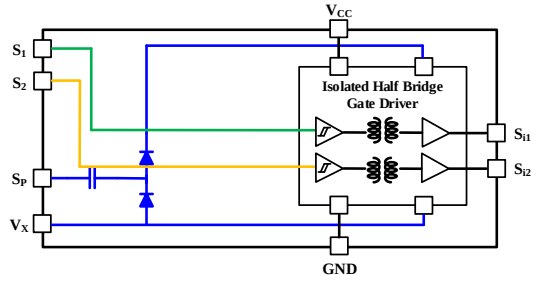


Fig. 11: Modular gate drive implementation of the series unit with isolated half bridge gate driver.

voltage ringing during the switch turn-off transition. Connecting multiple switches in parallel can reduce equivalent on-resistance, however, leading to higher total output capacitance. The turns ratio of the coupled inductor is 2:1. The two coupled inductors are implemented as printed-circuit-board (PCB) planar inductors with carefully controlled leakage and magnetizing inductance. The coupled inductor is built on a four-layer PCB in which there is one turn on each layer.

Two driving and powering modules were adopted in the MSP-LEGO prototype. Fig. 10 shows the modular gate drive implementation of the series unit with non-isolated half bridge gate driver. V_X is the source voltage of bottom switch in series unit. By applying a square wave voltage at S_P, a driving voltage for the isolated voltage domain is created. Fig. 11 shows an half bridge gate driver implementation. The prototype adopted half-bridge GaN module LMG5200 with integrated gate driving circuit. Digital isolator IL711 is used to level-shift the driving signals.

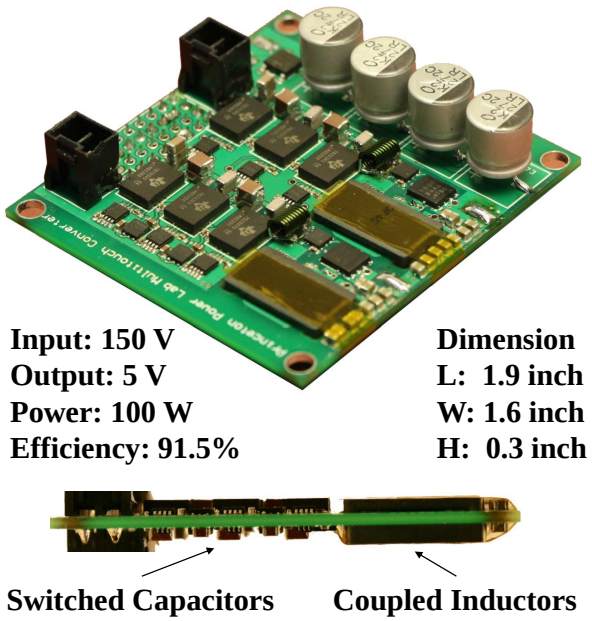


Fig. 12: Picture of the 110 W/in^3 MSP-LEGO prototype: (a) top view; (b) side view. The building blocks are highly modular and can be linearly extended.

Fig. 12 shows the prototype 30:1 MSP-LEGO dc-dc converter. The dimension of the power stage is 1.9×1.6×0.3 inch. The power density of this converter is 110 W/in^3. The electrolytic capacitors on the input side are the tallest components on board. All auxiliary circuit, e.g., the boot-strap floating supply, gate drivers, and level-shifters are included. Fig. 13 shows the measured waveform of the prototype delivering 3 A and 10 A. The negative current at the beginning of Φ_1 enables soft switching of all switches in both conditions. Fig. 14 shows the thermal images of the prototype under different output current conditions. With soft-switching, the half bridge module is very efficient. The hottest components on the PCB are the coupled inductor and the tapped switch. The heavy resonant current through the coupled inductor and the tapped switch contribute most of the system loss. Fig. 15 shows the measured efficiency of the prototype. The system efficiency achieves a peak efficiency of 91.5% with 10 A of output current. The converter can deliver a maximum current of 20 A. The converter maintains above 88% efficiency across a majority of the power range.

Fig. 16 shows the output voltage dynamic response of the prototype when input voltage steps down and steps up (with open-loop control). When the input voltage decreases from 150 V to 120 V, the output voltage fluctuation is around 600 mV. By reducing the duty cycle D, the output voltage can be regulated to the reference value and the settling time is about 400 ms. When the input voltage increases from 120 V to 150 V, the output voltage overshoot and settling time are also about 600 mV and 400 ms. In this prototype, the duty cycle is adjusted by continuous increment or decrement of control variable value in the digital controller. The dynamic performance can be further improved with advanced control strategy, such as feedforward control, in the future work. Fig. 17 shows the output voltage dynamic response of the

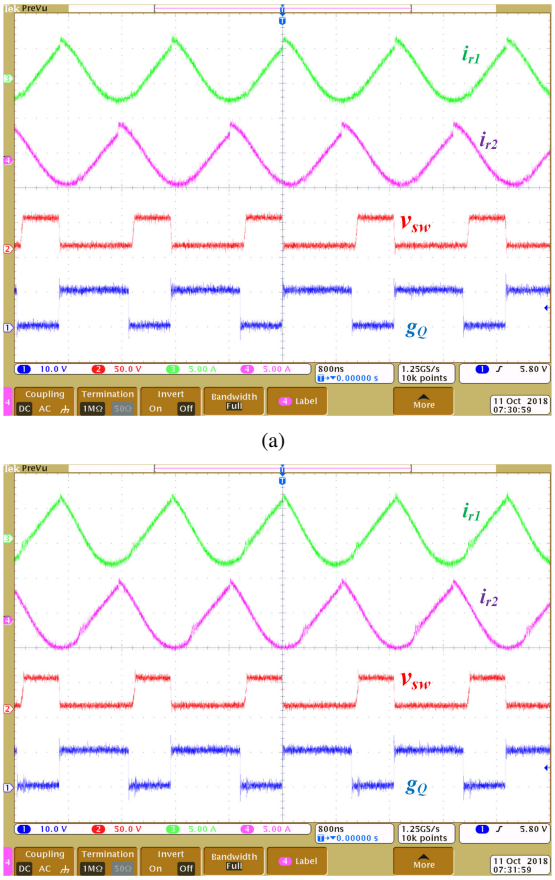


Fig. 13: Measured waveform of the MSP-LEGO prototype. i_{r1} and i_{r2} are the resonant current, v_{sw} is the switch node voltage, and g_Q is the gate drive voltage. (a) output current is 3A; (b) output current is 10A.

prototype when output current steps down and steps up. The output voltage ripple is very small.

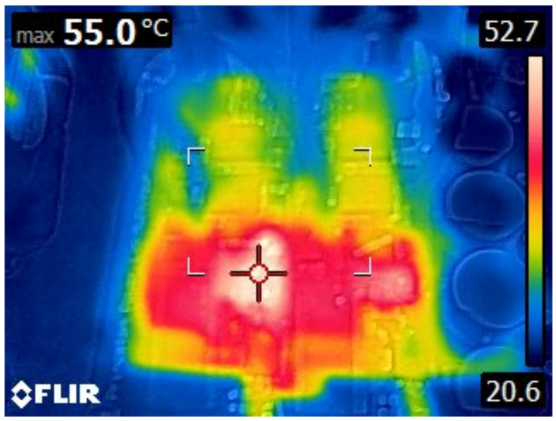
VI. Conclusions

This paper presents a MSP-LEGO power conversion architecture with hybrid-switched-capacitor building blocks and resonant-PWM operation, offering high power-density and high voltage conversion ratio. By decoupling the voltage stress and current stress in the switches with the MSP-LEGO architecture, the overall semiconductor die area of the converter can be reduced. The operation range of the system can be freely modified by linearly extending the number of switch-capacitor units and switch-inductor units. A non-isolated 150 Vdc-to-5 Vdc, 20 A prototype is built and tested to verify the advantages of the architecture. The peak efficiency of the prototype is 91.5%. The power density of the prototype is 110 W/in^3. The converter offers regulated output voltage and maintains high performance across a wide operation range.

Acknowledgements

The authors would like to thank National Science Foundation (under Award #1847365), the School of Engineering and Applied Science (SEAS) Innovation Fund, and the Andlinger Center for Energy and the Environment (ACEE) of Princeton University for supporting this work.

(a)



(b)

Fig. 14: Thermal image of the MSP-LEGO prototype. (a) output current is 3A; (b) output current is 10A.

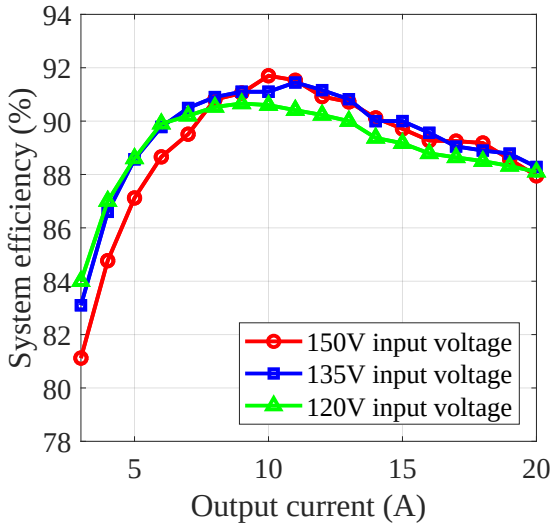


Fig. 15: Measured efficiency of the MSP-LEGO prototype. The prototype achieves its peak efficiency at 10 A. The output voltage of the prototype can be regulated by controlling the duty ratio of the switched capacitor stage.

APPENDIX I

The resonant frequency (and the size) of the C_r & L_r resonant tank is on the same order of magnitude as the switching frequency. In high frequency MSP-LEGO designs, both C_r and L_r are small, and the voltage ripple of C_r cannot be neglected when calculating the voltage conversion ratio. Here we derive the voltage conversion ratio of the MSP-LEGO converter considering the voltage variation in C_r. In Φ_1, the voltage of C_r (v_{Cr}) and the current of L_r (i_{Lr}) are:

$$\begin{cases} v_{C_r}(t) = \frac{V_{in}}{M} - V_o + A\sin(\omega_{r1}t + \beta), \\ i_{L_r}(t) = \frac{A}{Z_{r1}}\cos(\omega_{r1}t + \beta). \end{cases} \tag{A.1}$$

here $\omega_{r1} = \frac{1}{\sqrt{C_r(L_r+L_m)}}$ and $Z_{r1} = \sqrt{\frac{L_r+L_m}{C_r}}$.

Here β is the initial phase of resonant voltage or current. In Φ_2, the voltage of C_r and the current of L_r are:

$$\begin{cases} v_{C_r}(t) = nV_o + B\sin(\omega_r(t - DT_s) + \gamma) \\ i_{L_r}(t) = \frac{B}{Z_r}\cos(\omega_r(t - DT_s) + \gamma) \end{cases} \tag{A.2}$$

where $\omega_r = \frac{1}{\sqrt{C_r L_r}}$ and $Z_r = \sqrt{\frac{L_r}{C_r}}$.

Ignoring the deadtime, the voltage and current should be continuous during the transition. Also based on the ampere-second balance principle of the capacitor current and the voltage-second balance principle of inductor voltage during one period, a more accurate expression for the voltage conversion ratio is:

$$\frac{V_o}{V_{in}} = \frac{1}{M} \times \frac{1}{1 - \frac{(n+1)T_s(1-D)\omega_{r1}}{\left(1-\frac{L_r}{L_r+L_m}\right)(\cos(\omega_{r1}T_sD+\beta)-\cos\beta)}} \tag{A.3}$$

The voltage conversion ratio is related with the time when the resonant current reaches zero, which can be calculated based on the discharging time of output capacitance of the switches. Emperically, the value of β can be selected as $\frac{\pi}{3}$ or $\frac{\pi}{4}$. With these approximations, the voltage conversion ratio can be explicitly calculated. In general,the system voltage gain considering capacitor voltage variation is smaller than the conventional calculation method assuming a constant capacitor voltage. As a result, we expect to observe reduced voltage conversion ratio in high frequency MSP-LEGO designs with small C_r size.

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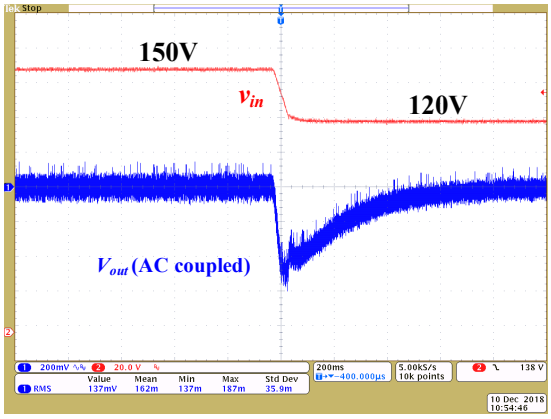
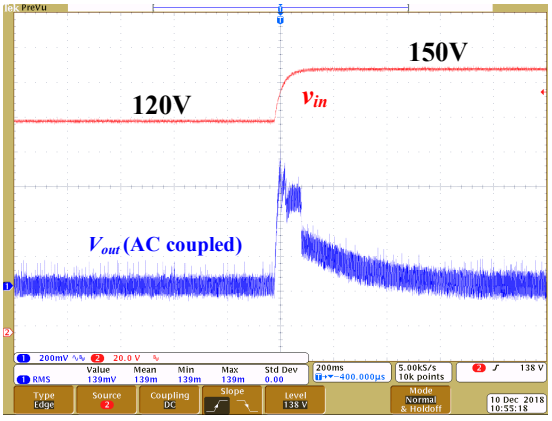
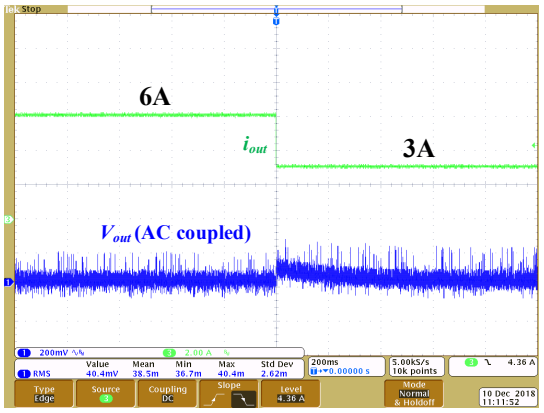


(a)

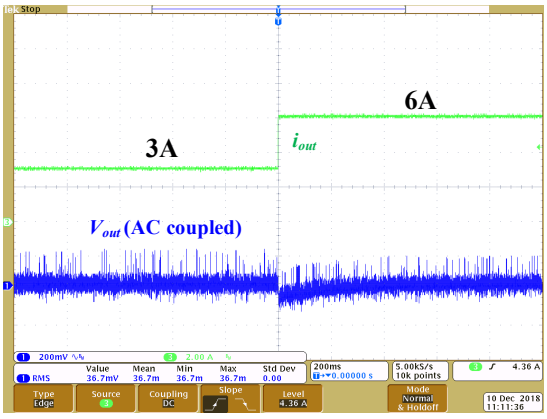


(b)

Fig. 16: Output voltage dynamic waveforms of the MSP-LEGO prototype when input voltage steps down and steps up. (a)input voltage changes from 150 V to 120 V; (b) input voltage changes from 120 V to 150 V.



(a)



(b)

Fig. 17: Output voltage dynamic waveforms of the MSP-LEGO prototype when output current steps down and steps up. (a)output current changes from 6 A to 3 A; (b) output current changes from 3 A to 6 A.

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