Highly stable amorphous-silicon thin-film transistors on clear plastic

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Hydrogenated amorphous-silicon (*a*-Si:H) thin-film transistors (TFTs) have been fabricated on clear plastic with highly stable threshold voltages. When operated at a gate field of 2.5×10^5 V/cm, the threshold voltage shift extrapolated to only ~1.2 V after ten years. This stability is achieved by a high deposition temperature for the gate silicon nitride insulator which reduces charge trapping and high hydrogen dilution during *a*-Si:H growth to reduce defect creation in *a*-Si:H. This gate field of 2.5×10^5 V/cm is sufficient to drive phosphorescent organic light emitting diodes (OLEDs) at a brightness of 1000 Cd/m^2. The half-life of the TFT current is over ten years, slightly longer than the luminescence half-life of high quality green OLEDs. © *2008 American Institute of Physics*. [DOI: 10.1063/1.2963481]

Amorphous-Si (*a*-Si) thin-film transistors (TFTs) are in universal use for active-matrix liquid crystal displays (AMLCDs) and the existing industrial infrastructure is capable of providing cost-effective large-area deposition of *a*-Si, a technology transferable to clear flexible plastic substrates.[1] However, the stability requirement for the TFT threshold voltage (V_T) is more stringent for driving organic light emitting diodes (OLEDs) than for driving AMLCDs. In AMLCDs, the TFT functions as a digital switch with a low duty cycle (~0.1%), and a threshold voltage drift of a few volts can be tolerated. In AMOLED pixels, the *a*-Si driver TFT operates in dc. An increase in the V_T of the driver TFT reduces the OLED drive current and therefore decreases the brightness of the pixel. Here we show experiments that raise the lifetime of *a*-Si TFTs on clear plastic substrates to become comparable or even exceed that of high quality green phosphorescent OLEDs.

The *a*-Si TFT samples were made on clear plastic substrates with either a "back-channel-etched" (or "etched") structure, where the top of the *a*-Si channel is exposed to the atmosphere after fabrication, or a "back-channel-passivated" (or "passivated") structure using standard *a*-Si TFT structures.[2] The latter process seals the *a*-Si channel *in situ* with a SiN_x layer immediately after *a*-Si deposition at the cost of an extra mask step used for opening holes in the passivation nitride for n^+ *a*-Si source/drain contacts.

We first studied the dependence of stability on gate electric field of etched TFTs with different deposition temperatures for the gate SiN_x [Table I, samples (a)–(c)]. All TFTs were made with 300-nm-thick gate nitride layers grown at a plasma power density of 22 mW/cm^2 and a chamber pressure of 500 mtorr. The 250-nm-thick *a*-Si layers were grown at a chamber pressure of 500 mtorr and at a plasma power density of 17 mW/cm^2. The 30-nm-thick n^+ *a*-Si layers were grown at 250 °C for the 285 and 250 °C processes, and at 200 °C for the 200 °C process, at 17 mW/cm^2 and 500 mtorr. The gate SiN_x deposition temperature is the highest temperature process step and hereafter we will refer to it as the process temperature. All TFTs were annealed at 180 °C in vacuum for 1 h to repair plasma etch damage.

Higher process temperatures yielded devices with higher V_T stability, with 285 °C process resulting in most stable devices.[3,4] At high gate electric fields (~10^6 V/cm and above), charge trapping in the gate nitride was the dominant instability mechanism.[5] The data closely fit a logarithmic model with λ close to 2 as expected:[6]

$$\Delta V_T \propto (\log t)^{\lambda}. \tag{1}$$

The recent development of high-efficiency phosphorescent OLEDs allows the operation of *a*-Si TFTs at lower device currents hence lower gate voltages where ΔV_T is expected to be lower.[7] For all low-field stress measurements in this letter, the TFTs were biased in saturation (with a constant drain voltage of 12 V) and ΔV_T was calculated from the measured drop in the saturation current. The measured change in mobility was negligible as seen in previous works.[8–12] Saturation measurements were done for two reasons: (i) saturation is the realistic operating condition in active-matrix organic light emitting diode (AMOLED) pixels, and (ii) changes in saturation current allow more accurate measurement of small ΔV_T's than linear measurements. The ΔV_T of the TFTs at a gate stress field of $\sim 2.5 \times 10^5$ V/cm (gate voltage of ~7.5 V) could be fitted to the logarithmic model only with $\lambda = 4.9$ which does not match the value expected for charge trapping ($\lambda \cong 2$). Furthermore, extrapolating ΔV_T versus gate field from high field data (above 10^6 V/cm) down to low field (below 2.5×10^5 V/cm) underestimates the shift at low field. These both suggest that a different mechanism dominates the shift at low gate electric fields. Due to the statistical variation of the TFT threshold voltages (Table I), the gate stress voltages were slightly adjusted for each TFT measurement to assure the same $V_{GS} - V_T$ of ~5.3 V and therefore the same initial saturation current of ~30 nA/μm gate width.

At low gate fields, we find that defect creation in the *a*-Si channel dominates the threshold voltage shift. This is modeled in the literature as a stretched exponential in time which may be approximated by a power law relation at its initial time stages:[8,9]

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TABLE I. Properties and process conditions that were varied and the saturation mobility and threshold voltage of the fabricated TFTs (with standard deviations). The parameters that were held constant are described in the text. The column "Sample/Curve label" refers to the curves of Figs. 1–3. The W/L ratio is 150 μm/5 μm for all the TFTs.

Sample/ Curve label	TFT back channel	SiN_x temp. (°C)	*a*-Si:H Deposition Temp. (°C)	*a*-Si:H Deposition Pressure (torr)	*a*-Si:H Deposition $[H_2]/[SiH_4]$ flow ratio	Annealing Temp. (°C)	Mobility ($cm^2/V s$)	Threshold voltage (V)
(a)	Etched	200	200	0.5	4	180	0.65 ± 0.04	2.1 ± 0.4
(b)	Etched	250	250	0.5	0	180	0.63 ± 0.06	2.0 ± 0.3
(c)	Etched	285	250	0.5	0	180	0.63 ± 0.04	2.0 ± 0.3
(d)	Passivated	285	250	0.5	0	180	0.64 ± 0.04	2.3 ± 0.1
(e)	Passivated	285	250	0.5	0	180+260	0.62 ± 0.05	2.4 ± 0.3
(f)	Passivated	285	250	0.8	10	180	0.66 ± 0.05	2.2 ± 0.1
(g)	Passivated	285	250	0.8	10	180+260	0.61 ± 0.04	2.4 ± 0.2

$$\Delta V_T \propto t^{\beta}, \tag{2}$$

where β is a constant at a given gate stress field. The data are precisely fitted with a β of ~0.44 [Fig. 1, curves (a)–(c)] in good agreement with the literature.[8–12] Thus raising the *a*-Si TFT lifetime at low gate fields further requires improving the properties of the *a*-Si TFT channel and interface.

Therefore, a second set of samples [Table I, samples (d)–(g), and Fig. 1] was fabricated, fixing the gate SiN_x deposition temperature at 285 °C and varying the *a*-Si plasma enhanced chemical vapor deposition (PECVD) growth conditions for both etched and passivated structures. *a*-Si grown at 250 °C from pure silane and annealed at 180 °C gave a much lower ΔV_T in the passivated structure, curve (d), than in the etched structure, curve (c). An additional annealing of 1 h in vacuum at 260 °C slightly reduced ΔV_T in the passivated structure, curve (e), while this 260 °C annealing degraded the dc characteristics of the etched TFTs so much that they were not measured further. This is consistent with the lasting damage created by plasma and process chemicals to the exposed back channel. Varying the *a*-Si deposition temperature in the range of 230–280 °C in both types of devices made no significant change. Diluting the silane with hydrogen for the *a*-Si growth slightly degraded the passivated devices, curve (f), compared to the passivated devices without hydrogen dilution, curve (d). The straight line fits to (c)–(f) have β in the range of 0.36–0.44, which is again consistent with defects in the *a*-Si or at the *a*-Si/nitride interface. Finally, the 260 °C annealing of the passivated sample (g) grown with hydrogen dilution dramatically reduces the ΔV_T (a β of 0.21). Extrapolating ΔV_T of this TFT gives ~1.2 V after ten years of continuous operation, curve (g). This extrapolation provides a conservative estimate for long-term TFT threshold voltage shifts because extrapolating with a power law relation [Eq. (2)] neglects the saturation of defect density at long stress times.[8,9]

Hydrogen dilution in PECVD is thought to increase the stability of *a*-Si solar cells by removing the weak Si–Si bonds that are potentially later broken.[13] A similar mechanism may explain the improvement in the TFT stability.

Figure 2 compares the stability of the TFT with improved *a*-Si [curve (g)] and the standard etched and passivated TFTs [curves (d) and (e)] with the stability of the TFTs on glass substrates reported in the literature. Because of the different bias stress conditions, and since the ΔV_T induced by

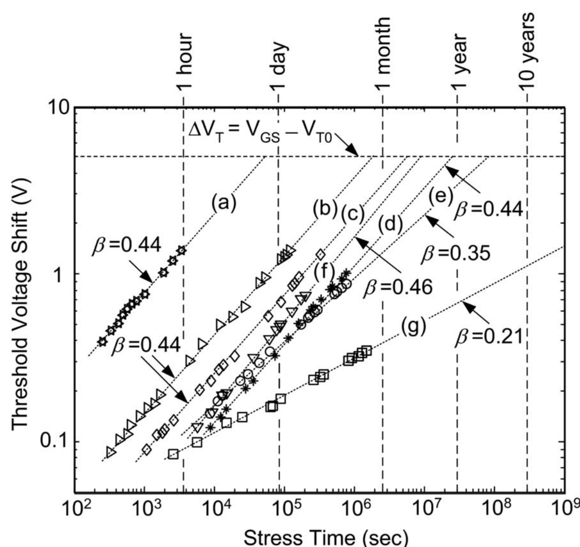

FIG. 1. ΔV_T vs time [symbols, data points; lines, extrapolations based on Eq. (2)] of the test TFTs (Table I) at a gate field of $\sim 2.5 \times 10^5$ V/cm.

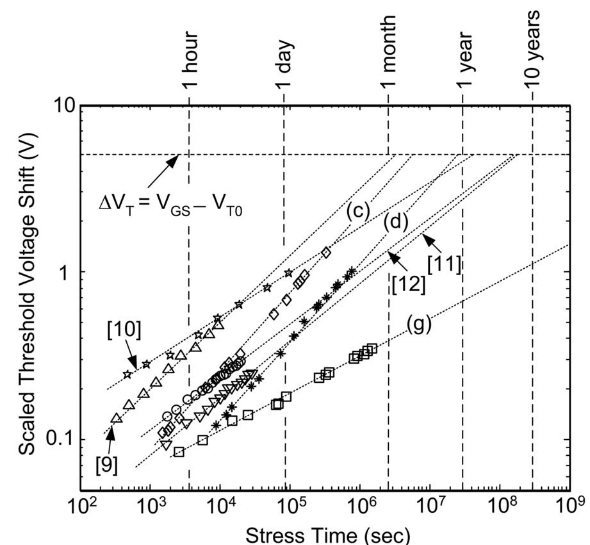

FIG. 2. ΔV_T vs time (symbols, data points; lines, extrapolations) of the test TFTs (c), (d), and (h) (Table I) and the scaled ΔV_T of *a*-Si TFTs reported in literature (Refs. 9–12) based on Eq. (3). The TFT parameters are Ref. 9 etched TFTs, V_{GS}=20 V, V_{T0}=2.5 V, insulator: SiN_x 500 nm; Ref. 10: passivated TFTs, V_{GS}=25 V, V_{T0}=4.5 V, insulator: SiO_x 300 nm+SiN_x 50 nm; Ref. 11: passivated TFTs, V_{GS}=8 V, V_{T0}=1.3 V, insulator: SiN_x, 300 nm, Ref. 12: passivated TFTs, V_{GS}=15 V, V_{T0}=2.7 V, insulator: SiN_x, 200 nm. Relative dielectric constants of 7.5 and 3.9 were assumed for all nitride and oxide insulators, respectively.

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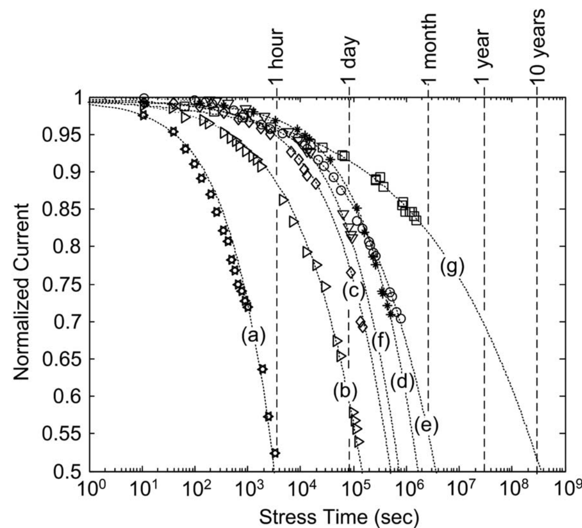

FIG. 3. Normalized TFT drain current measured in saturation (V_{DS}=12 V) at a constant gate field of $\sim 2.5\times 10^5$ V/cm [symbols, data points; lines, extrapolations based on Eq. (2)] for all curves of Fig. 1, with the same labels.

defect creation is proportional to the accumulation charge in the TFT channel,[8,9] the ΔV_T reported by other groups has been scaled by the ratio of the accumulation charge per unit area of the channel at their bias stress conditions (Q_{ch}) to that of ours ($Q_{ch,PU}$) for a fair comparison[11] (C_{ins} is the gate dielectric capacitance per unit area of the channel, V_{T0} is the initial threshold voltage, and the subscript PU refers to our TFTs):

$$\Delta V_{T,\mathrm{scaled}} = \Delta V_T \times \frac{Q_{\mathrm{ch,PU}}}{Q_{\mathrm{ch}}} = \Delta V_T \times \frac{(2/3)C_{\mathrm{ins,PU}}(V_{\mathrm{GS,PU}} - V_{T0,\mathrm{PU}})}{C_{\mathrm{ins}}(V_{\mathrm{GS}} - V_{T0})}. \quad (3)$$

The coefficient of 2/3 accounts for the lower accumulation charge in the saturation regime (where our TFTs were stressed) compared to the linear regime.[11] While the stability of TFTs made with standard *a*-Si is comparable to the previous work, the TFT made with the improved *a*-Si is significantly more stable. This indicates an improvement in the properties of the *a*-Si TFT channel and interface.

Figure 3 shows the measured and extrapolated drop in the drain saturation current (gate voltage of ~7.5 V and drain voltage of 12 V) for all of our devices (Table I). Results plotted this way show how the pixel current (i.e., the driver TFT current) drops with time at a fixed data voltage input (i.e., gate voltage of the driver TFT) in an AMOLED pixel. The chosen data voltage produces a current that generates a luminance of 1000 $\mathrm{Cd/m^2}$ on the green phosphorescent OLEDs of 57 Cd/A efficiency. A pixel size of 500 $\times 500\ \mu\mathrm{m}^2$ needs a driver TFT with channel width/length (W/L) ratio of 150 μm/5 μm (or $W/L \approx 1$ for a 100 $\times 100\ \mu\mathrm{m}^2$ pixel size).[4] The time over which the OLED luminance decays to 50% under constant current is defined as the OLED half-life. Similarly we define the time over which the TFT current drops to 50% of its initial value under constant voltage bias in saturation as the TFT half-life, which is more than ten years (80 000 h) for the improved *a*-Si. This is comparable or exceeds the half-life of high quality green phosphorescent OLEDs (65 000 h).[7]

In summary, we demonstrated *a*-Si TFTs fabricated on clear plastic with an extrapolated half-life of approximately ten years. The critical elements are a high temperature plastic, hydrogen dilution during *a*-Si growth, and a back-channel passivated TFT structure. This result suggests that *a*-Si may qualify as the backplane semiconductor in the commercial production of AMOLED displays on clear plastic substrates.

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